REPORT
on
EE 671: VLSI DESIGN Assignment-2

Part-A)

The logarithmic adder using Brent Kung architecture for adding 32-bit operands was implemented using Structural Type of Architecture. The final circuit was implemented and a few vectors were given as the testbench to check the outcome of the circuit. The simulation results are as follows:

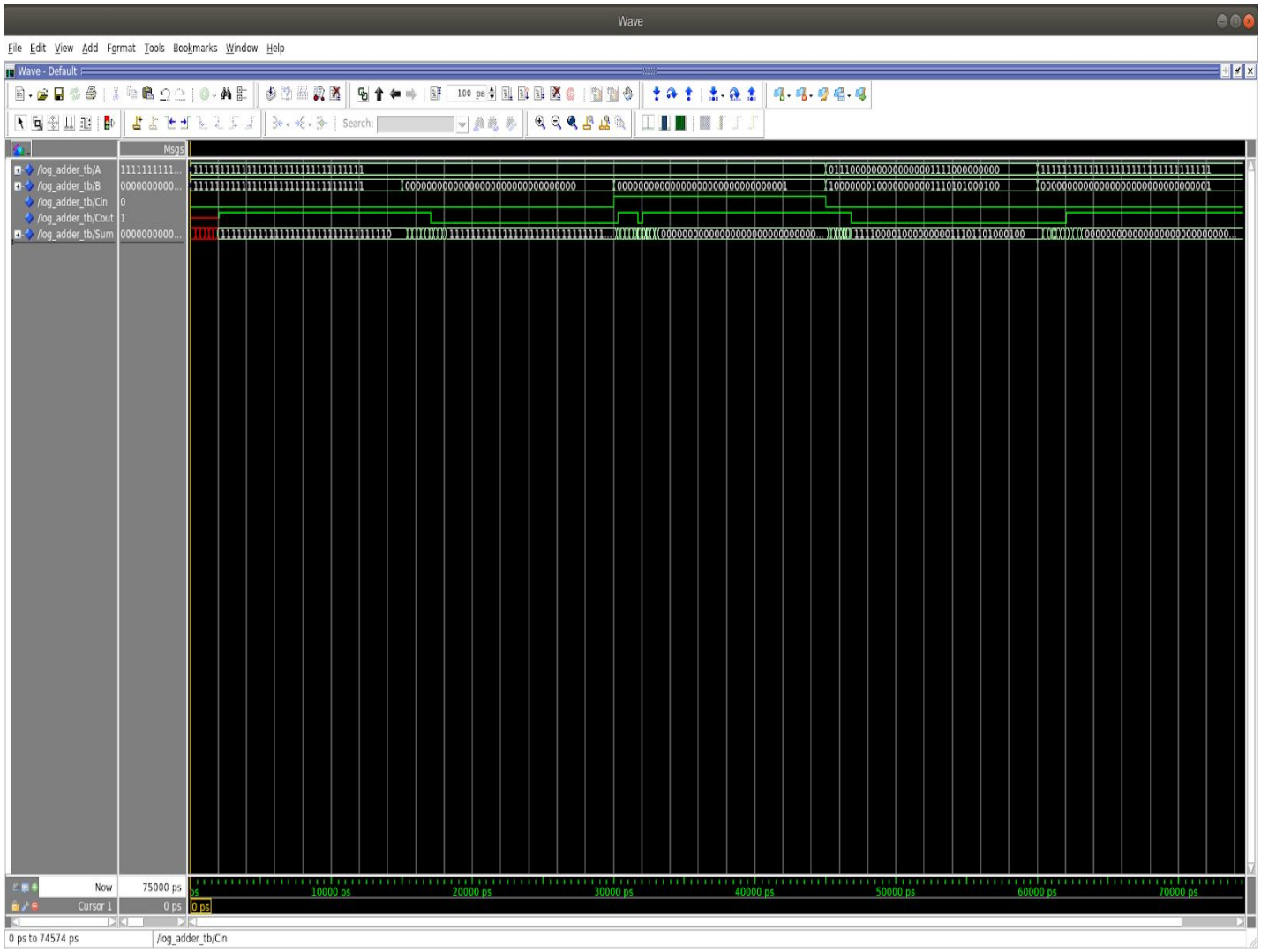

Fig-1: Simulation Results.

The photo is added to the assignment folder.

Part-B)

Critical Path: In parallel adders, the critical path is decided by computation of the carry from least significant bit (LSB) adder to the most significant bit (MSB) adder. The critical path is decided by the odd bits of carry generated. One of the odd bits always decide the critical path.In the worst case C_31 is generated in the last. After the generation of **'Carry'** for all the stages, the **'Sum'** of all the bits is calculated and the final result is calculated. The worst-case arises when the carry propagates from the LSB to MSB, that is(example):

{G=AB=0} and {P=(A xor B)=1} with LSB of A=B=1 and Cin=0.

The **Sum** for any case is guaranteed at **3.15 ns(max)** with **Cout** available at **2.05 ns(max)** which is shown in the simulation results. The photo is also available in the folder.

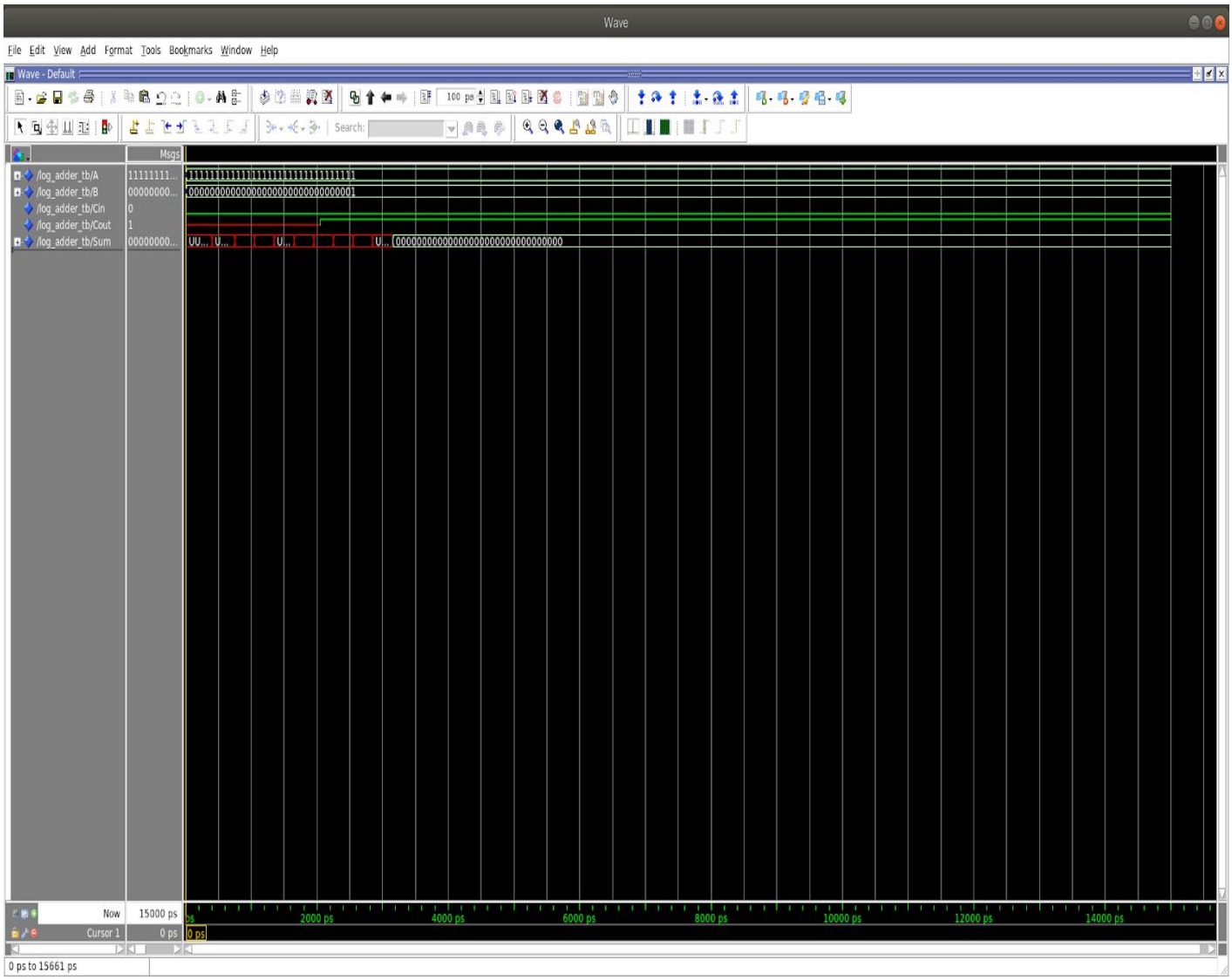

Fig-2: Worst Case Delay.