REPORT
on
EE 671: VLSI DESIGN Assignment-3

Part-A)
The Dadda multiplier for unsigned 16x16 bit multiplication with a Brent Kung adder for the final addition was implemented using VHDL and the design was simulated using appropriate test vectors. The delays were not included and the result obtained is shown in image titled as **"PART-A.png"**. A python script was used for generating the VHDL Code. The script file is also included in the assignment folder. The name of the script is **"logic_generator.py"**.

Part-B)
The delays were added for the constituent components and the design was re-simulated. RTL simulation and Gate-Level Simulation was done. The results are shown in images titled as **"Part-B-Gate_Level.png"** and **"Part-B-RTL.png"**.

CRITICAL PATH: It is dependent on the wires present in the 16th bit which has 16 wires. All the wires of the 16th bit(including carry from the 15th bit) will pass through full adders and hence will arrive after all the wires in other bits. The maximum time taken till all the bits reach the final stage after reduction (before adding using Brent Kung Adder) is **2.65 ns.** The final product depends on the input to the Brent Kung Adder and it is available at **5.4 ns**(Max) or before.

The maximum propagate bits to the Brent Kung can be generated for any **30 bits only.**
One such test vector is:

A<="1111111111111110";
B<="1000000000000001";

For this test vector, the product is available at 5.4 ns.

***All the images are in the folder named "Images".**