University of Southern California

Viterbi School of Engineering

EE577A

VLSI System Design

Sequential Logic – Flip-Flop Design

References: Online resources and research papers

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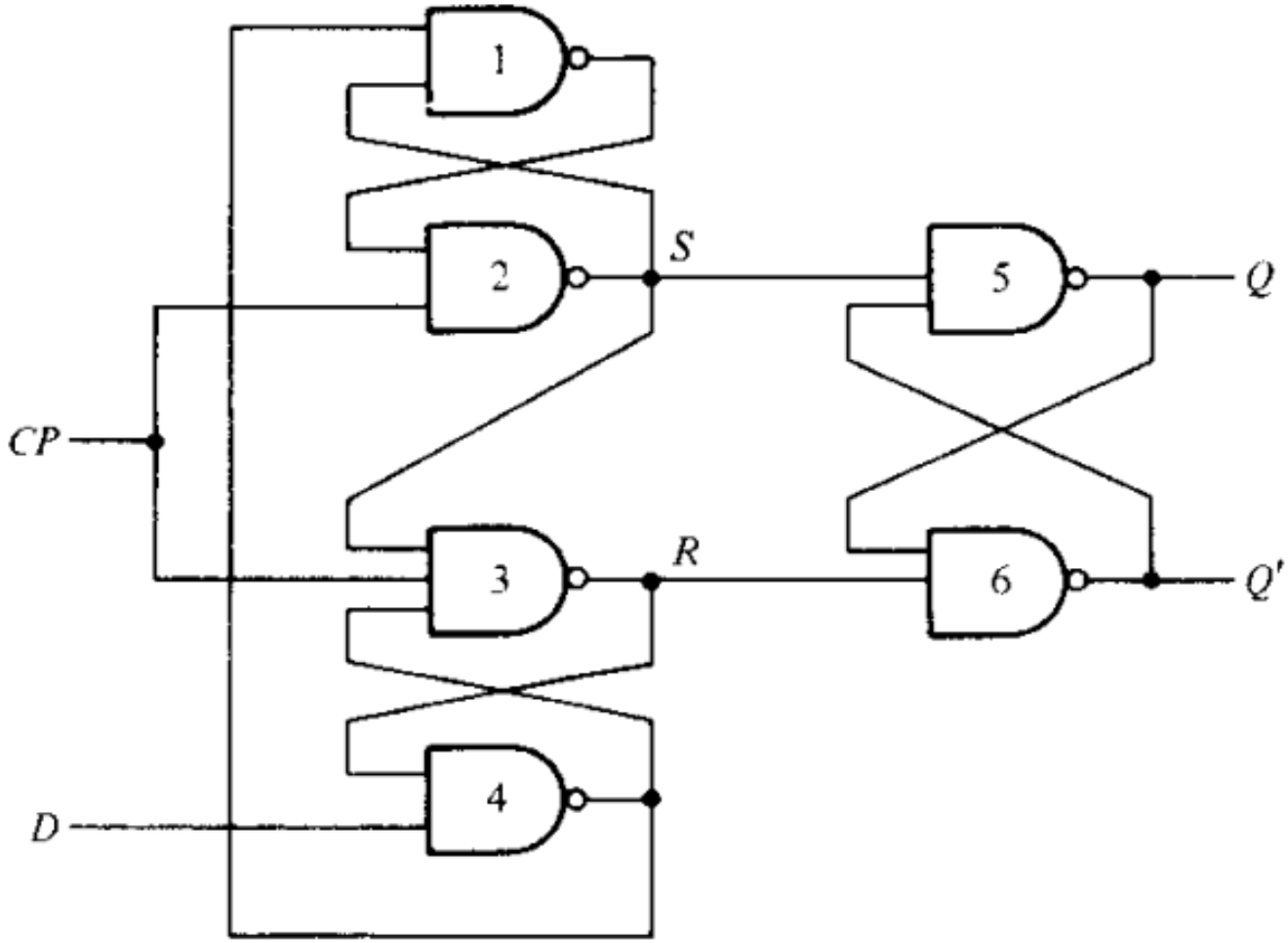
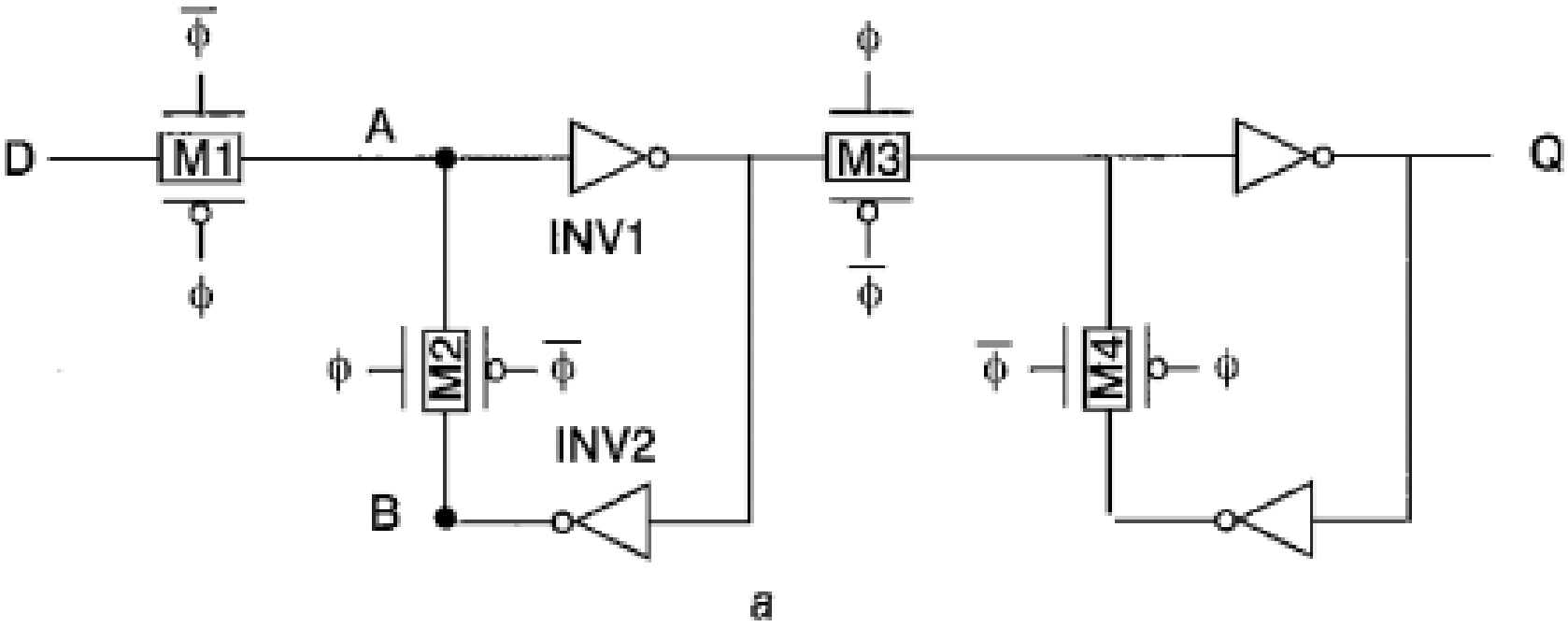
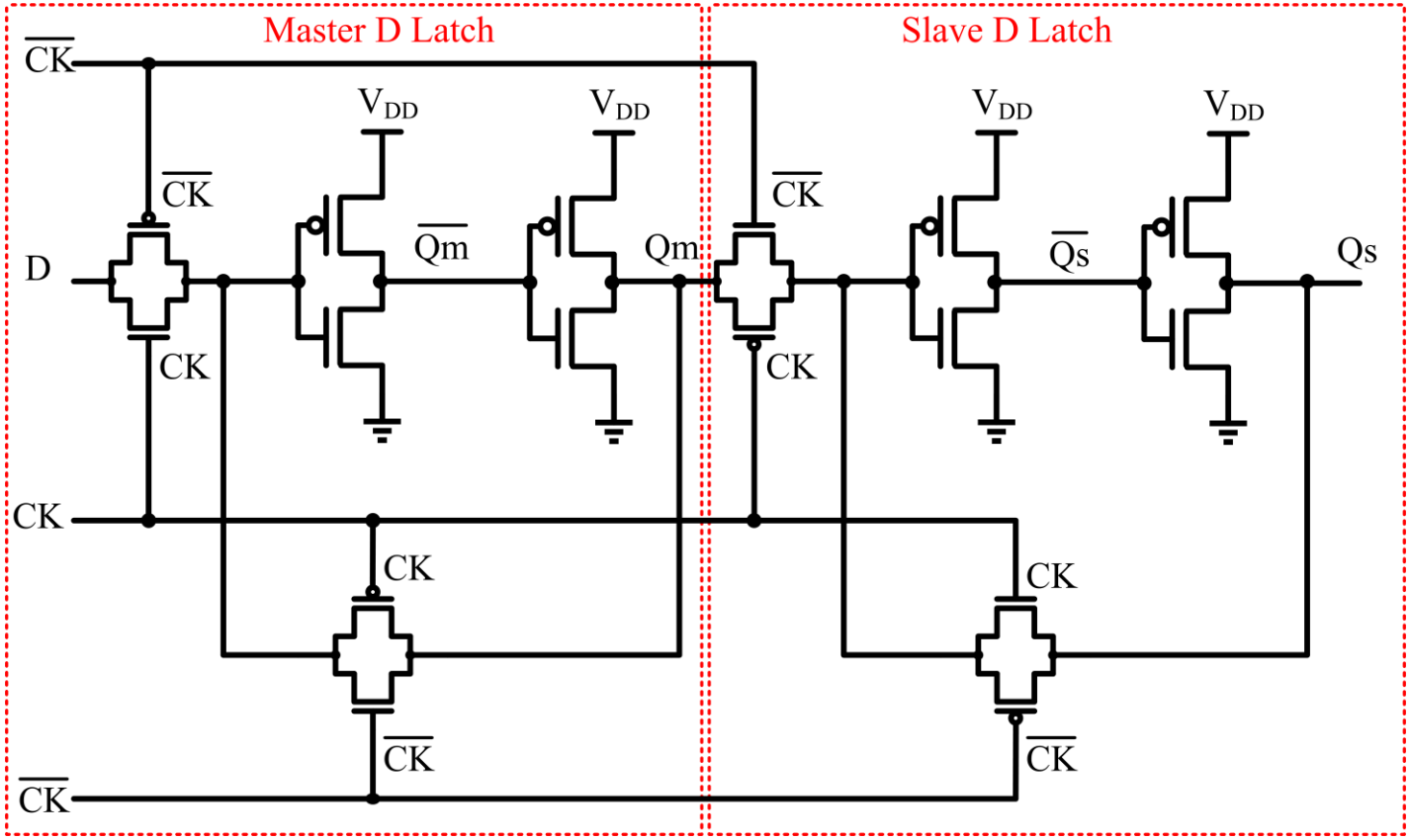
NAND Bistable DFF



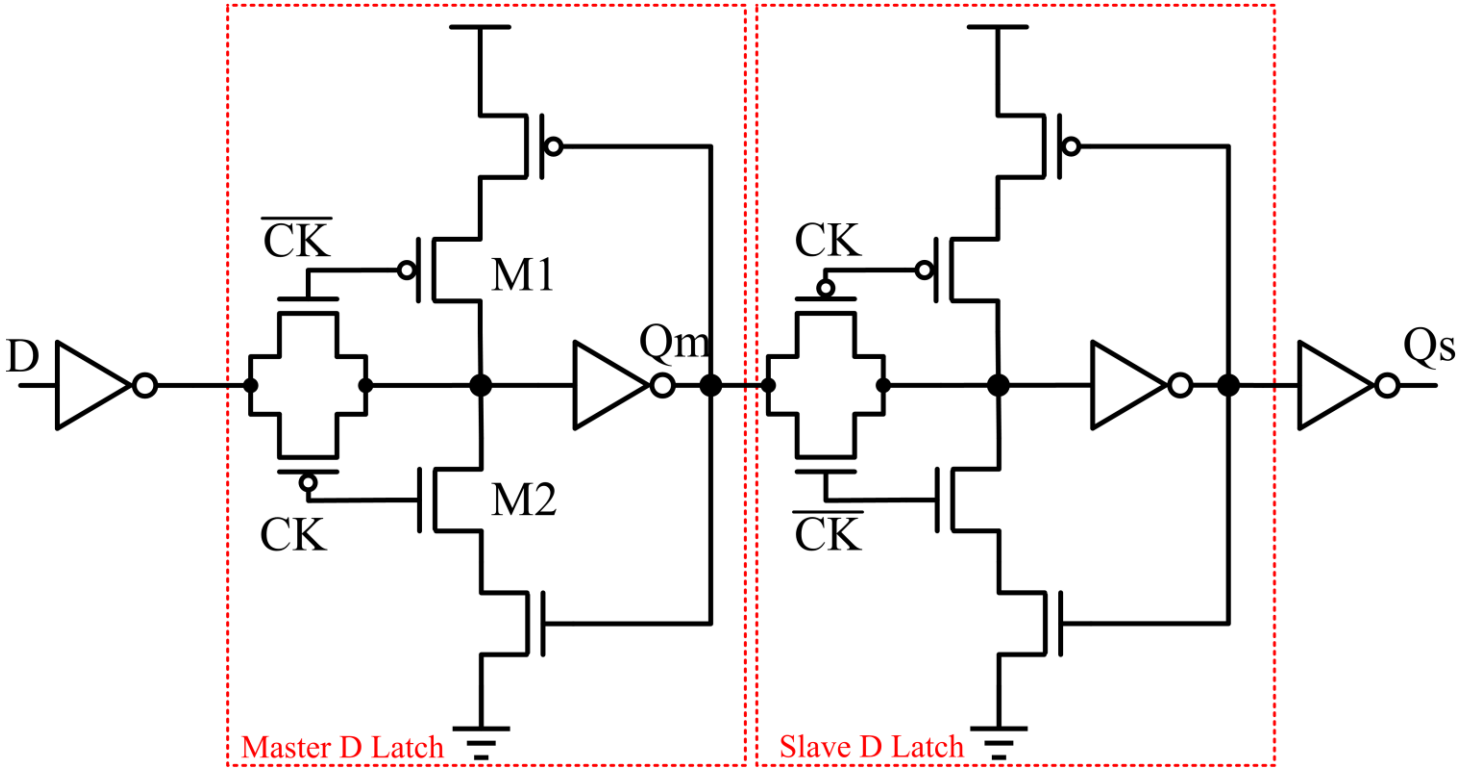
TG-based DFF 1



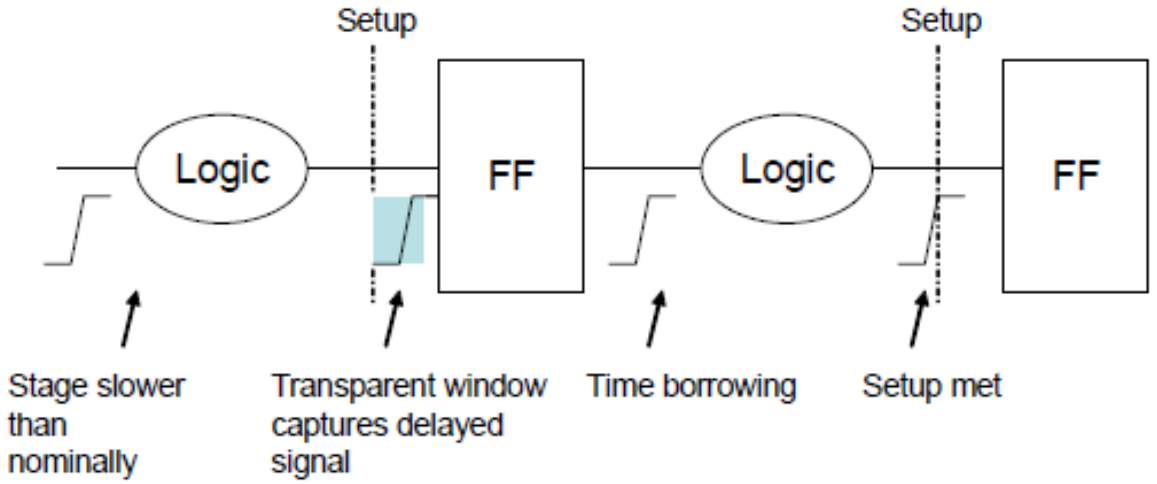
TG-based DFF 2



TG-based DFF 3 (Transmission Gate FF (TGFF)

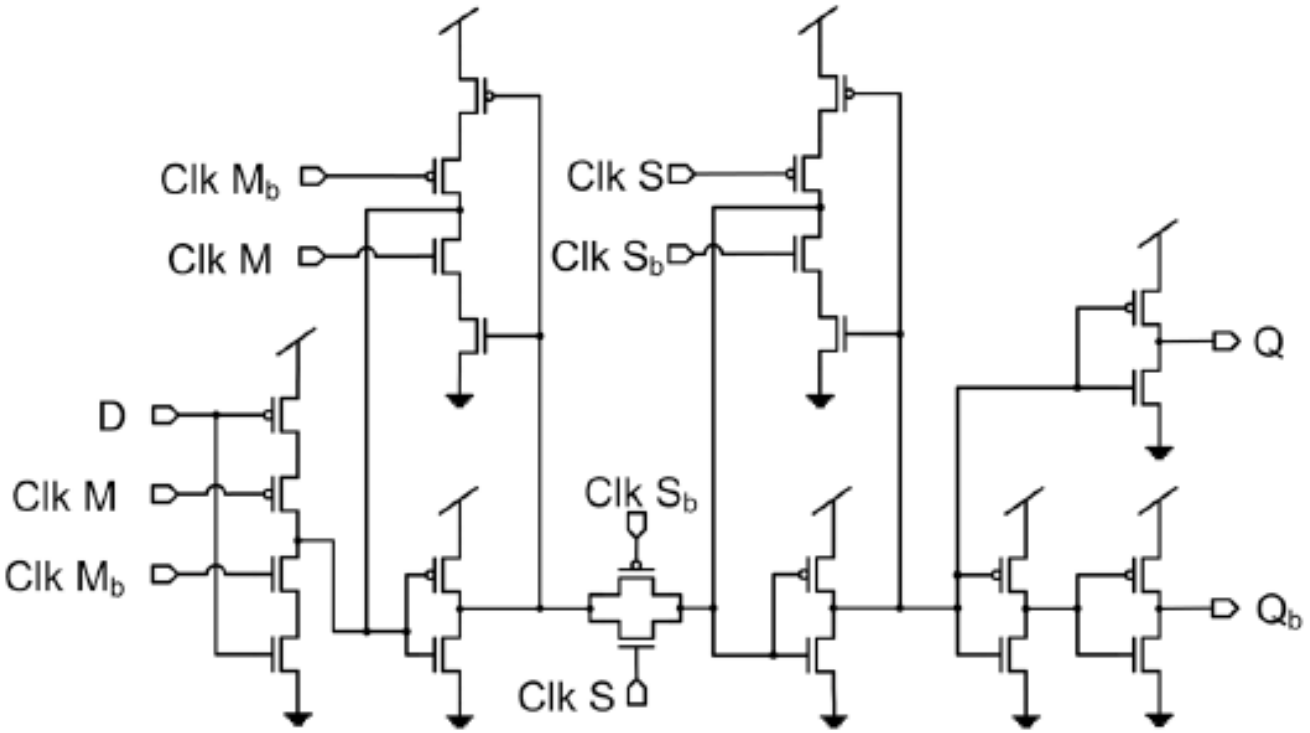


Soft-Edge Flip Flop



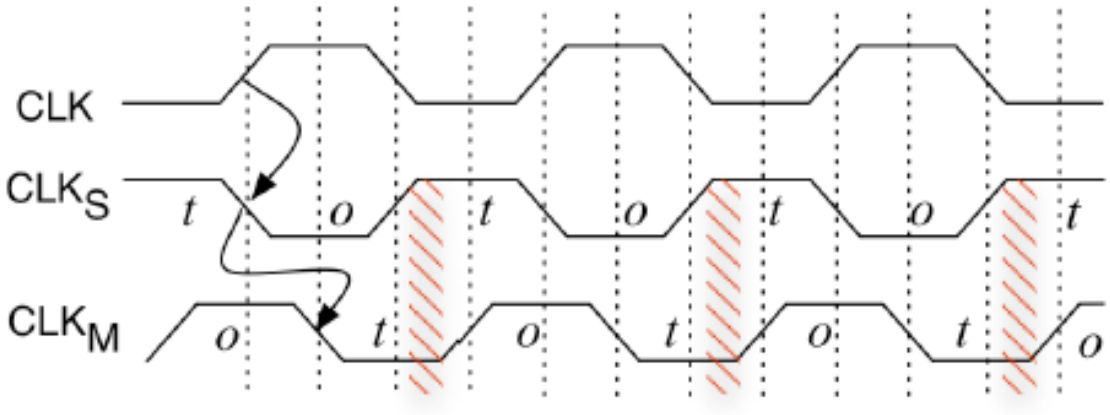
- Transparency window compensating for delay variation (Blaauw, et al.)

Soft-Edge Flip Flop (Cont.)

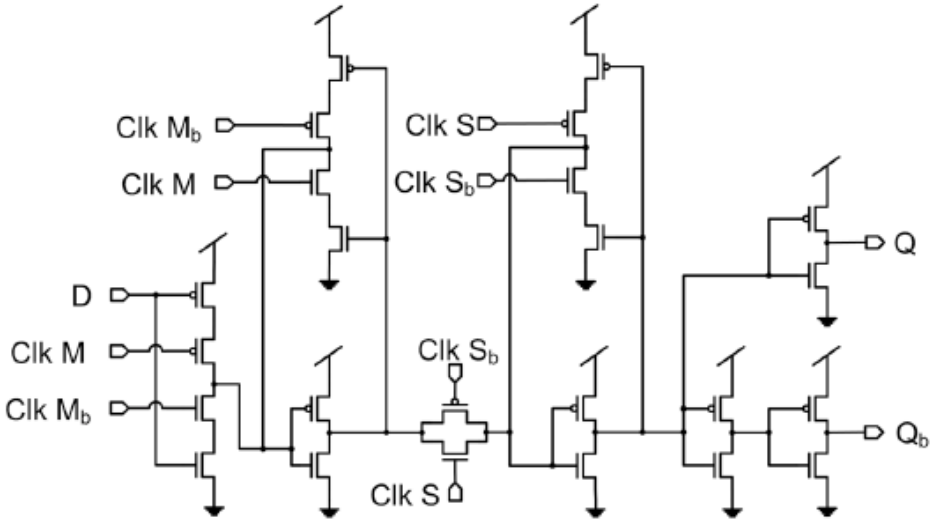


- **(Blaauw, et al.)**

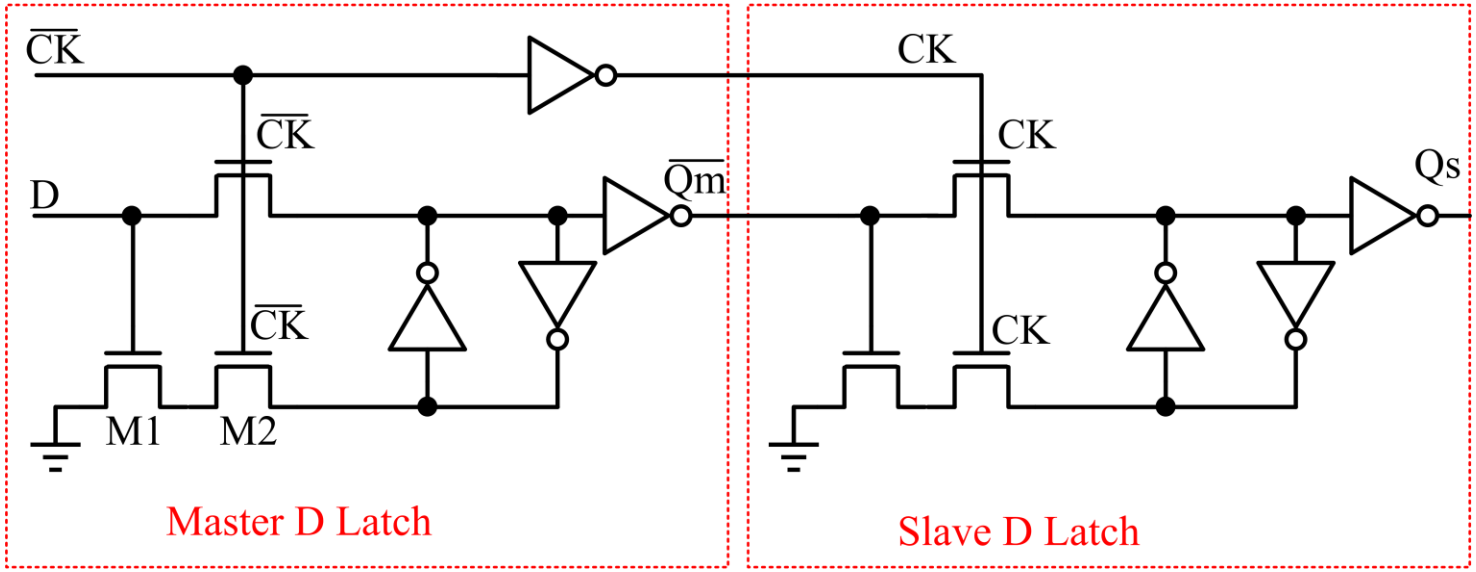
Soft-Edge Flip Flop (Cont.)



- Delaying the master clock (CLKM) relative to the slave clock (CLKS) creates a window of transparency (*t* = transparent, *o* = opaque) Blaauw, et al.

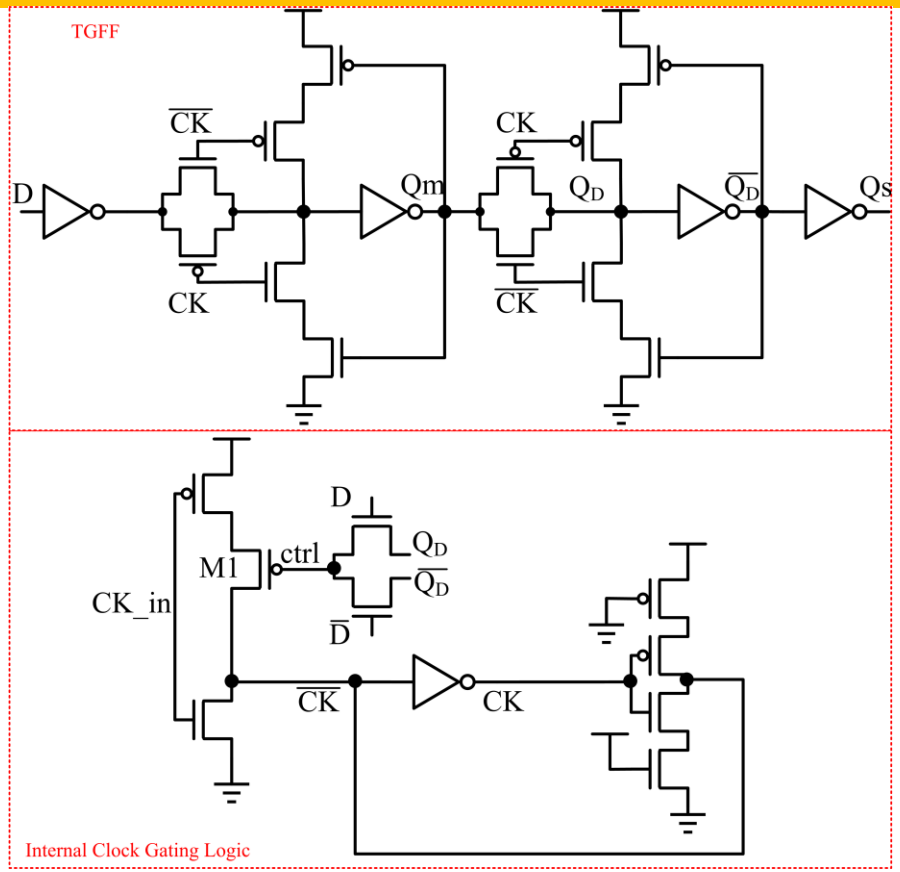


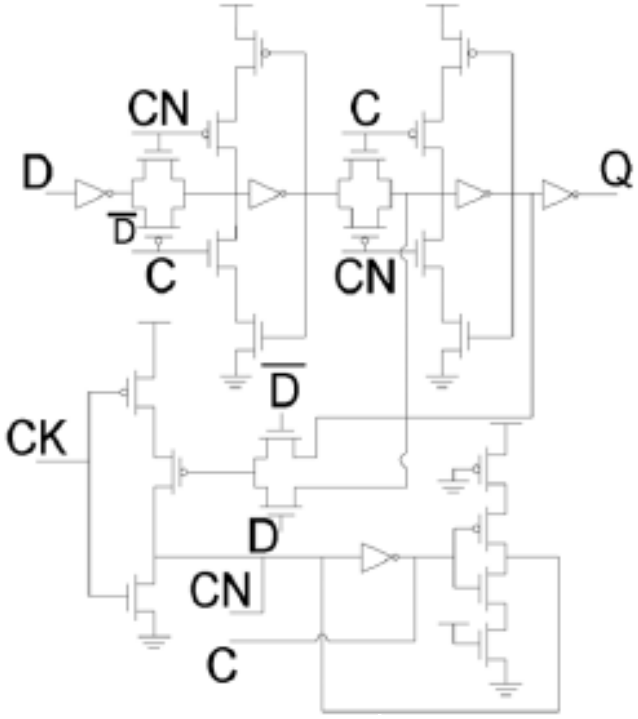
Write-Port Master-Slave FF (WPMS)



- WPMS trades off increased data power for reduced clock power
- The increased data power is because of the increased contention within the uninterrupted cross-coupled storage node inverters
- The reduced clock power is due to the reduction of the number of the transistors controlled by clock

Gated Master-Slave FF (GMSL)



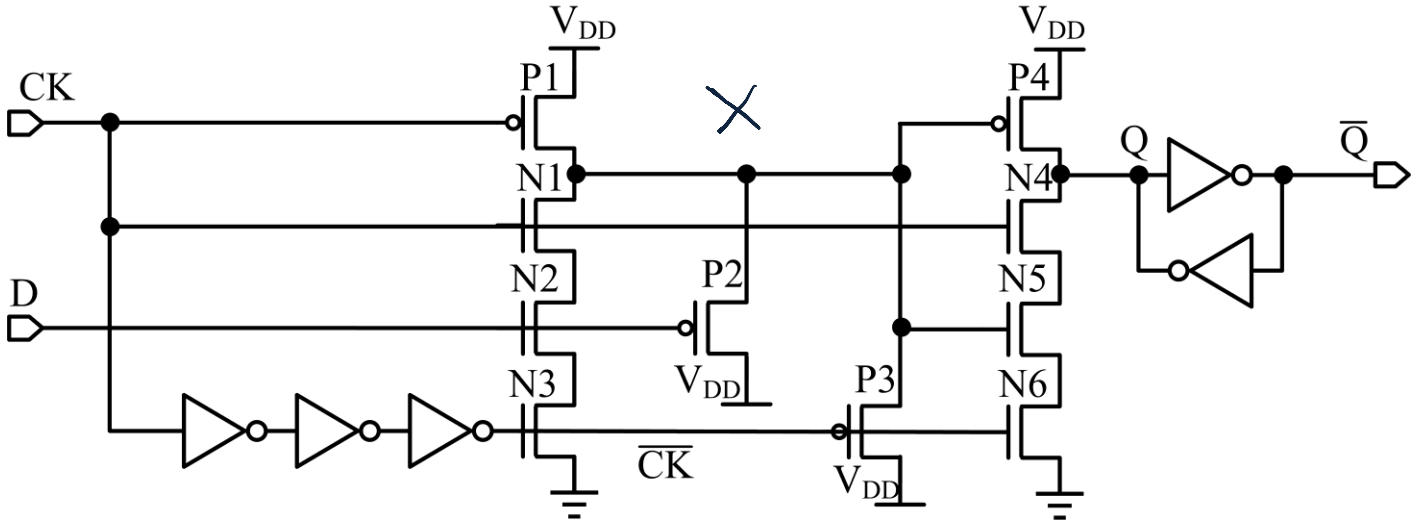


- If Q_D=1, D=1 or Q_D=0, D=0, i.e., data in the slave D latch matches the new input D, then ctrl=1 disabling the clock
- Add an internal clock gating logic to TGFF to save energy in the clocked nodes

Pulse-Triggered FF (P-FF)

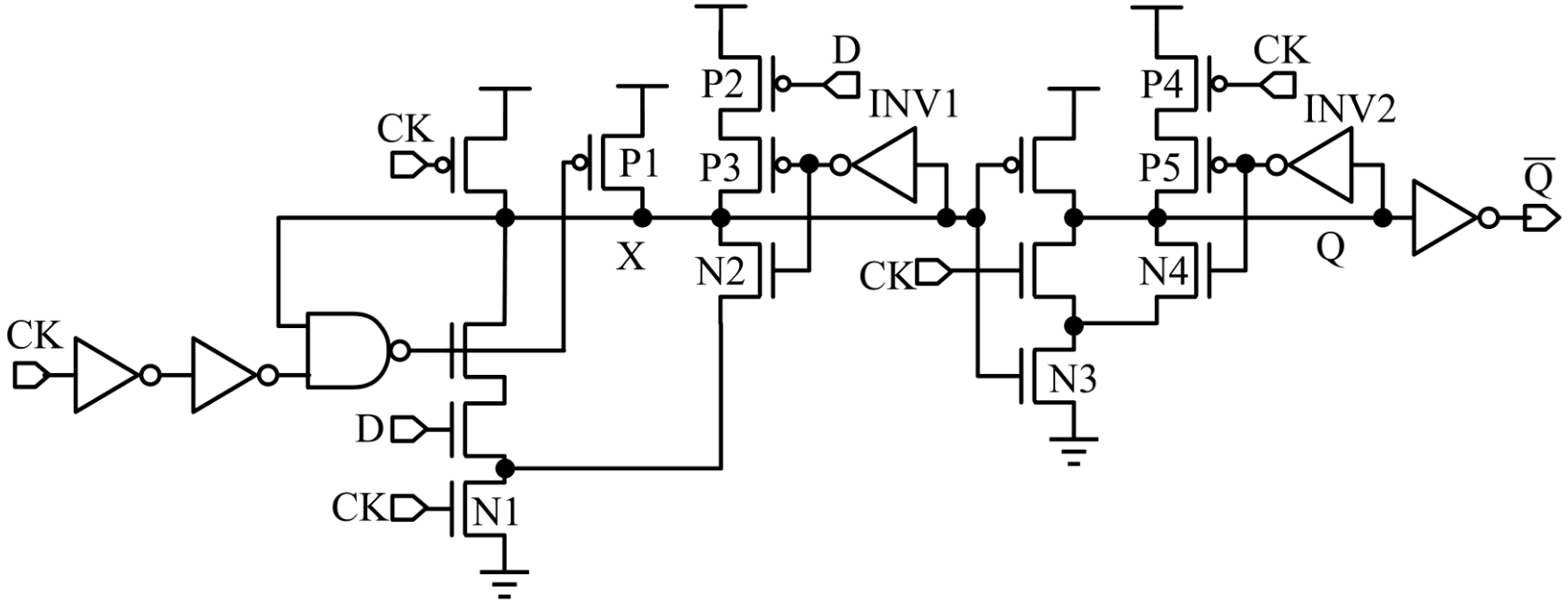
- A P-FF consists of a pulse generator for generating the strobe signals and usually ONE latch for storing data
- In implicit P-FFs, the pulse generator is in the latch design while an explicit P-FF needs separated pulse generator and latch
- Since there is only one latch, unlike master-slave FFs, P-FF is transparent only for a short time window during writing. This transparency window is generated by the pulse generator
- Compared with master-slave flip-flops, P-FFs have smaller area, shorter setup time and shorter D-Q delay (only one latch, so shorter D-Q path). P-FFs can use the semi-dynamic structure where the first stage is dynamic and the second is static

Hybrid Latch FF (HLFF)



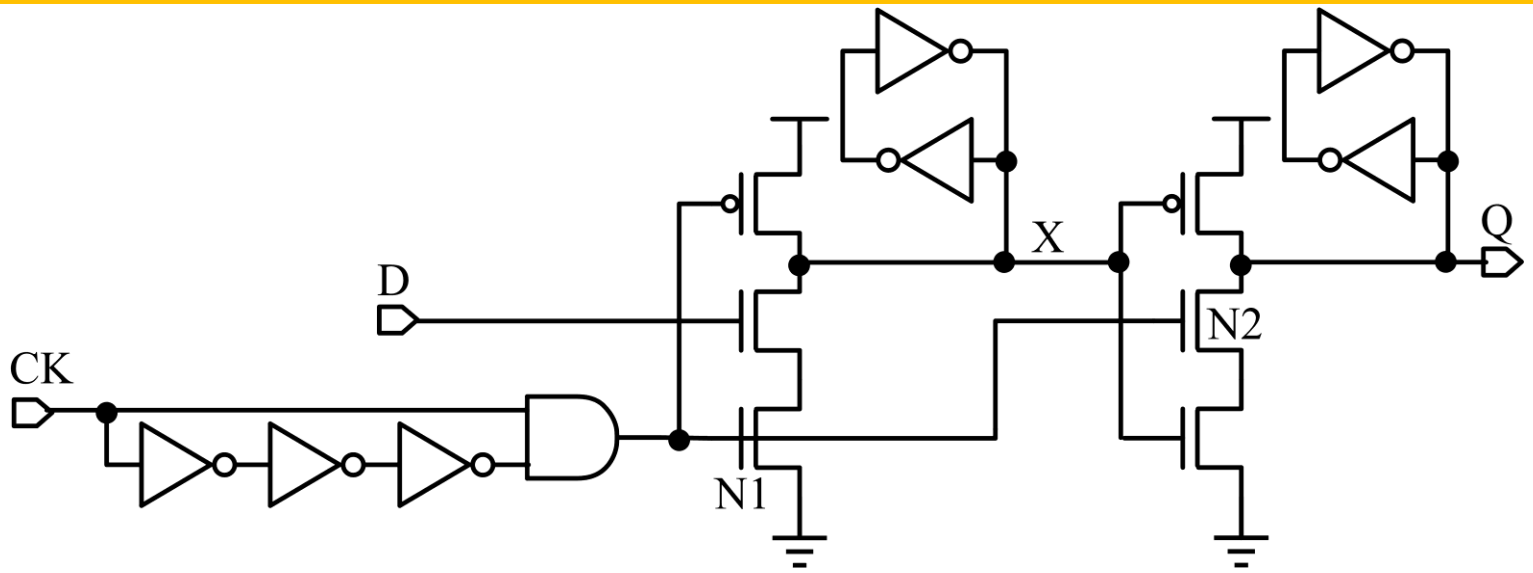
- Three inverters are used to generate a delayed inverted clock
- Before rising edge of clock: N1 N4 off, N3 N6 P1 ON, X pre-charged to VDD and Q holds previous value
- When rising edge of clock arrives: N1 N4 ON, N3 N6 is ON for a while. During this period, both "1" and "0" writing paths are transparent and the data D can be transmitted to node Q
- HLFF needs only 1 latch and is less sensitive to clock jitter. It trades off power for speed

UltraSPARC Semi-dynamic FF (USDFF)



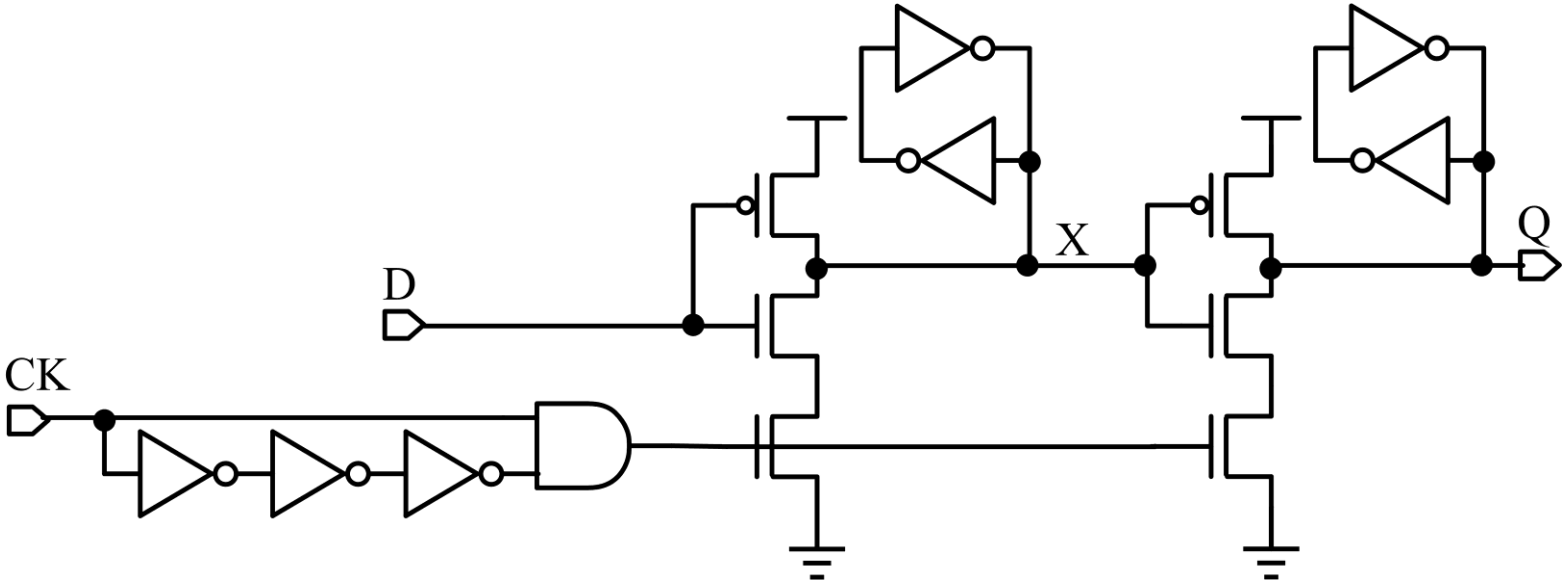
- USDFF is aimed to reduce the side effects from soft error hazards by increasing charge stored at sensitive nodes and increasing the current to restore the correct state
- When D and CK rise, P2-3 holds node X high. After three gate delays, P1 is enabled, holding X high even if D falls
- When D=1, N1-2 and INV1 form a latch that holds X low. N3-4, P4-5, and INV2 work as a clocked latch for storage node Q

Explicit-Pulsed FF (EPFF)



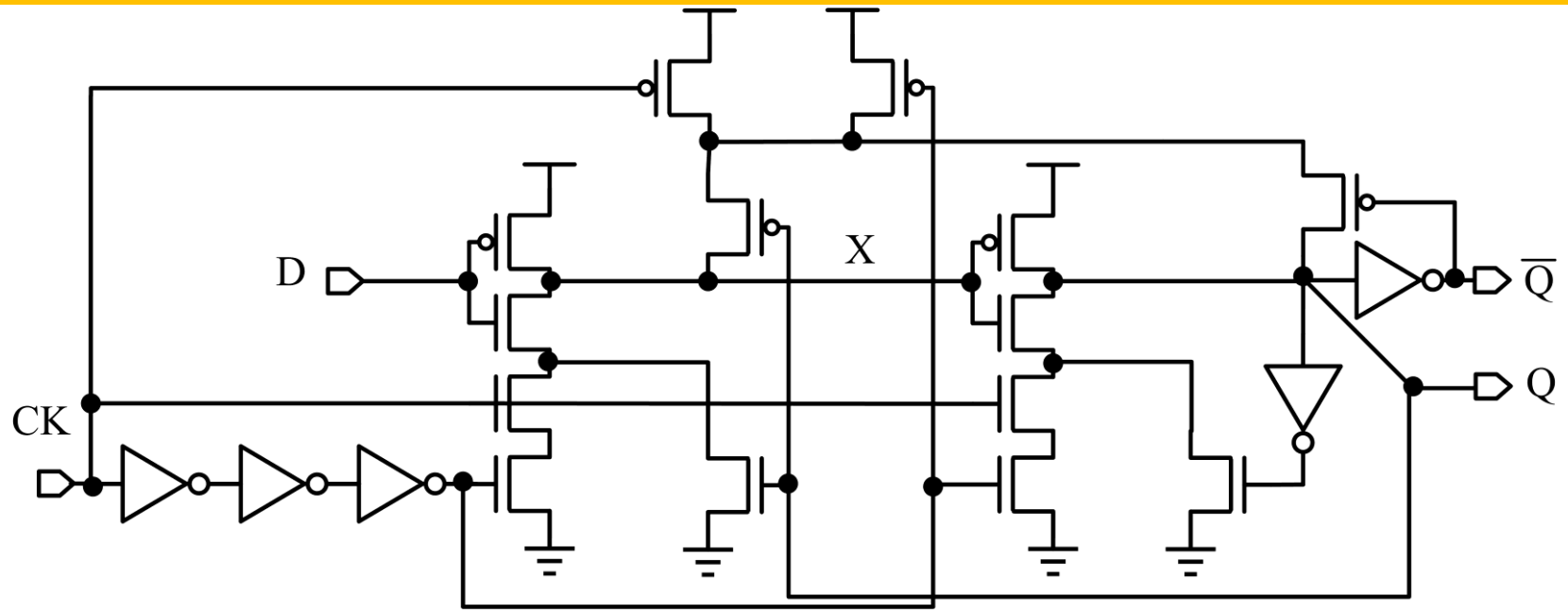
- The first stage is dynamic and the second stage is static. The back to back inverters are used as latches
- During precharge, CK=0 and X is precharged to 1
- When CK=1, EPFF is transparent for a short time (N1 and N2 are ON for a short time) and input D can be written into Q

Static Explicit-Pulsed FF (SEPFF)



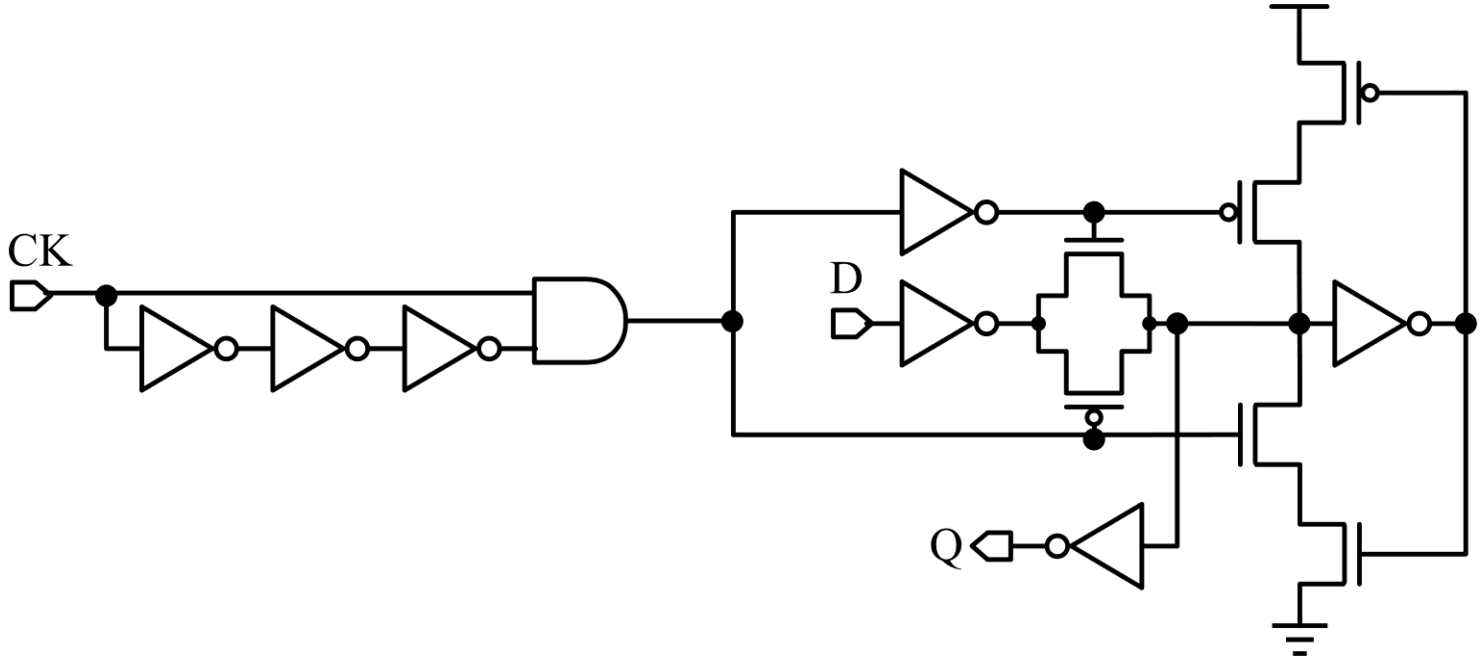
- In order to save power during precharge, change the EPFF into SEPFF by changing the first dynamic stage into static
- When the transparency window arrives, D can be written into the SEPFF. Otherwise, the latches hold the original data
- There is no precharge in SEPFF, hence, it results in less amount of power dissipation than in EPFF

Conditional Precharge FF (CPFF)



- The internal node precharge is conditional in CPFF
- Assume X is precharged to high when CK=0. The transparency window arrives when CK=1, and if D=1, X switches to 0 and Q=1
- If there is a consecutive D=1 cases, then as long as D=1 and Q=1, X remains 0 (not precharged to VDD). This is the so called conditional precharge technique

Transmission Gate Pulsed Latch (TGPL)

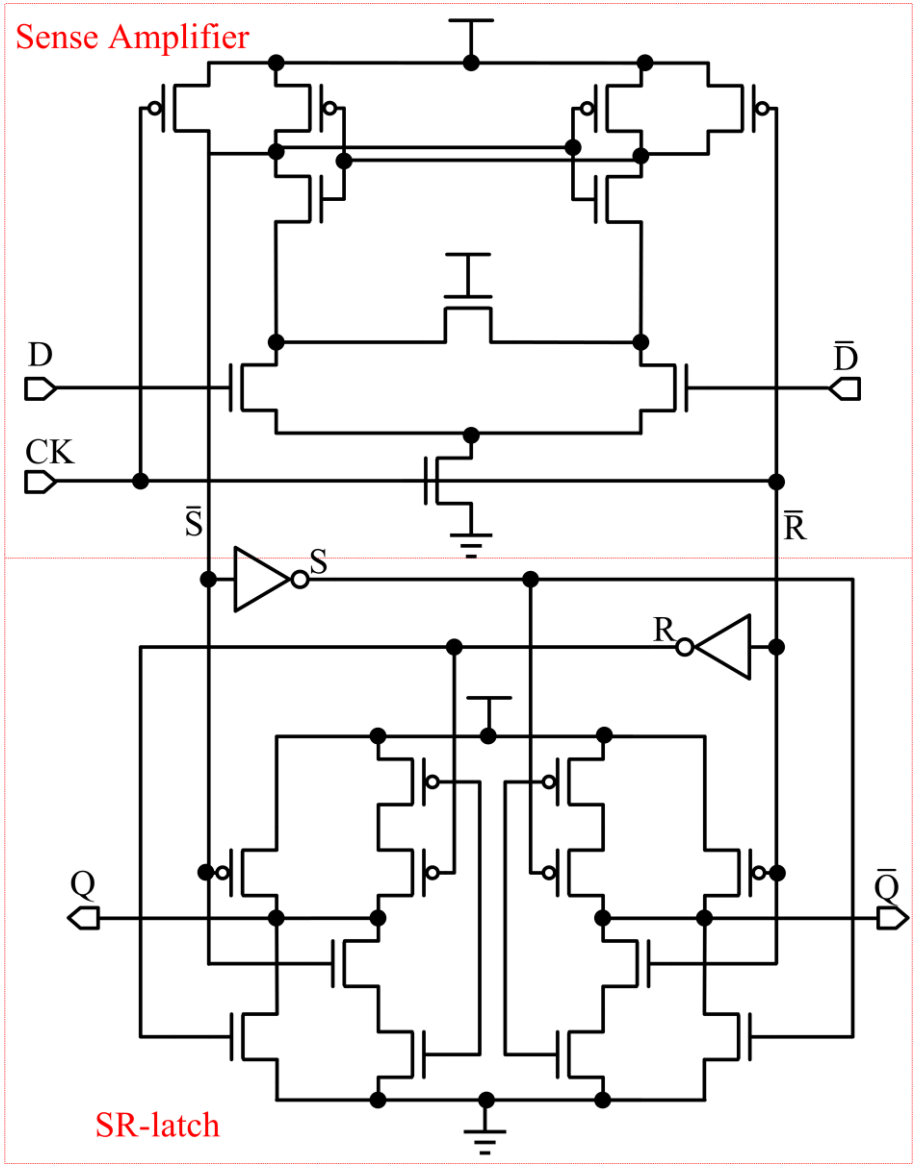


- During the transparency window, D is latched into the internal node
- After the transparency window, the latch holds the previous data

Differential FFs

- They use both input and complemented input and deliver output and complemented output
- A flip-flop consists of two blocks: a pulse generator (PG) and a slave latch (SL), similar to the MS latch combination consisting of master and slave latches
- The first stage (PG) is a function of the clock and data signals. Therefore, as a result of changes in clock and data values a pulse of a sufficient duration is produced. This pulse in turn sets the slave latch
- P-FFs have robustness and reliability issues because the delicate pulse generator is sensitive to process variations, noise and also the transition of the clock
- Differential FFs are designed to absorb clock slew using sense amplifier (SA)

Modified Sense-Amplifier FF (MSAFF)

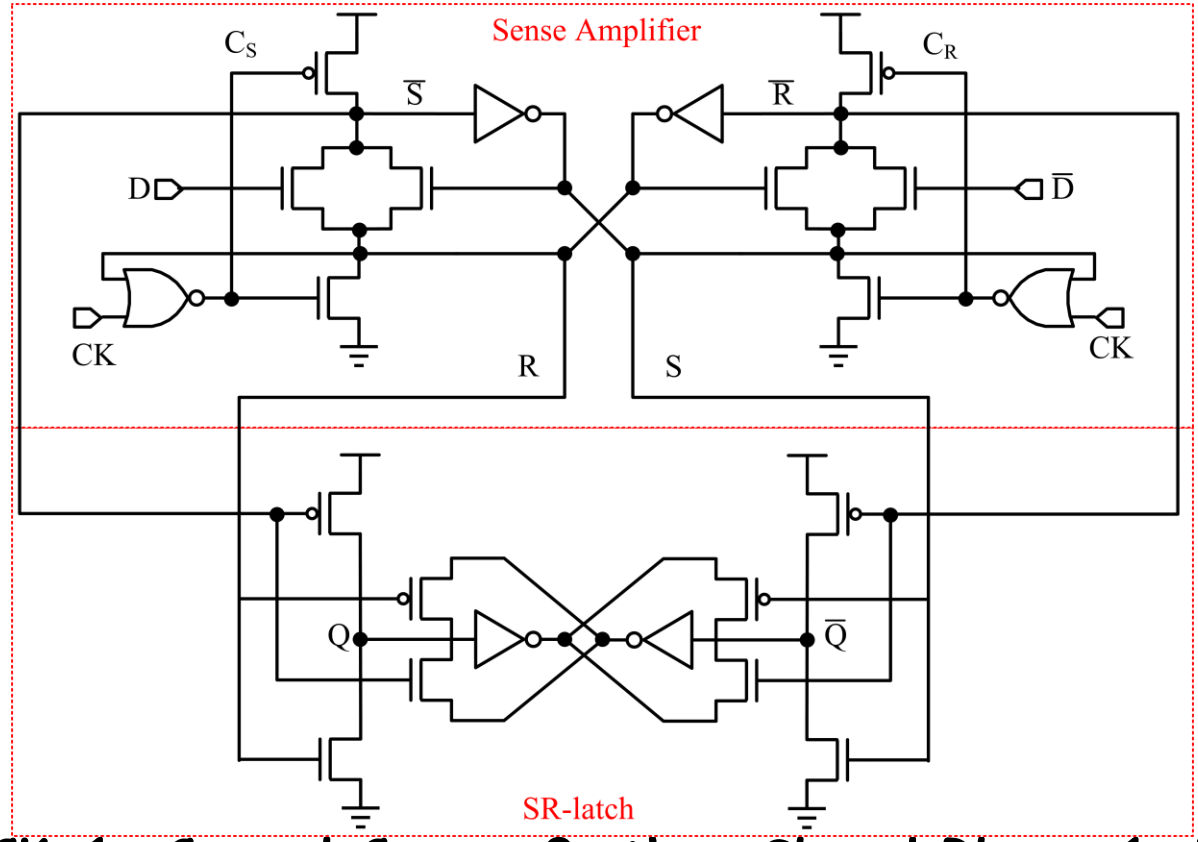


- MSAFF consists of an SA (as pulse generator) and an SR-latch
- The SR-latch is designed to overcome asymmetry of the back to back NAND based SR-latch

$Q = S + R'Q$

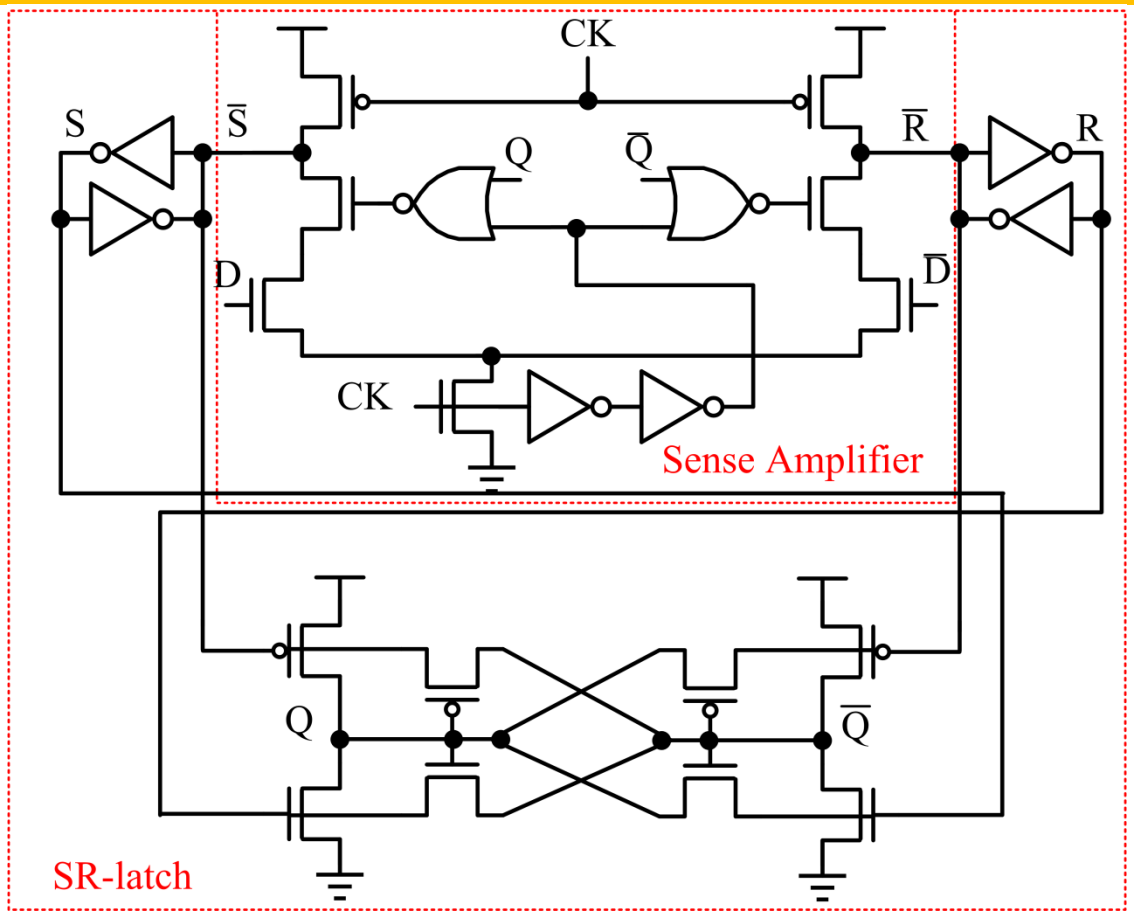
$Qbar = R + S'Q'$

Skew-Tolerant FF (STFF)



- When CK=1, Cs and C_R are 0, then S' and R' are 1. The SR-latch holds the previous data
- When CK=0, Cs and C_R are 1, and the sense amplifier functions similar as the reading circuit in SRAM
- STFF is designed to achieve high slew absorption

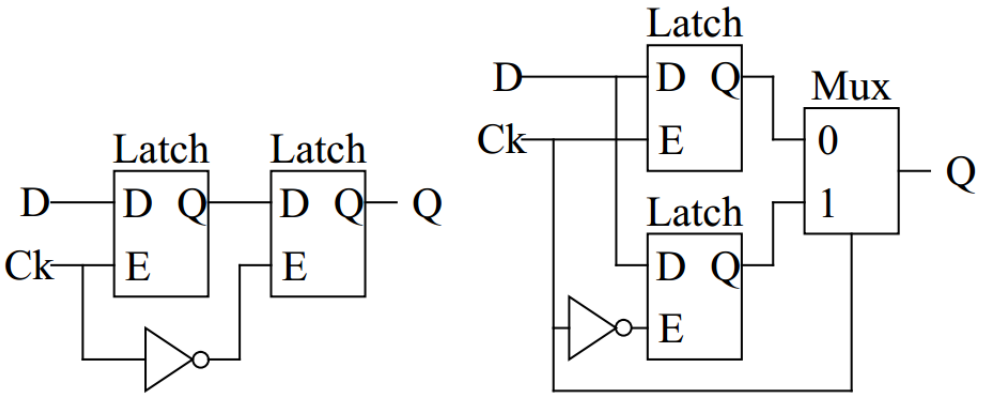
Conditional Capture FF (CCFF)



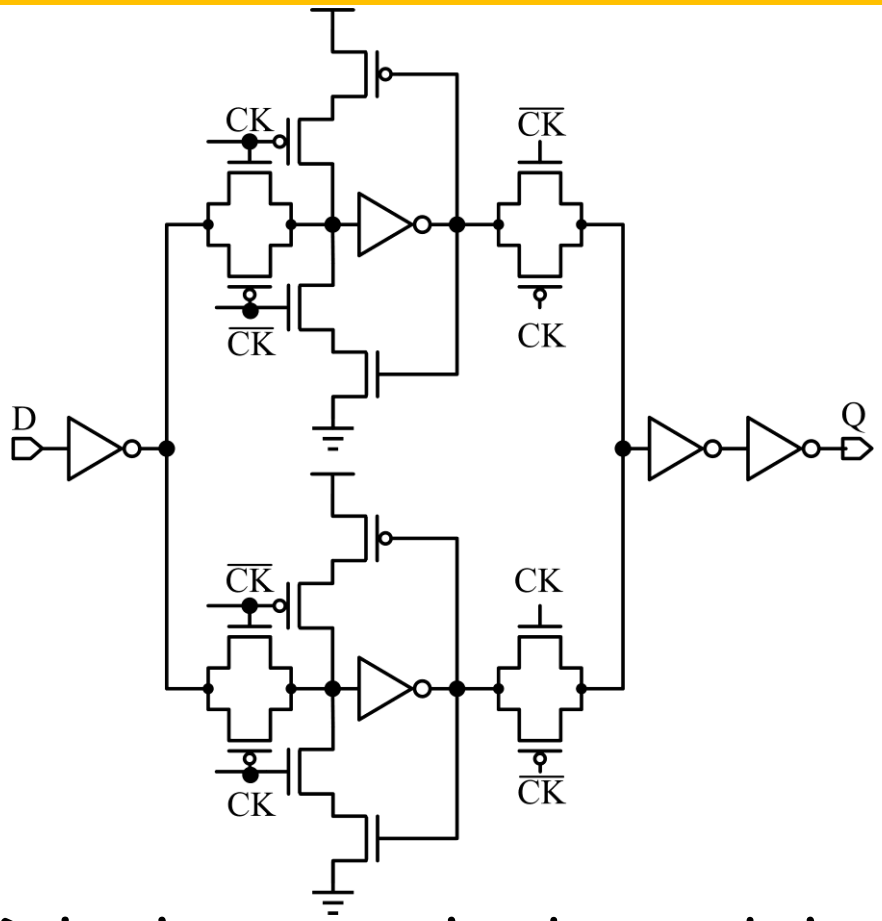
- CCFF is designed to achieve speeds comparable to the MSAFF, HLFF, etc. with power consumptions comparable to static designs like TGFF. CCFF reduces unnecessary internal switching activities with the control from Q and Q'

Double Edge Triggered (DET)

- A Single Edge Triggered (SET) flip-flop changes its output on one of the two clock edges. A DET flip-flop changes its output on both of clock edges
- SET has an idle clock edge with internal nodes switching (that should be added to the total power consumption). DET keeps both clock edges busy, and if we are given the same amount of data and same frequency, the SET needs twice the total time therefore more energy
- In conclusion, DET halves the clock frequency and saves energy

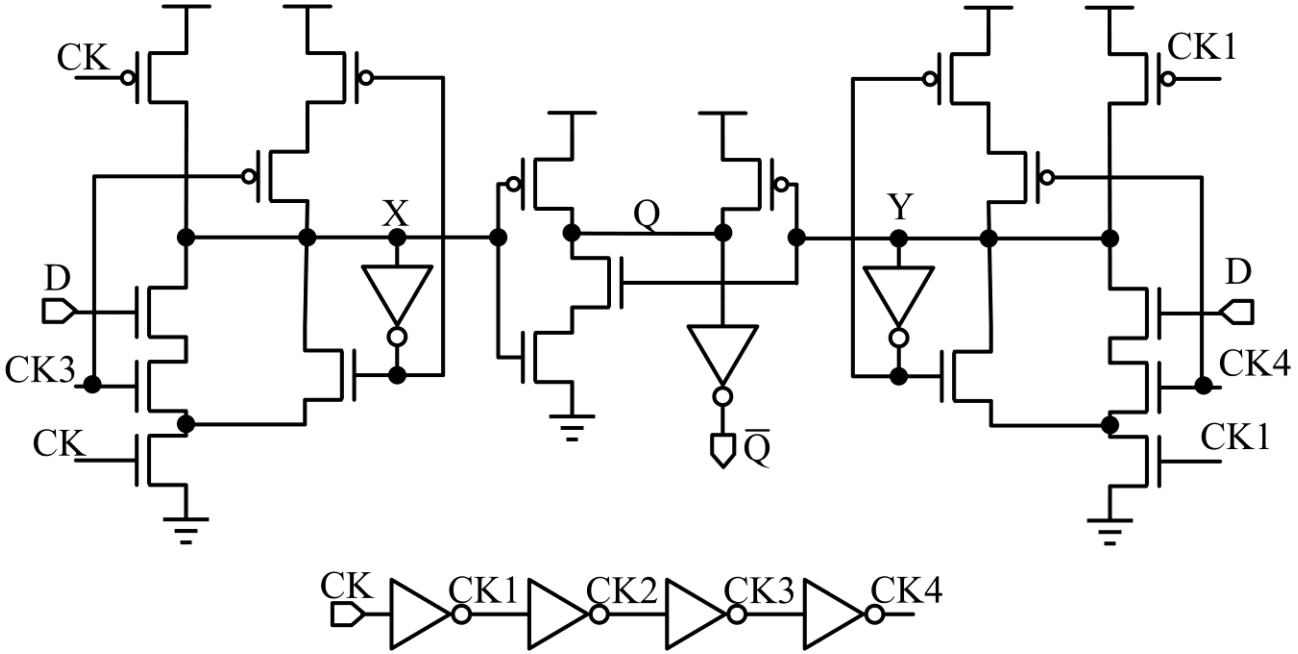


Transmission Gate Latch-Mux (DET-TGLM)



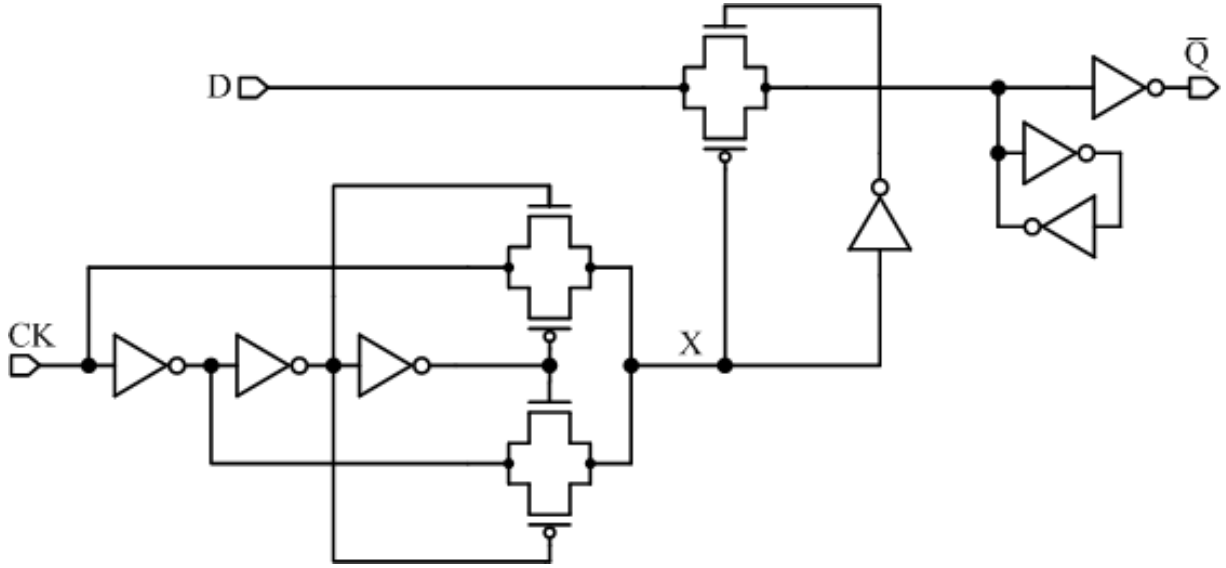
- CK=0, the top D latch outputs the data and the bottom one captures the input D. CK=1, the bottom D latch outputs the data and the top one captures the input D
- Hence, the DET-TLGM outputs data on both of clock edges

Symmetric Pulse Generator FF (DET-SPGFF)



- DET-SPGFF combines the idea of DET and P-FFs. The left stage is opposite to the right stage and the middle stage is the static output stage
- CK=0, X is precharged to high. When CK makes a low to high transition, the transparency window allows D to be written into X. In the rest of the clock cycle, X keeps the captured D value

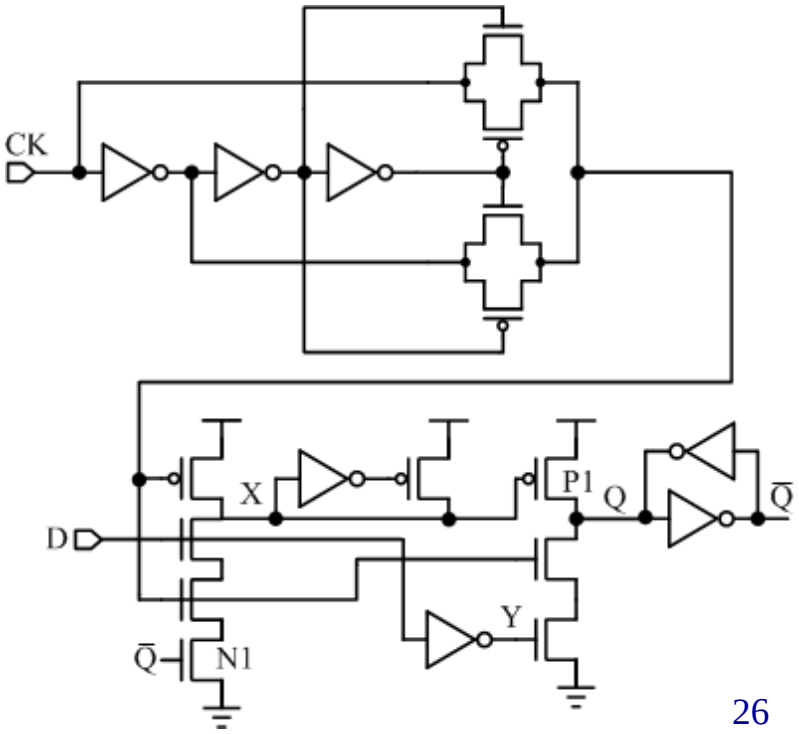
Static Pulsed Latch (DET-SPL)



- DET-SPL combines the ideas of DET and P-FFs. DET-SPGFF uses semi-dynamic structure and DET-SPL uses static logic
- The 3 inverters and 2 TGs after CK build the pulse generator part. During rising or falling of clock signal, there will be a temporary transparency window (X=0 in this window), hence D can be written into the latch
- After the clock is high or low, the window is closed (X=1). So the latch holds the previous D value

Conditional Discharge FF (DET-CDFF)

- The top part is the clock generator used in DET-SPL
- During the transparency window, if X has been precharged to V_{DD}, D=1 and Q=0, then Q'=1, N1 is ON, thus X is discharged, P1 is on and Q=1. If D=1 and Q=1, then Q'=0, N1 is OFF, no internal activity exists in this case and this is the idea of conditional discharge
- For the case D=0, then Y=1, Q will be discharged to ground through the previous PDN
- In this case, X holds the old value, thus no internal activity exists



Conclusion

- The clock system, composed of clock network interconnection and flip-flops, consumes around 30%-60% power in a VLSI chip. Therefore, reducing the power consumed by flip-flops will have a deep impact on the overall power consumption
- From a timing perspective, the delay of flip-flops accounts for a large portion of the clock cycle if the operating frequency is high. Therefore, developing fast flip-flops is well worth the efforts
- Process variation, soft error and noise in today's chips require high robustness and reliability of flip-flops
- Based on the requirement listed above, MSFF, P-FFs, SAFF and DET have different advantages and disadvantages, hence it's the designers' responsibility to figure out which is the best structure in our projects