University of Southern California

Viterbi School of Engineering

EE577A

VLSI System Design

Static Characteristics and Noise Margin

References: Syllabus textbooks, Professor Massoud Pedram's slides, online resources

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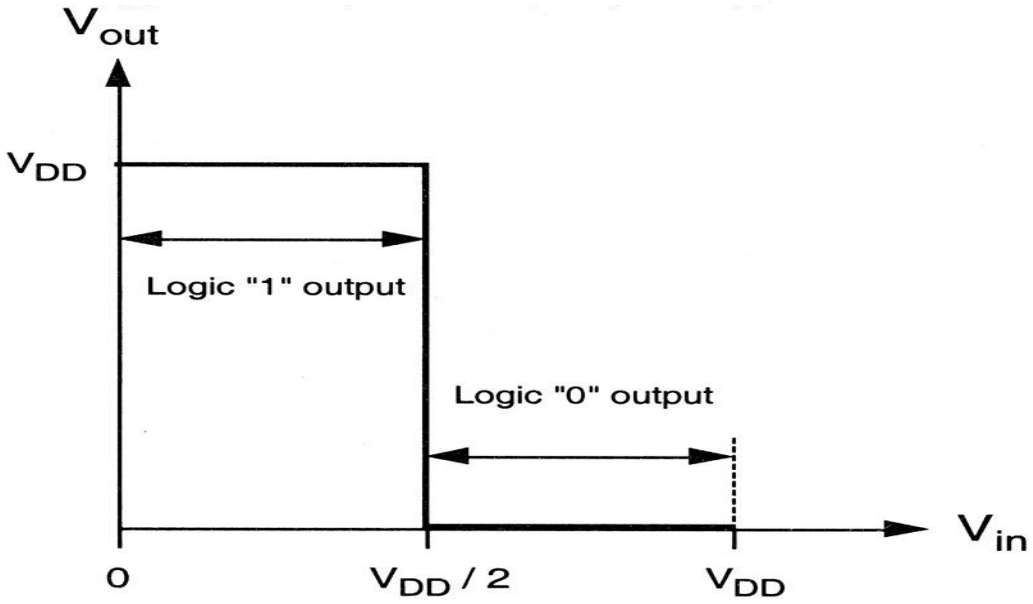
Ideal Inverter Threshold Voltage V_M

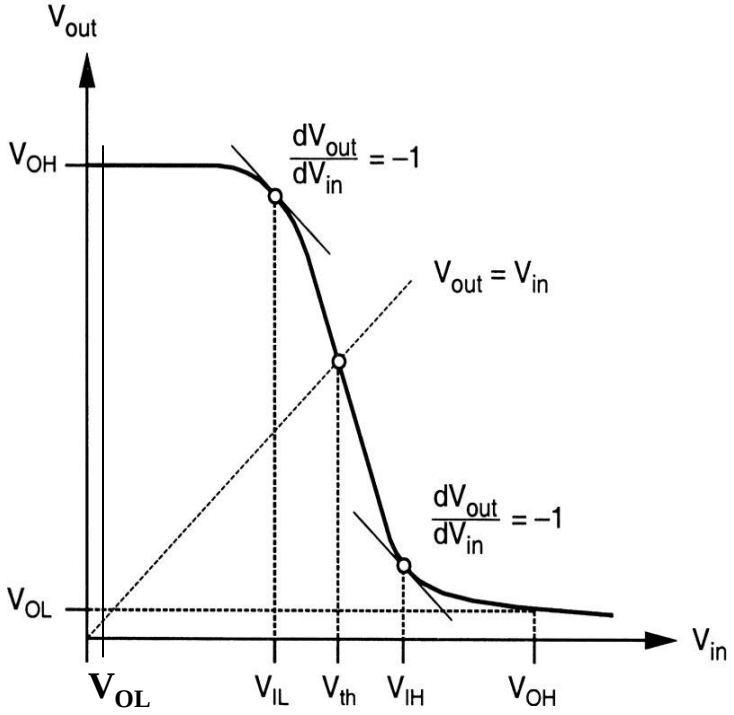
- For $0 \leq V_{in} < V_M = V_{DD}/2$ $V_{out} = V_{DD}$ (logic "1")
- For $V_M < V_{in} \leq V_{DD}$ $V_{out} = 0$ (logic "0")
- $0 \leq V_{in} < V_M$ input is interpreted as a logic "0"
- $V_M < V_{in} \leq V_{DD}$ input is interpreted as a logic "1"



VTC

- There are two critical voltage points for which:

  $dV_{out}/dV_{in} = -1$
- V_{OH}: Max output voltage when output level is logic "1"
- V_{OL}: Min output voltage when output is level logic "0"
  - $V_{OH} = f(V_{OL}) = V_{OL}'$
  - $V_{OL} = f(V_{OH}) = V_{OH}'$
- V_{IL}: Maximum input voltage which can be interpreted as logic "0"
- V_{IH}: Minimum input voltage which can be interpreted as logic "1"
- Inverter threshold voltage (V_M): defined as the point where $V_{in}=V_{out}$ (transition voltage)



Noise Margin (NM)

- Noise Margin for low signal levels: $NM_L = V_{IL} - V_{OL}$
- Noise Margin for high signal levels: $NM_H = V_{OH} - V_{IH}$

- *A narrow transition (or uncertain) region would allow larger noise margins, therefore reducing the width of the uncertain region is (desirable and) an important design objective*

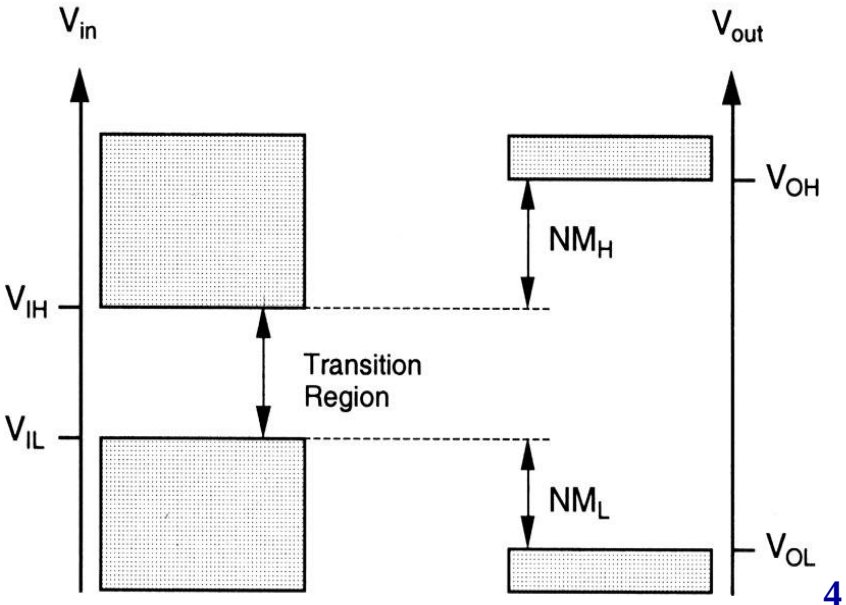
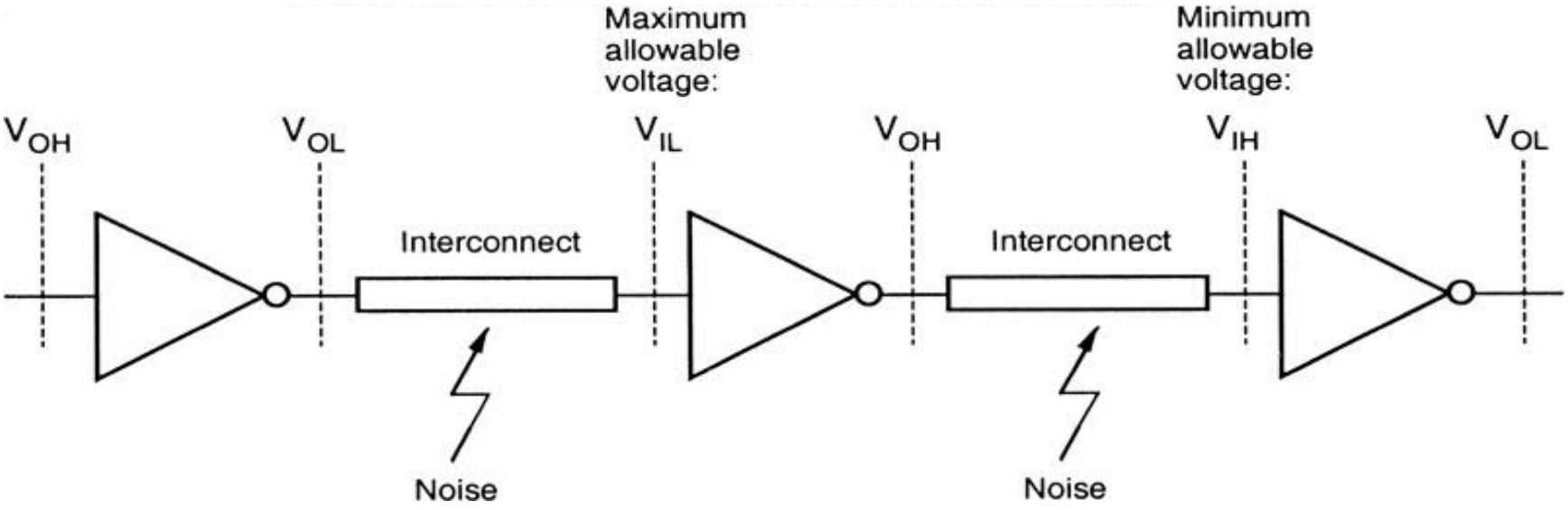
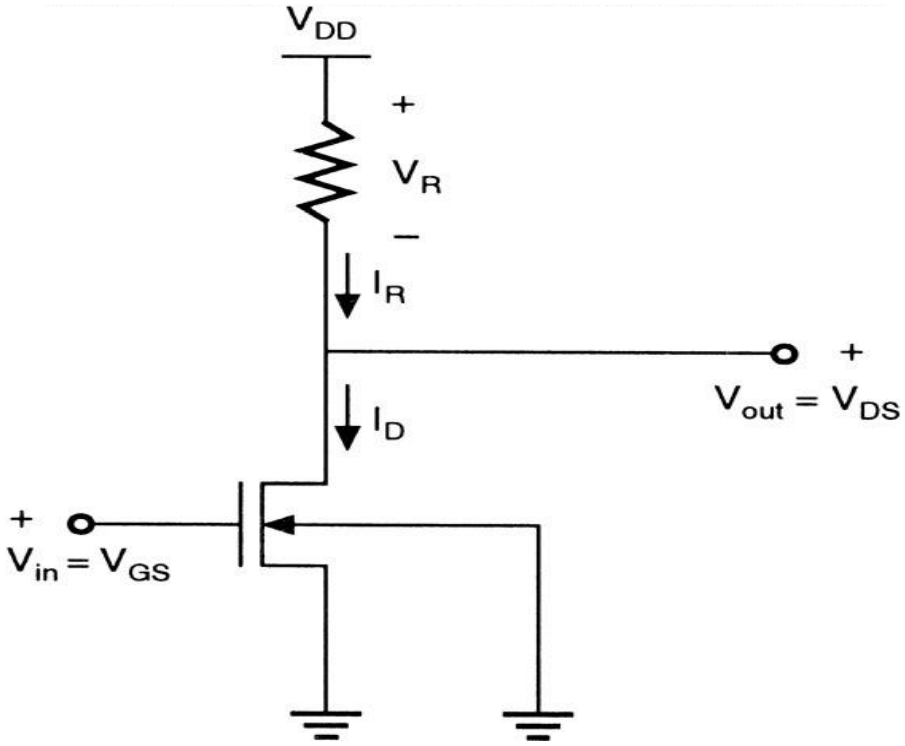


Illustration of noise margins

Noise Immunity

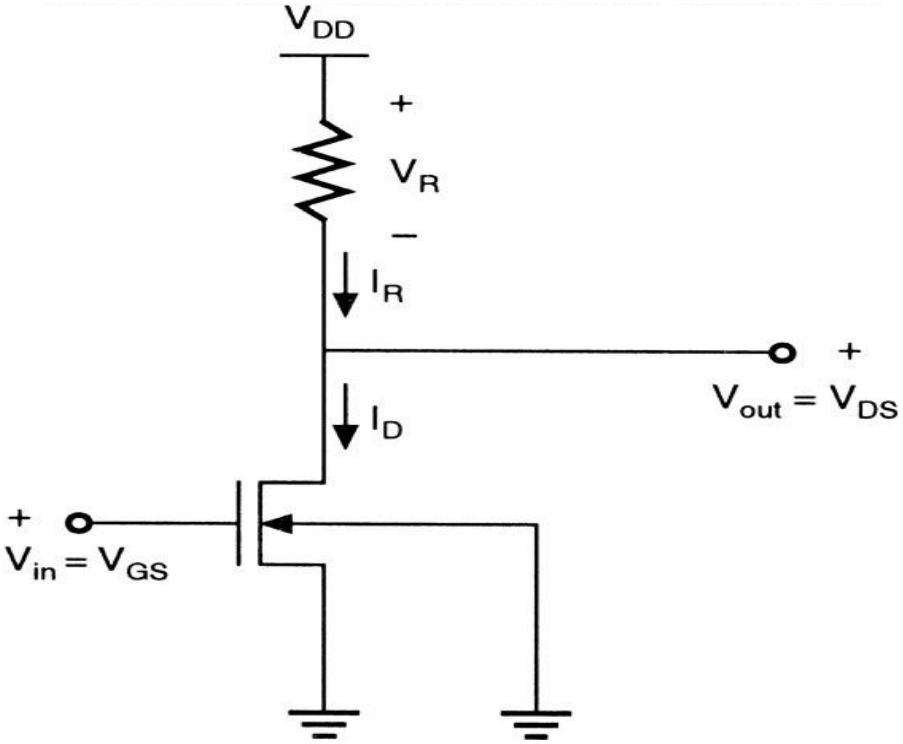


Resistive-Load nMOS Inverter



Calculation of V_{OH}

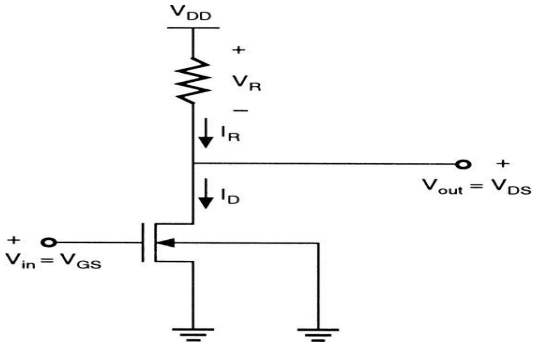
- $V_{out} = V_{DD} - R_L.I_R$
- When $V_{in} < V_{T0}$
  - transistor is in cut off
  - $I_R = I_D = 0$
  - $V_{OH} = V_{DD}$



Calculation of V_{OL}

- Assume $V_{in} = V_{OH} = V_{DD} \Rightarrow V_{in} - V_{T0} > V_{out} \Rightarrow$ Linear region
- $I_R = (V_{DD} - V_{out})/R_L$
- Using KCL for output node $\Rightarrow I_R = I_D$

$$(V_{DD} - V_{OL})/R_L = (k_n/2) \cdot [2.(V_{DD} - V_{T0}).V_{OL} - V^2_{OL}]$$



- V_{OL} can be numerically calculated from above
- Alternatively the above equation can be solved for V_{OL} which results in :

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{(V_{DD} - V_{T0} + \frac{1}{k_n R_L})^2 - \frac{2V_{DD}}{k_n R_L}}$$

- Note: Instead of memorizing the noise margin related equations, one can use the definitions (e.g. here for V_{OL}) and write a KCL based on the transistor mode (e.g., here it is linear)

Calculation of V_{IL}

- $dV_{out}/dV_{in} = -1$ at $V_{in} = V_{IL}$
- $V_{out} > V_{in}-V_{TO} \Rightarrow$ the transistor operates in saturation region
- KCL for the output node:

$$(V_{DD}-V_{out})/R_L = (k_n/2).(V_{in}-V_{TO})^2 \qquad (1)$$

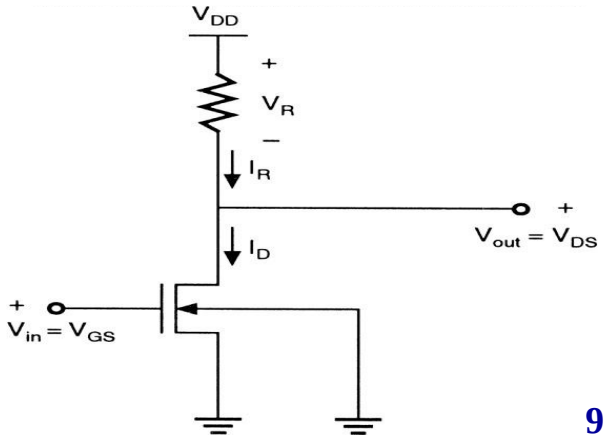
- Differentiate both sides $(-1/R_L).(dV_{out}/dV_{in}) = k_n.(V_{in}-V_{TO})$
- Substitute $dV_{out}/dV_{in}=-1$

$$(-1/R_L).(-1)=k_n.(V_{IL}-V_{TO})$$

$$V_{IL} = V_{TO} + 1/(k_nR_L) \qquad (2)$$

- By substituting (2) into (1)

$$V_{out}(V_{in}=V_{IL}) = V_{DD}-(k_nR_L/2).(V_{TO}+1/k_nR_L-V_{TO})^2$$
$$= V_{DD}-1/(2k_nR_L)$$



Calculation of V_{IH}

- V_{IH} is the larger of the two points at which slope is equal to -1
- When $V_{in} = V_{IH}$, V_{out} is slightly larger than $V_{OL} \Rightarrow V_{out} < V_{in}-V_{TO}$

  $\Rightarrow$ Linear mode, therefore KCL for the output node:

$$(V_{DD}-V_{out})/R_L = (k_n/2).[2.(V_{in}-V_{TO}).V_{out}-V^2_{out}] \quad (3)$$

- Differentiate both sides wrt V_{in}

$$-(1/R_L).dV_{out}/dV_{in} = k_n/2.[2.(V_{in}-V_{TO}).dV_{out}/dV_{in}+2V_{out}-2V_{out}.dV_{out}/dV_{in}]$$

By substituting $dV_{out}/dV_{in} = -1$ at $V_{in} = V_{IH}$

$$(-1/R_L).(-1) = k_n.[(V_{IH}-V_{TO}).(-1)+2V_{out}]$$

$$V_{IH} = V_{TO} + 2V_{out} - 1/k_nR_L \quad (4)$$

By substituting (4) into (3) :

$$(V_{DD}-V_{out})/R_L = (k_n/2).[2.(V_{TO}+2V_{out}-1/k_nR_L-V_{TO}).V_{out}-V_{out}^2]$$

Positive solution:

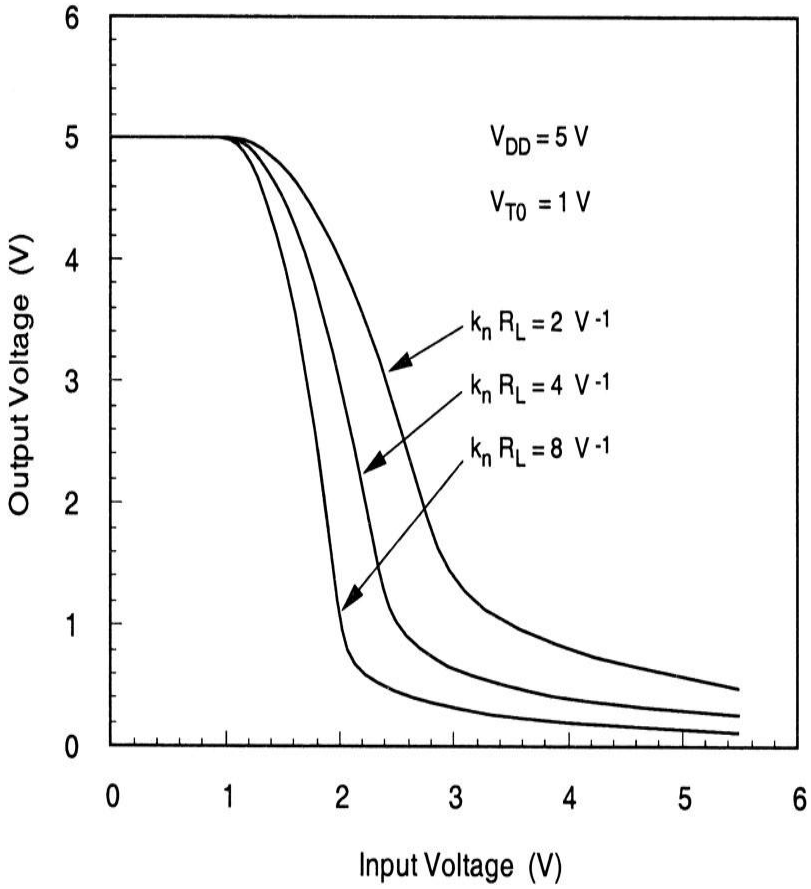
$$V_{out}(V_{in}=V_{IH}) = [(2/3).V_{DD}/k_nR_L\ ]^{1/2} \quad (5)$$

Substitute (5) into (4):

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3}\cdot\frac{V_{DD}}{k_nR_L}} - \frac{1}{k_nR_L}$$

Calculation of V_{IH} (Cont.)

- k_nR_L plays an important role in determining the shape of the VTC
- V_{OH} is determined primarily by V_{DD}
- Adjustment of V_{OL} receives primary attention
- V_{IL} & V_{IH} are usually treated as secondary design variables
- For larger k_nR_L values, V_{OL} becomes smaller and shape of the VTC approaches that of the ideal inverter



VTC of the resistive-load inverter for different values of k_nR_L

Power Consumption and Gate Area

- DC power consumption of the resistive-load inverter circuit is found by considering two cases:
  1. $V_{in} = V_{OL}$ (low) $\Rightarrow$ transistor is in cut-off $\Rightarrow I_D = I_R = 0$ $\Rightarrow P_{DC} = 0$
  2. $V_{in} = V_{OH}$ (high) $\Rightarrow$ transistor is in linear region and $V_{out} = V_{OL}$

$$I_D = I_R = (V_{DD} - V_{OL})/R_L$$

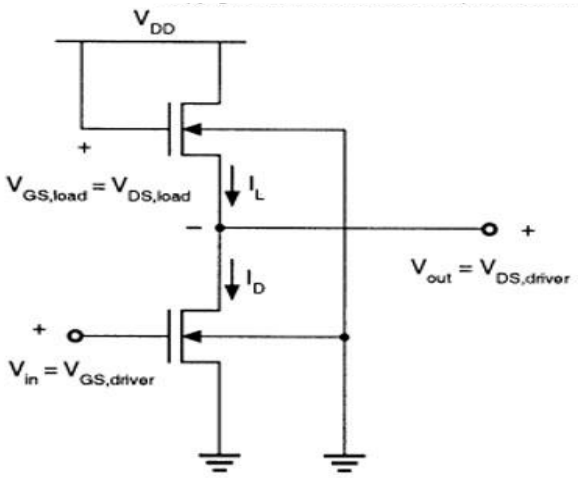
- Assuming Voltage is "low" 50% of time and "high" 50% of time

$$P_{DC}(\text{average}) = (V_{DD}/2).(V_{DD} - V_{OL})/R_L$$

- The gate area depends on two parameters
  1. (W/L) ratio of the driver transistor. It can be approximated by the gate area (W x L)
  2. R_L value. Resistor area depends on fabrication technology

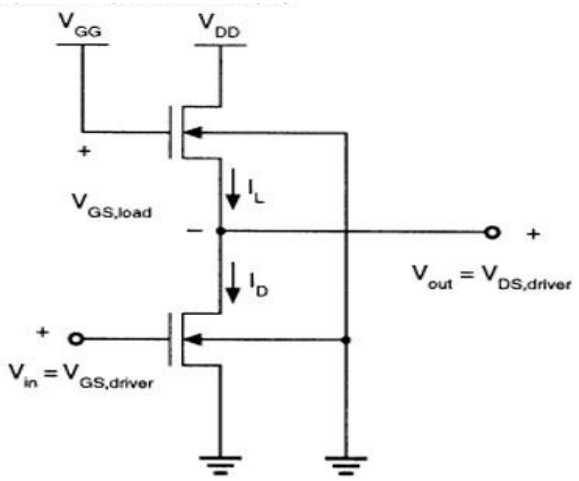
Inverters with n-Type MOSFET Load

- Resistive-load inverter circuit is not suitable in most VLSI circuit designs because of large area occupied by the load resistor
- Use nMOS as the active resistor load
  - Advantages: smaller area and better performance



(a)

Inverter with saturated enhancement-type NMOS load

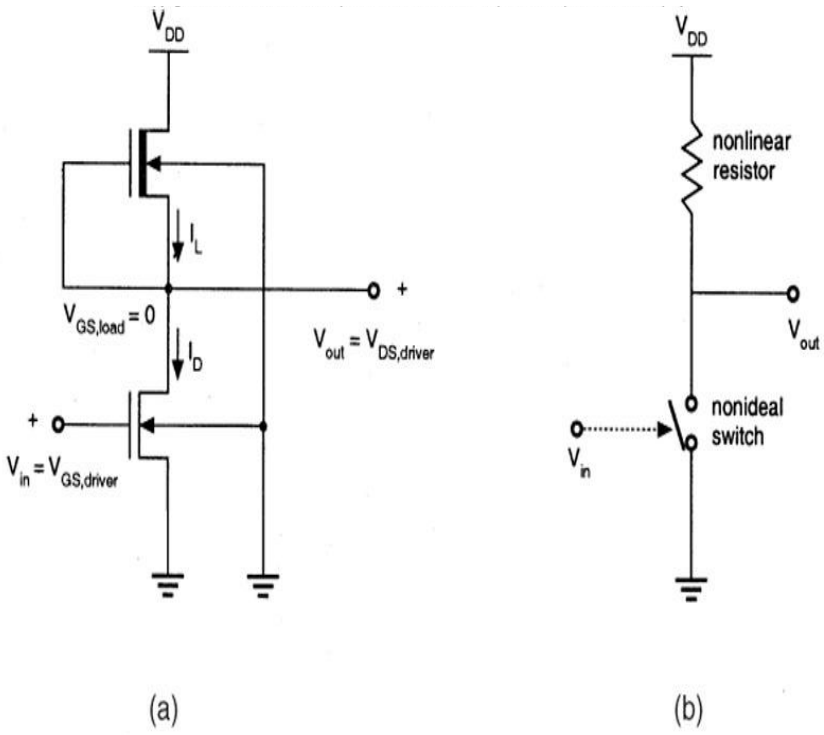


(b)

Inverter with linear enhancement-type NMOS load

Depletion-Load nMOS Inverter

- Advantages:
  - Sharp VTC transition and better noise margins
  - Single power supply
  - Smaller overall layout
- Downside: fabrication process is more complicated. DC power consumption
- Driver device: enhancement type nMOS transistor with $V_{T0,driver} > 0$
- Load: depletion-type nMOS transistor with $V_{T0,load} < 0$
  - $V_{GS,load} = 0 \Rightarrow V_{GS,load} > V_{T,load}$
  - $V_{SB,load} = V_{out}$



(a) Inverter with depletion-type nMOS load
(b) Simplified equivalent circuit consisting of a nonlinear load resistor & a non-ideal switch controlled by input

Depletion-Load nMOS Inverter (Cont.)

- $V_{SB,load} = V_{out} \Rightarrow$ threshold voltage is a function of V_{out}

$$V_{T,load} = V_{T0,load} + \gamma(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|})$$

- When V_{out} is low $V_{out} < V_{DD}+V_{T,load} \Rightarrow$ depletion-type load transistor is in saturation

$I_{D,load} = (k_{n,load}/2).[-V_{T,load}(V_{out})]^2 = (k_{n,load}/2).|V_{T,load}(V_{out})|^2$

- When V_{out} is high $V_{out} > V_{DD}+V_{T,load} \Rightarrow$ load transistor is in the linear region

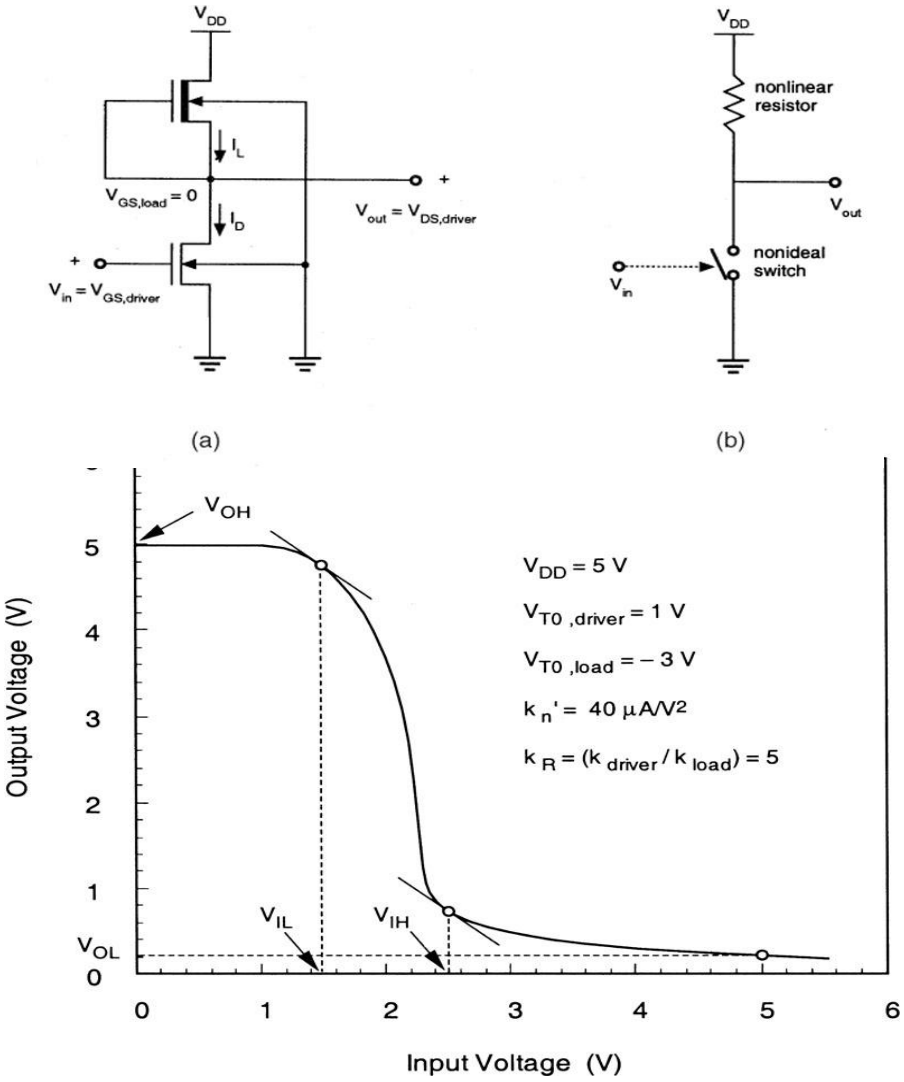
$I_{D,load} = (k_{n,load}/2).[2|V_{T,load}(V_{out})|.(V_{DD}-V_{out})-(V_{DD}-V_{out})^2]$

- VTC can be constructed by setting:

$I_{D,driver} = I_{D,load}$, $V_{GS,driver} = V_{in}$, $V_{DS,driver} = V_{out}$ and solving $V_{out} = f(V_{in})$

Depletion-Load nMOS Inverter (Cont.)

V_{in}	V_{out}	Driver Operating Region	Load Operating Region
V_{OL}	V_{OH}	cut-off	linear
V_{IL}	$\approx V_{OH}$	saturation	linear
V_{IH}	small	linear	saturation
V_{OH}	V_{OL}	linear	saturation



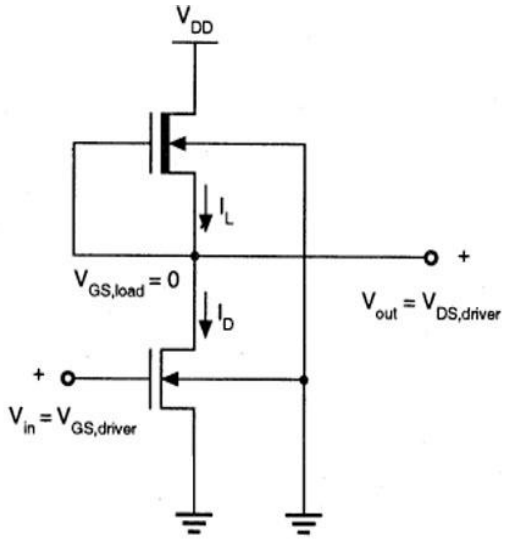
Typical VTC of a depletion-load inverter circuit

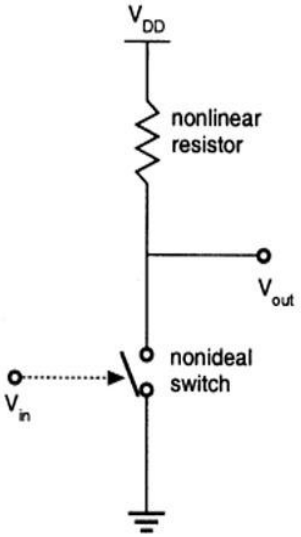
Calculation of V_{OH}

- $V_{in} < V_{T0} \Rightarrow$ driver transistor is in cut-off;
  load transistor is in linear region
- $V_{out} = V_{OH}$, $I_{D,load} = 0$

  $I_{D,load} = (k_{n,load}/2).[2|V_{T,load}(V_{OH})|.(V_{DD}-V_{OH})-(V_{DD}-V_{OH})^2] = 0$
- The only valid solution in the linear region is:

$$V_{OH} = V_{DD}$$





Calculation of V_{OL}

- $V_{in} = V_{OH} = V_{DD} \Rightarrow$ driver transistor is in linear region; and depletion-type load is in saturation

$$(k_{driver}/2).[2.(V_{OH}-V_{T0}).V_{OL}-V_{OL}^2] = (k_{load}/2).[-V_{T,load}(V_{OL})]^2$$

  - Temporarily, neglect dependence of $V_{T,load}$ on V_{OL} resulting in:

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - (\frac{k_{load}}{k_{driver}}).|V_{T,load}(V_{OL})|^2} \qquad \textbf{(I)}$$

- The actual value of V_{OL} is found by solving Eqns I and II (using numerical iterations.) The iterative method converges rapidly, because actual value of V_{OL} is relatively small

$$V_{T,load} = V_{T0,load} + \gamma(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|}) \qquad \textbf{(II)}$$

Calculation of V_{IL}

- $dV_{out}/dV_{in} = -1$ when $V_{in} = V_{IL}$
- Driver transistor in saturation, load transistor in linear region
- KCL at output node:

$$(k_{driver}/2).(V_{in}-V_{T0})^2 = (k_{load}/2).[2|V_{T,load}(V_{out})|.(V_{DD}-V_{out})-(V_{DD}-V_{out})^2] \quad \text{(I)}$$

- After differentiation both sides with respect to V_{in}

$$k_{driver}.(V_{in}-V_{T0}) = (k_{load}/2).[2|V_{T,laod}(V_{out})|(-dV_{out}/dV_{in})+2(V_{DD}-V_{out}).(-dV_{T,load}/dV_{in})-2(V_{DD}-V_{out})(-dV_{out}/dV_{in})]$$

- Assume $(dV_{T,load}/dV_{in})$ is negligible:

$$V_{IL} = V_{T0} + \frac{k_{load}}{k_{driver}} \cdot \left(V_{out} - V_{DD} + \left|V_{T,load}(V_{out})\right|\right) \quad \text{(II)}$$

- The actual value of V_{IL} is found by solving Eqn.s I, II, and III using numerical iterations

$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{\left|2\phi_F\right| + V_{out}} - \sqrt{\left|2\phi_F\right|}\right) \quad \text{(III)}$$

Calculation of V_{IH}

- $dV_{out}/dV_{in} = -1$ when $V_{in} = V_{IH}$
- Driver transistor in linear region, load transistor in saturation

$$(k_{driver}/2).[2.(V_{in}-V_{T0}).V_{out}-V_{out}^2] = (k_{load}/2).[-V_{T,load}(V_{out})]^2 \quad \text{(I)}$$

- Differentiating both sides with respect to V_{in}

$$k_{driver}.[V_{out}+(V_{in}-V_{T0})(dV_{out}/dV_{in})-V_{out}(dV_{out}/dV_{in})]$$
$$= k_{load}.[-V_{T,load}(V_{out})].(dV_{T,load}/dV_{out}).(dV_{out}/dV_{in})$$

- Substitute $(dV_{out}/dV_{in})=-1$ and solve for $V_{in}=V_{IH}$, yielding:

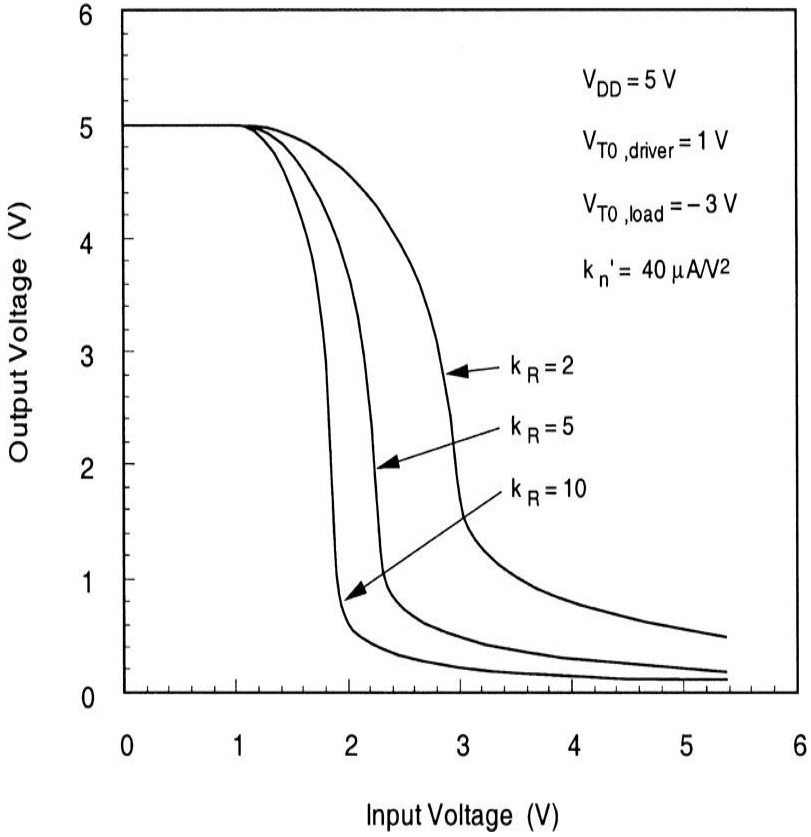
$$V_{IH} = V_{T0} + 2V_{out} + \frac{k_{load}}{k_{driver}} \cdot \left(-V_{T,load}(V_{out})\right) \cdot \frac{dV_{T,load}}{dV_{out}} \quad \text{where} \quad \frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} \quad \text{(II)}$$

- The actual value of V_{IH} is found by solving I, II, and III using numerical iterations

$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|}\right) \quad \text{(III)}$$

Shape of the VTC

- The general shape of VTC and the noise margins are determined by the threshold voltages of the driver and the load devices, and by the driver-to-load ratio $k_R = k_{driver}/k_{load}$
- Threshold voltages are usually set by the fabrication process $\Rightarrow$ k_R emerges as a primary design parameter
- Main advantage: sharp VTC transition and large noise margins is possible with relatively small k_R values (and needs much smaller area than those for resistive load or enhancement-load inverter)



VTC of depletion-load inverters, with different k_R

Design of Depletion-Load Inverter

- Inverter parameters that can be changed by designers:
  1. V_{DD}, dictated by external constraints and by fabrication process
  2. $V_{T,driver}$ and $V_{T,load}$ dictated by external constraints and by fabrication process
  3. (W/L) ratios of the driver and the load transistors (more specifically driver-to-load ratio, k_R), are primary design parameters
- Since $V_{OH} = V_{DD}$, we have three critical voltages on the VTC
- V_{OL} is usually the most significant design constraint and aiming for a certain V_{OL} automatically sets V_{IL} and V_{IH}
- We can re-arrange the V_{OL} equation:

$$k_R = (k_{driver}/k_{load}) = |V_{T,load}(V_{OL})|^2 \; / \; [2(V_{OH}-V_{T0})V_{OL}-V_{OL}^2]$$

Design of Depletion-Load Inverter (Cont.)

$$k_R = [k`_{n,driver} \cdot (W/L)_{driver}] \; / \; [k`_{n,load} \cdot (W/L)_{load}]$$

- $k`_n = \mu_n C_{ox}$. In general $k`_{n,driver} \neq k`_{n,load}$
- But if $k`_{n,driver} \approx k`_{n,load} \Rightarrow k_R = (W/L)_{driver} / (W/L)_{load}$
- So this design procedure determines the ratio of the driver and the load transconductances, but not specific (W/L) ratio of each of the transistors
- Actual sizes of the driver and load transistors are usually determined by other design constraints such as:
  - Current-drive capability
  - Steady-state power dissipation
  - Transition switching speed

Power and Area considerations

- DC power consumption of the depletion-load inverter circuit is found by considering two cases:

1. V_{in}: low $\Rightarrow$ driver transistor is in cut-off and $V_{out} = V_{OH} = V_{DD} \Rightarrow I_D = I_R = 0 \Rightarrow P_{DC\text{-}low} = 0$
2. $V_{in} \approx V_{DD}(high)$ and $V_{out} = V_{OL} \Rightarrow$

$$I_D(V_{in}=V_{DD}) = (k_{load}/2).[-V_{T,load}(V_{OL})]^2$$

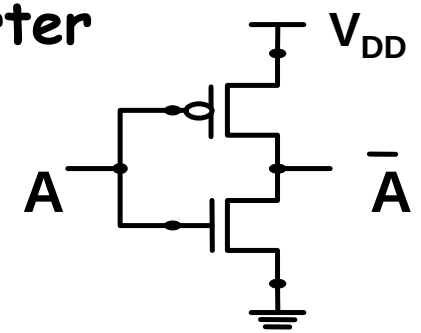
$$= (k_{driver}/2).[2.(V_{OH}-V_{T0}).V_{OL}-V_{OL}^2]$$

- Assume V_{in} is low during 50% of the operation time and high during the other 50% :

$$P_{DC} = (V_{DD}/2).(k_{load}/2).[-V_{T,load}(V_{OL})]^2$$

CMOS Inverter (Cont.)

- Both NMOS and PMOS contribute equally to circuit operation characteristics
- Advantages over the other inverters configurations:
  - Steady-state power dissipation is virtually negligible
  - VTC exhibits a full output voltage swing between 0V and V_{DD} and the VTC is usually sharp
    - VTC resembles those of an ideal inverter

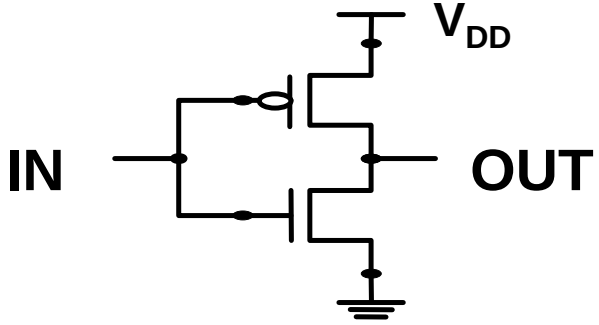


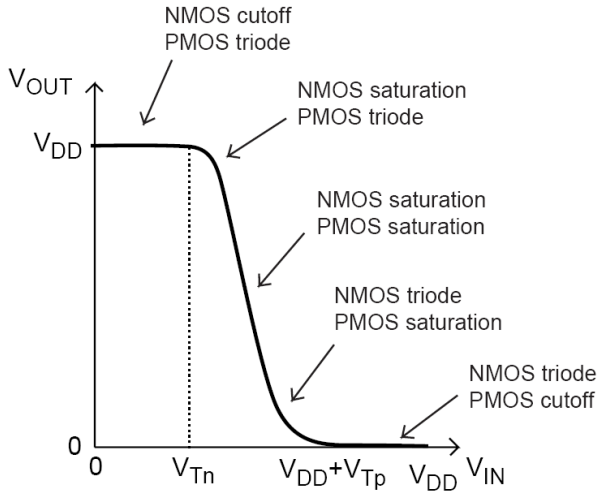
- Disadvantages:
  - Higher process complexity
  - Close proximity of NMOS and PMOS may lead to the formation of two parasitic bipolar transistors, causing latch-up condition, so additional guard rings must be built around NMOS and PMOS transistors

Circuit Operation (Cont.)

Region	Important V_{in} in the region	V_{out}	NMOS	PMOS
A	$< V_{To,n}$	V_{OH}	cut-off	linear
B	V_{IL}	High $\approx V_{OH}$	saturation	linear
C	V_M	V_M	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$> V_{DD}+V_{T0,p}$	V_{OL}	linear	cut-off

$V_{OH} = V_{DD}$ $V_{OL} = 0$





Calculation of V_{IL}

- NMOS transistor in saturation, PMOS transistor in linear region

$I_{D,n} = I_{D,p} \Rightarrow$

$(k_n/2).(V_{in}-V_{T0,n})^2 = (k_p/2).[2.(V_{in}-V_{DD}-V_{T0,p}).(V_{out}-V_{DD}) - (V_{out}-V_{DD})^2]$

- Differentiate both sides wrt V_i

$k_n.(V_{in}-V_{T0,n}) = k_p.[(V_{in}-V_{DD}-V_{T0,p}).(dV_{out}/dV_{in})+(V_{out}-V_{DD}) - (V_{out}-V_{DD}).(dV_{out}/dV_{in})]$

- Substituting $V_{in} = V_{IL}$ and $(dV_{out}/dV_{in}) = -1$:

$$k_n.(V_{IL}-V_{T0,n}) = k_p.(2V_{out}-V_{IL}+V_{T0,p}-V_{DD})$$

- Equations in red must be solved together to get V_{IL} and corresponding output

Solve by iteration

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R.V_{T0,n}}{1+k_R} \quad \text{where} \quad k_R = \frac{k_n}{k_p}$$

Calculation of V_{IH}

- When $V_{in}=V_{IH} \Rightarrow$ nMOS in linear; pMOS in saturation
- KCL at the output node:

$$(k_n/2).[2.(V_{in}-V_{T0,n}).V_{out}-V^2_{out}] = (k_p/2).(V_{in}-V_{DD}-V_{T0,p})^2$$

- Differentiate both sides with respect to V_{in}:

$$k_n.[(V_{in}-V_{T0,n}).(dV_{out}/dV_{in})+V_{out}-V_{out}.(dV_{out}/dV_{in})] = k_p.(V_{in}-V_{DD}-V_{T0,p})$$

- Substituting $V_{in}=V_{IH}$ and $(dV_{out}/dV_{in})=-1$

$$k_n.(-V_{IH}+V_{T0,n}+2V_{out}) = k_p.(V_{IH}-V_{DD}-V_{T0,p})$$

Solve by iteration

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R(2V_{out} + V_{T0,n})}{1+k_R}$$

Calculation of V_M

- Definition: $V_M = V_{in} = V_{out}$
- For $V_{in} = V_{out}$ both transistors are in saturation

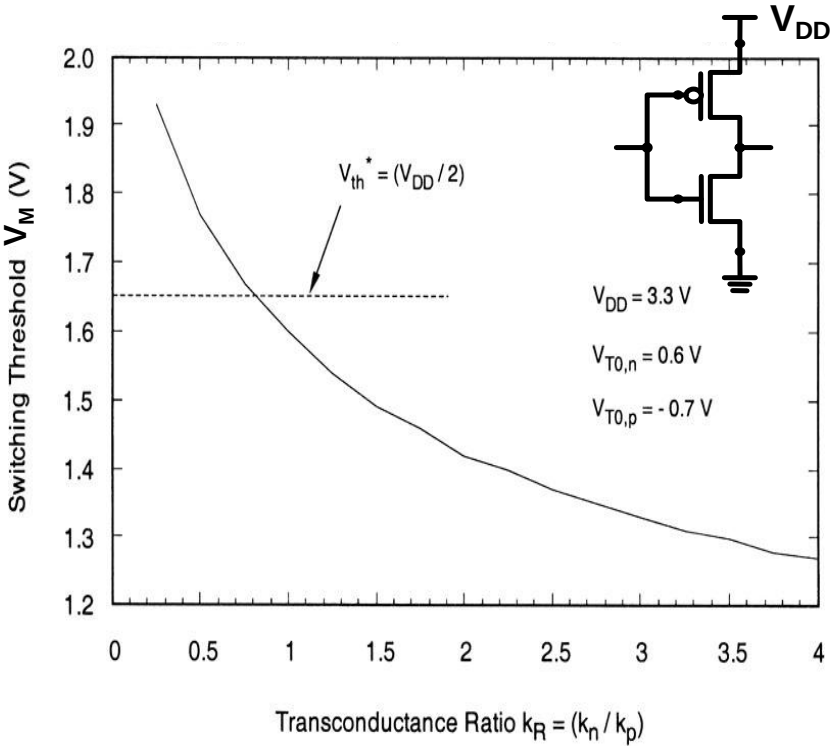
$$k_n/2.(V_{GS,n}-V_{T0,n})^2 = k_p/2.(V_{GS,p}-V_{T0,p})^2$$

$$\Rightarrow k_n.(V_{in}-V_{T0,n})^2 = k_p.(V_{in}-V_{DD}-V_{T0,p})^2$$

$$\Rightarrow V_{in}.[1+(k_p/k_n)^{1/2}] =$$

$$V_{T0,n}+(k_p/k_n)^{1/2}.(V_{DD}+V_{T0,p})$$

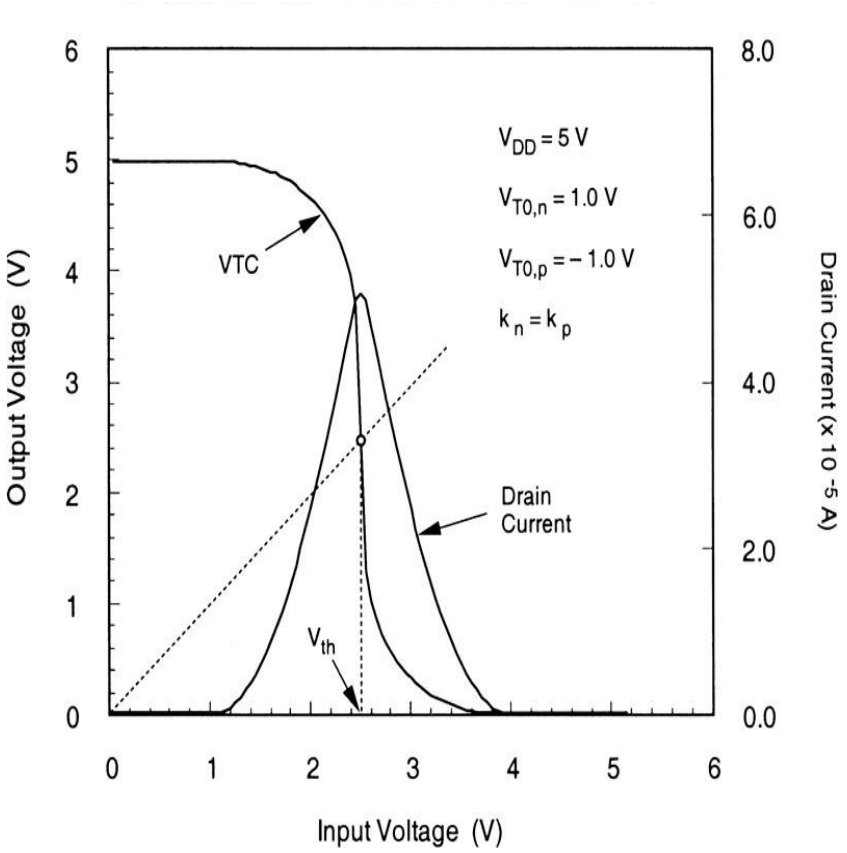
$$V_M = \frac{V_{T0,n} + \frac{1}{\sqrt{k_R}}.(V_{DD} + V_{T0,p})}{1+\frac{1}{\sqrt{k_R}}}$$



Variation of the inversion threshold voltage as a function of k_R

Calculation of V_M (Cont.)

- When $V_{in} < V_{TO,n}$ or $V_{in} > (V_{DD} - V_{TO,p})$ the CMOS inverter does not draw any significant current from power supply except for reverse leakage current of pn-junctions and subthreshold current
- The transistors conduct a nonzero current during low-to-high and high-to-low transitions, i.e., in region B, C, and D
- Current from power supply reaches its peak value when $V_{in}=V_M$ (when both devices are in saturation)



Typical VTC and the power supply current of a CMOS inverter circuit

Design of CMOS Inverters

- V_M is one of the most important parameters that characterize the steady-state input-output behavior of the CMOS inverter circuit
- The CMOS inverter can provide a full output voltage swing between 0 and V_{DD} $\Rightarrow$ noise margins are relatively wide
- Therefore, the problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired voltage value
- Given V_{DD} , $V_{T0,n}$, $V_{T0,p}$ and inverter threshold voltage V_M

$$(1/k_R)^{1/2} = (V_M - V_{T0,n})/(V_{DD} + V_{T0,p} - V_M)$$

$$k_R = k_n/k_p = [(V_{DD} + V_{T0,p} - V_M)/(V_M - V_{T0,n})]^2$$

for an Ideal inverter: $V_{M,ideal} = V_{DD}/2$ $\Rightarrow$

$$(k_n/k_p)_{ideal} = [(0.5V_{DD} + V_{T0,p})/(0.5V_{DD} - V_{T0,n})]^2$$

Design of CMOS Inverters (Cont.)

- For completely symmetric input-output characteristics :

$$V_{TO} = V_{TO,n} = |V_{TO,p}| \Rightarrow (k_n/k_p)_{\text{symmetric inverter}} = 1$$

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox}.(\frac{W}{L})_n}{\mu_p C_{ox}.(\frac{W}{L})_p} = \frac{\mu_n.(\frac{W}{L})_n}{\mu_p.(\frac{W}{L})_p} = 1$$

The above result is based on the assumption that t_{ox}, and hence, C_{ox} have the same values for both transistors

- For ideal symmetric inverter:

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} = \frac{230 cm^2/V \cdot s}{580 cm^2/V \cdot s} \Rightarrow \left(\frac{W}{L}\right)_p \approx 2.52 \left(\frac{W}{L}\right)_n$$

The numerical μ values are typical and they change with surface doping concentration of the substrate and tub

Design of CMOS Inverters (Cont.)

- For a symmetric CMOS inverter with $V_{T0,n} = |V_{T0,p}|$ and $k_R = 1$

$\Rightarrow$

$$V_{IL} = (1/8).(3V_{DD}+2V_{T0,n})$$

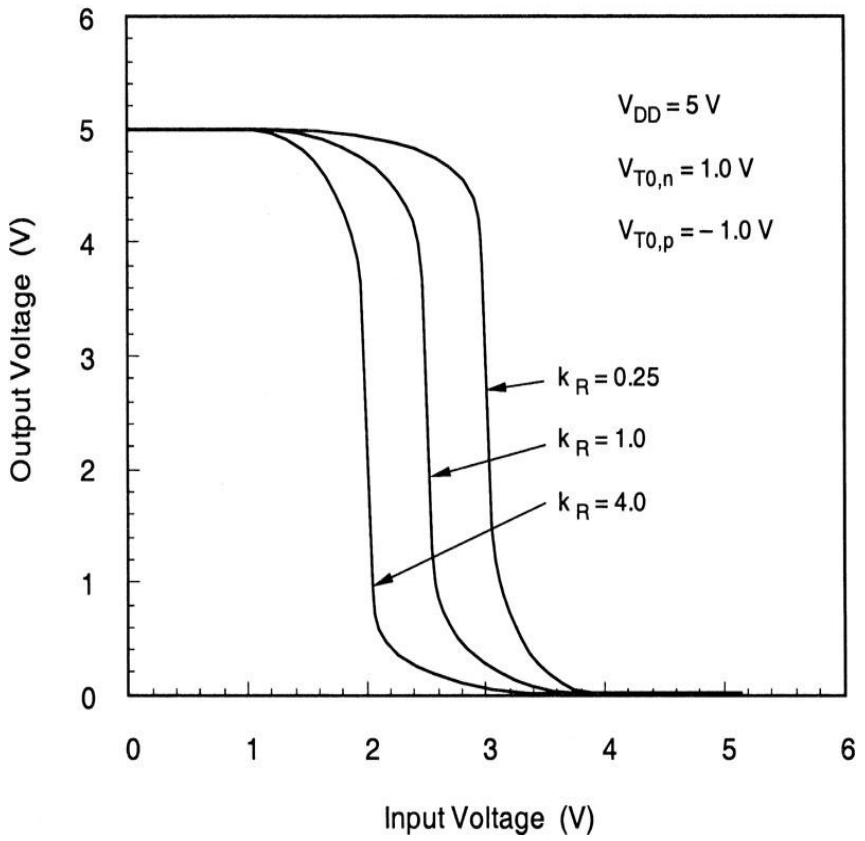
$$V_{IH} = (1/8).(5V_{DD}-2V_{T0,n})$$

$$V_{IL}+V_{IH} = V_{DD}$$

$$NM_L = V_{IL}-V_{OL} = V_{IL}$$

$$NM_H = V_{OH}-V_{IH} = V_{DD}-V_{IH}$$

$$NM_L = NM_H = V_{IL}$$



VTC of three CMOS inverters, with different NMOS-to-pMOS ratios.

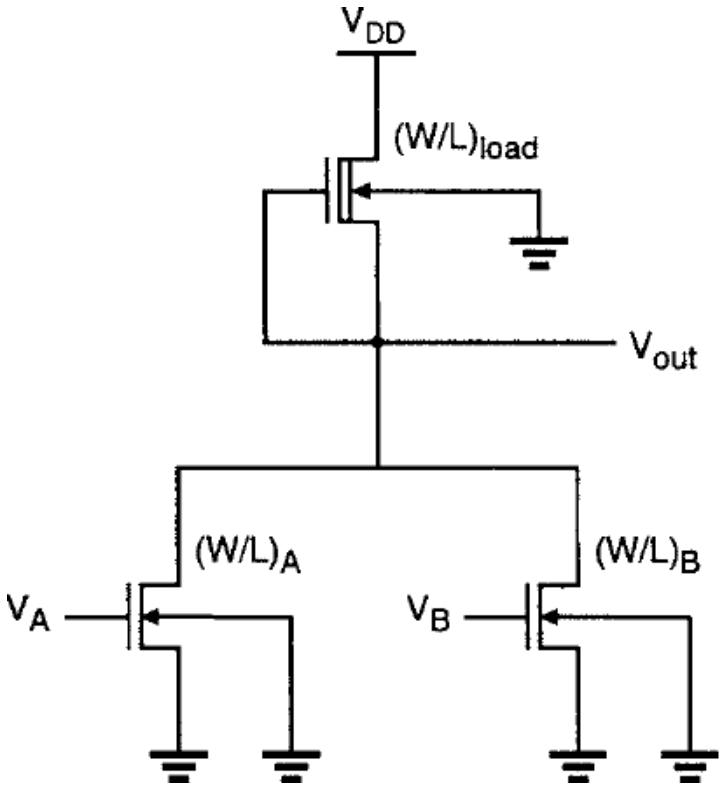
NOR2: Calculation of V_{OL}

- **Calculation of V_{OL}**
  - To calculate the output low voltage V_{OL}, we must consider three different cases as follows:

(i) $V_A=V_{OH}$, $V_B=V_{OL}$

(ii) $V_A=V_{OL}$, $V_B=V_{OH}$

(iii) $V_A=V_{OH}$, $V_B=V_{OH}$



V_{OL} Calculation

- Assuming that the threshold voltages of the two enhancement-type driver transistors are identical, the driver-to-load ratio of the corresponding inverter can be found as follows

In case (i)

$$k_R = \frac{k_{driver,A}}{k_{load}} = \frac{k'_{n,driver}\left(\frac{W}{L}\right)_A}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}$$

In case (ii)

$$k_R = \frac{k_{driver,B}}{k_{load}} = \frac{k'_{n,driver}\left(\frac{W}{L}\right)_B}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}$$

- The output low voltage level V_{OL} in <u>SIS cases</u> is found as:

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}(V_{OL})|^2}$$

V_{OL} Calculation (Cont.)

- In case (iii), the saturated load current is the sum of the two linear-mode driver currents

$$I_{D,load} = I_{D,driverA} + I_{D,driverB}$$

$$\frac{k_{load}}{2}|V_{T,load}(V_{OL})|^2 = \frac{k_{driver,A}}{2}[2(V_A - V_{T0})V_{OL} - V_{OL}{}^2] + \frac{k_{driver,B}}{2}[2(V_B - V_{T0})V_{OL} - V_{OL}{}^2]$$

- Since the gate voltages of both driver transistors are equal we can devise equivalent driver-to-load ratio for the NOR structure

$$k_R = \frac{k_{driver,A} + k_{driver,B}}{k_{load}} = \frac{k'_{n,driver}\left[\left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_B\right]}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}$$

Output Voltage for MIS Case

- In the case iii, the output voltage level is

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver,A} + k_{driver,B}} \right) \cdot |V_{T,load}(V_{OL})|^2}$$

- This result suggests a simple design strategy for designing NOR2 gates – achieve a certain max V_{OL} for case i and ii:

$$k_{driver,A} = k_{driver,B} = k_R k_{load}$$

  - This design choice yields two identical driver transistors, which guarantee the required value of V_{OL} in the worst case

- Note that the V_{OL} for the case iii is lower than that obtained for cases i and ii

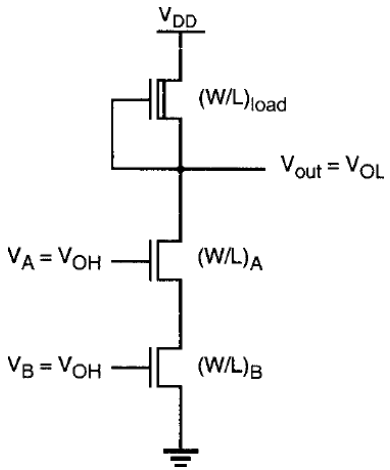
Analysis of NAND2

- Consider NAND2 gate with its inputs set to V_{OH}
  - The drain currents of all transistors in the circuits are equal to each other

$$I_{D,load} = I_{D,driverA} = I_{D,driverB}$$

$$\frac{k_{load}}{2}|V_{T,load}(V_{OL})|^2 = \frac{k_{driver,A}}{2}[2(V_{GS,A} - V_{T,A})V_{DS,A} - V_{DS,A}{}^2]$$

$$= \frac{k_{driver,B}}{2}[2(V_{GS,B} - V_{T,B})V_{DS,B} - V_{DS,B}{}^2]$$



  - The gate-to-source voltages of both driver transistors can be assumed to be approximately equal to V_{OH}
  - We may neglect the substrate-bias effect for driver transistor A, and assume $V_{T,A}=V_{T,B}=V_{TO}$ since the source-to-substrate voltage of driver A is low

Analysis of NAND2 (Cont.)

- (From the previous page equations) the drain-to-source voltages of both driver transistors can be obtained as follows:

$$V_{DS,A} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{TO})^2 - (\frac{k_{load}}{k_{driver,A}}) |V_{T,load}(V_{OL})|^2}$$

$$V_{DS,B} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{TO})^2 - (\frac{k_{load}}{k_{driver,B}}) |V_{T,load}(V_{OL})|^2}$$

- The output voltage V_{OL} is equal to the sum of the drain-to-source voltages of both drivers. Assuming $k_{driver,A} = k_{driver,B} = k_{driver}$ we obtain:

$$V_{OL} \approx 2\left(V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - (\frac{k_{load}}{k_{driver}}) \cdot \left|V_{T,load}(V_{OL})\right|^2} \right)$$

CMOS NOR2 Gate

- As expected: $V_{OH} = V_{DD}$; $V_{OL} = 0$
- For circuit design purposes, the **switching threshold voltage V_M** (or **V_{th}**) of the CMOS gate emerges as a key design criterion

- Assuming both input voltages switch simultaneously, i.e., $V_A = V_B$. Furthermore: $(W/L)_{n,A} = (W/L)_{n,B}$ and $(W/L)_{p,A} = (W/L)_{p,B}$

- By definition, the output voltage is equal to the input voltage at the switching threshold:

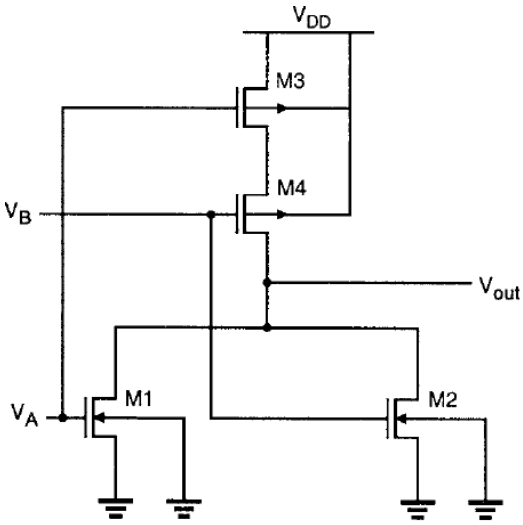
$$V_A = V_B = V_{out} = V_{th}$$

- The combined drain current of the two NMOS transistors is,

$$I_D = k_n (V_{th} - V_{T,n})^2$$

- Thus, we obtain the first equation for the switching threshold:

$$V_{th} = V_{T,n} + \sqrt{\frac{I_D}{k_n}}$$



CMOS NOR2 Gate (Cont.)

- The pMOS transistor, M3, operates in the linear region, while the other transistor, M4, is in saturation for $V_{in}=V_{out}$

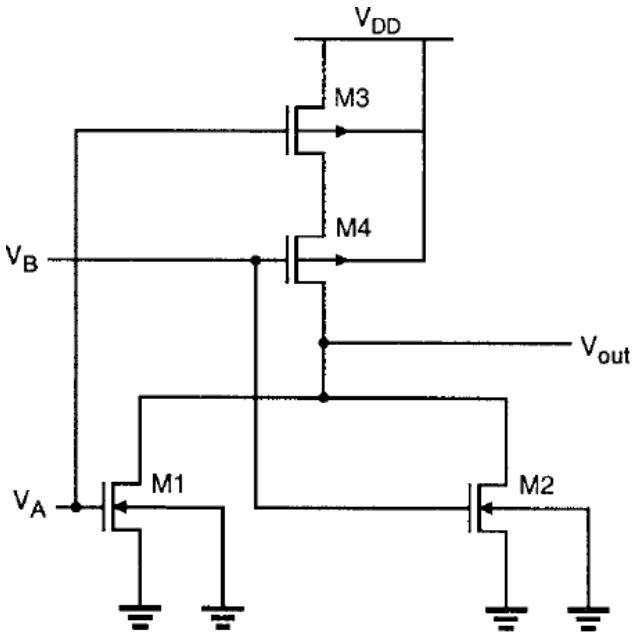
$$I_{D3}=\frac{k_p}{2}[2(V_{th}-V_{DD}+|V_{T,p}|)V_{DS3}-V_{DS3}^{\ 2}] \qquad I_{D4}=\frac{k_p}{2}(V_{th}-V_{DD}-V_{DS3}+|V_{T,p}|)^2$$

- The drain current of both pMOS transistors are identical: $I_{D3} = I_{D4} = I_D$ this yields the second equation of the switching threshold:

$$V_{DD}-V_{th}-|V_{T,p}|=2\sqrt{\frac{I_D}{k_p}}$$

- Combining these two equations, we obtain:

$$V_{th}(NOR2)=\frac{V_{T,n}+\frac{1}{2}\sqrt{\frac{k_p}{k_n}}(V_{DD}-|V_{T,p}|)}{1+\frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$$



CMOS NOR2 Gate (Cont.)

- Compare this with the switching threshold voltage of a CMOS inverter:

$$V_{th}(NOR2) = \frac{V_{T,n} + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T,p}|)}{1 + \frac{1}{2}\sqrt{\frac{k_p}{k_n}}}$$

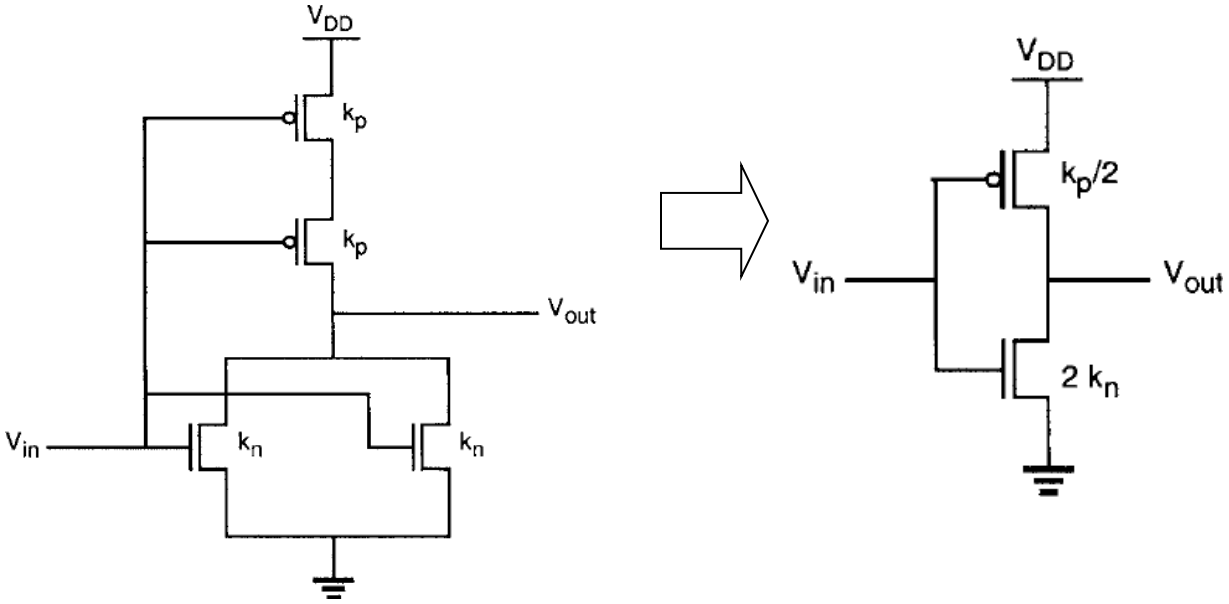
$$V_{th}(INV) = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

- If $k_n = k_p$ and $V_{T,n} = |V_{T,p}|$, the switching threshold of the CMOS inverter is equal to $V_{DD}/2$, whereas the switching threshold of the CMOS inverter is equal to

$$V_{th}(NOR2) = \frac{V_{DD} + V_{T,n}}{3}$$

Alternative Derivation (Equivalent Inverter)

- The switching threshold of the NOR2 gate can be obtained by using the equivalent-inverter approach
  - When both inputs are identical, the parallel-connected NMOS transistors can be represented by a single NMOS transistor with $2k_n$
  - The series-connected pMOS transistors are represented by a single pMOS transistor with $k_p/2$



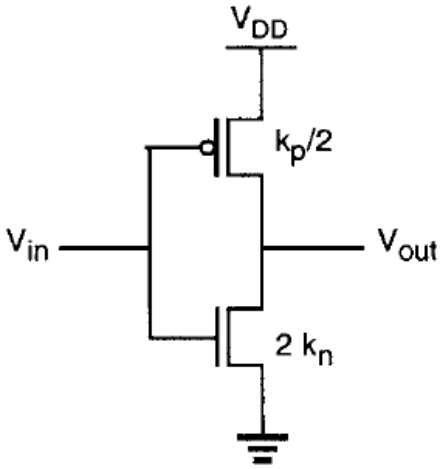
- Using the inverter switching threshold expression for the equivalent inverter circuit, we obtain:

$$V_{th}(NOR2) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{k_p}{4k_n}}}$$

Note: $V_{T,n} = |V_{T,p}|$ and $k_p = 4k_n \Rightarrow V_{th} = V_{DD}/2$

Alternative Derivation (Cont.)

- Using the inverter switching threshold expression for the equivalent inverter circuit, we obtain:



$$V_{th}(NOR2) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{k_p}{4k_n}}}$$

Note: $V_{T,n} = |V_{T,p}|$ and $k_p = 4k_n \Rightarrow V_{th} = V_{DD}/2$