University of Southern California

Viterbi School of Engineering

EE577A

VLSI System Design

Transient Behavior of MOS Gates

References: syllabus textbook, Professor Massoud Pedram's slides, online resources

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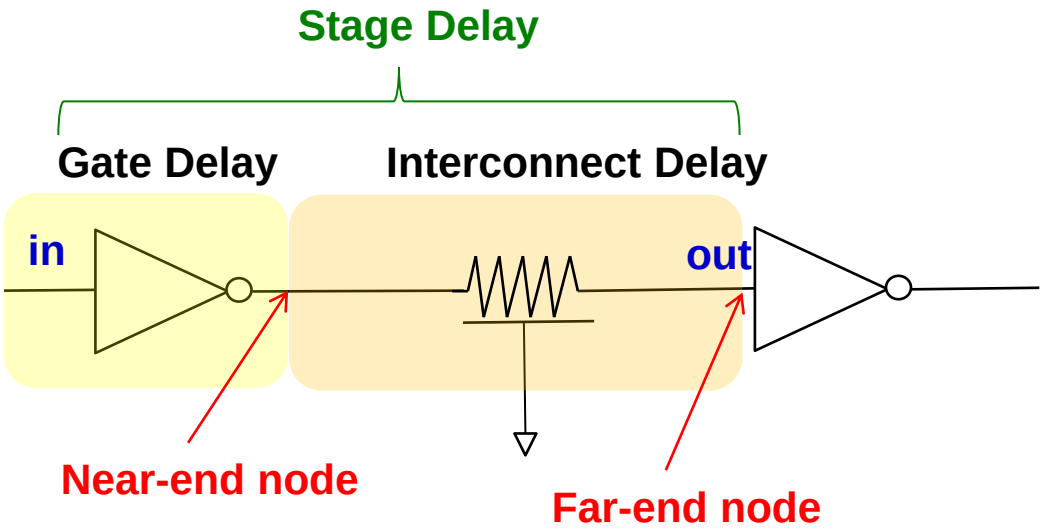
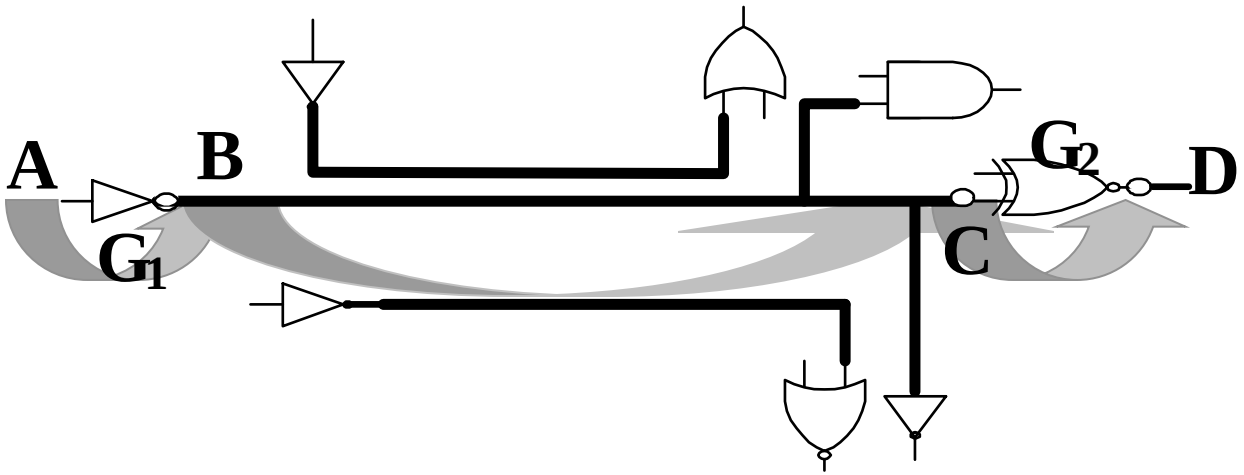
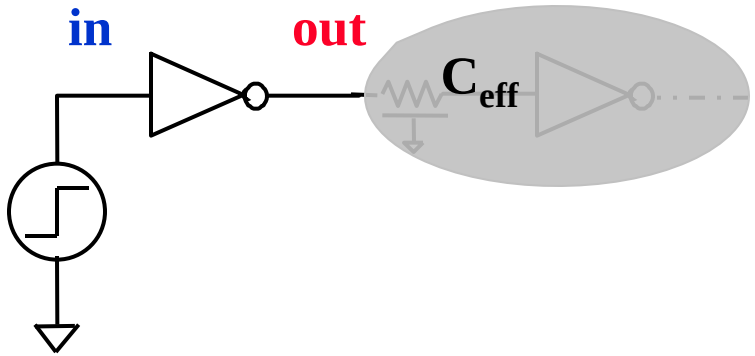
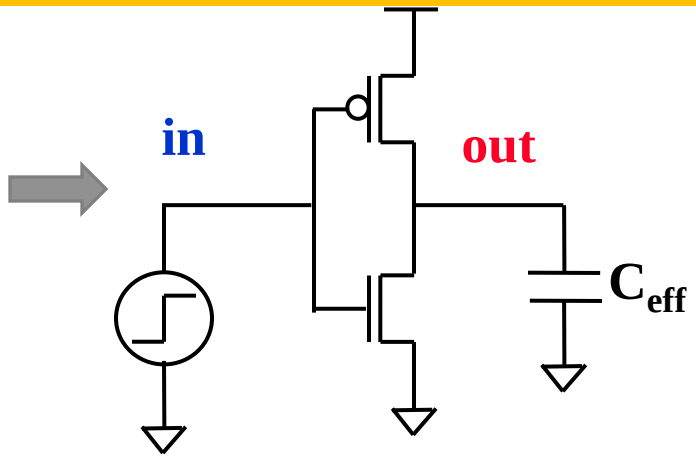
Background

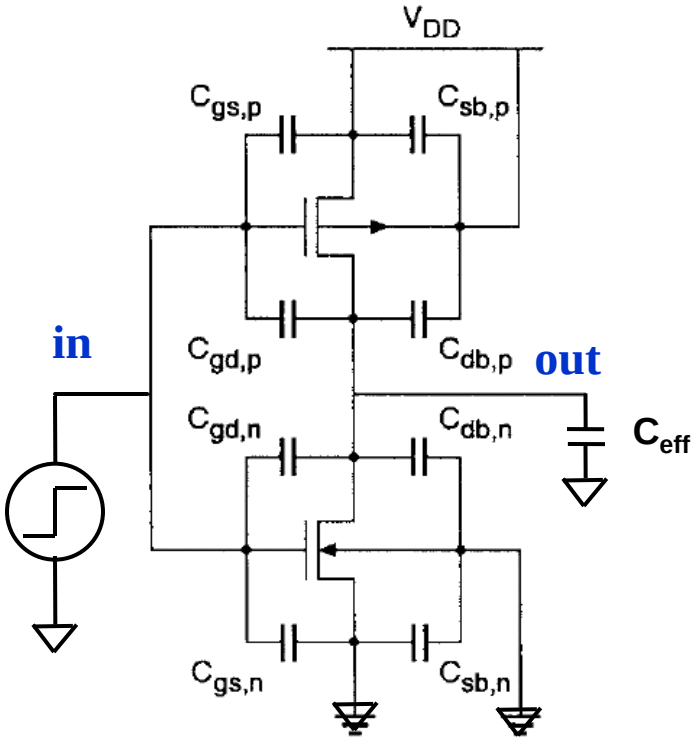

Stage Delay
Gate Delay
Interconnect Delay
in
out
Near-end node
Far-end node


A
B
G1
G2
C
D

CMOS Inverter with a Single Lumped Load



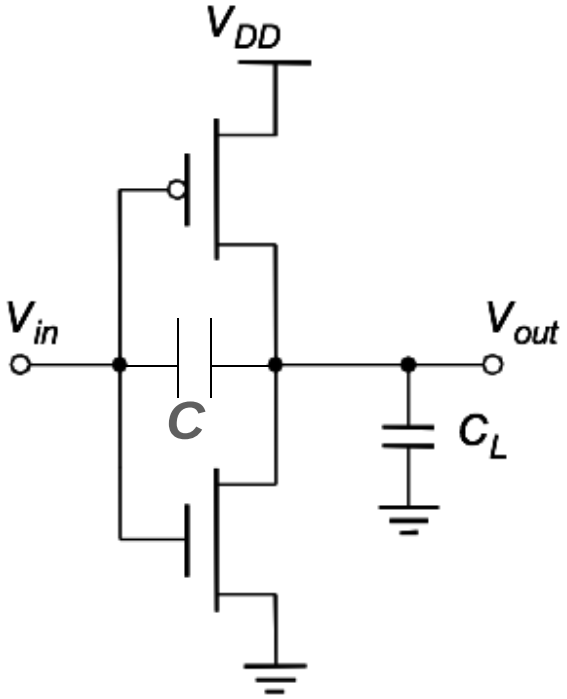


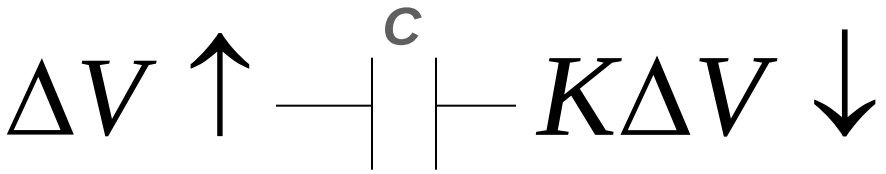


C_{gd}, C_{gs}, C_{gb}: Oxide caps

C_{db}, C_{sb}: Junction caps

Miller Capacitance





$$Q = C(\Delta V - (-K\Delta V))$$

$$= \underbrace{(K+1)C}_{C_{eff}}\Delta V$$

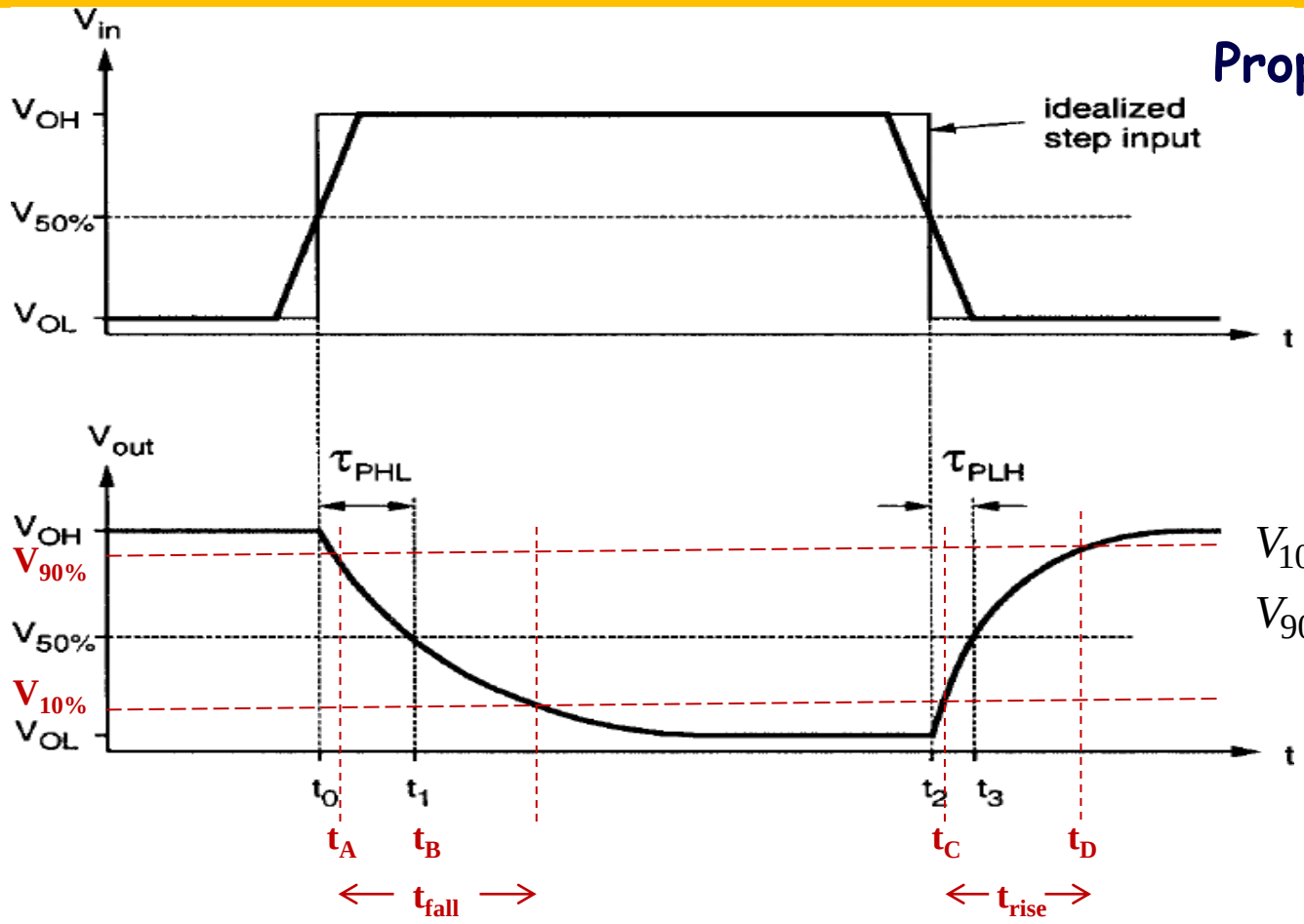
$$K = 1 \rightarrow C_{eff} = 2C$$

$$C_{eff-out} = \frac{K+1}{K}C$$

$$K = 1 \rightarrow C_{eff-out} = 2C$$

Effective Capacitance increases because of Miller Effect

Timing-Related Definitions



Propagation delays:

$$t_{df} \equiv \tau_{pHL} = t_1 - t_0$$

$$t_{dr} \equiv \tau_{pLH} = t_3 - t_2$$

$$V_{50\%} = \frac{1}{2}(V_{OL} + V_{OH})$$

$$V_{10\%} = V_{OL} + 0.1 \cdot (V_{OH} - V_{OL})$$

$$V_{90\%} = V_{OL} + 0.9 \cdot (V_{OH} - V_{OL})$$

Rise and Fall times aka transition times aka slews:

$$t_{fall} = t_B - t_A$$

$$t_{rise} = t_D - t_C$$

Average Capacitance Current Method

- **Let** $I_{avg,HL}$: average current during high-to-low output transition

  $I_{avg,LH}$: average current during low-to-high output transition

- **We can write:**

$$I_{avg,HL} = \frac{1}{2}[i_c(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_c(V_{in} = V_{OH}, V_{out} = V_{50\%})]$$

$$I_{avg,LH} = \frac{1}{2}[i_c(V_{in} = V_{OL}, V_{out} = V_{50\%}) + i_c(V_{in} = V_{OL}, V_{out} = V_{OL})]$$

- **Therefore,**

$$\tau_{pHL} = \frac{C_{load}\Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load}(V_{OH} - V_{50\%})}{I_{avg,HL}}$$

$$\tau_{pLH} = \frac{C_{load}\Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load}(V_{50\%} - V_{OL})}{I_{avg,LH}}$$

- **Similar expressions may be written for rise/fall time calculation**

Delay Calculation for Small-Geometry

- MOS Current driving capability is significantly reduced by velocity saturation:

$$I_D(sat) = W.v_d(sat).C_{ox}.V_{DSAT} \qquad V_{DSAT} = V_{DD} - V_T$$

- Assume discharge and charge currents are approximated with the saturation current (this shows the weak dependence of t_d in low geometry)
  - Better delay estimates possible with better current models such as Sakurai-Newton current model

$$t_{df} = \frac{C_{load}(V_{DD}/2)}{W_n.v_d(sat).C_{ox}(V_{DD} - V_{T,n})}$$

Delay Calculation for CMOS Gates Under Step Input: Quick Approximate Formula

- **Long channel devices (quadratic current equations)**

$$\tau_{pHL} = \frac{C_{load} V_{DD}}{k_n \left(V_{DD} - V_{tn}\right)^2}$$

$$\tau_{pLH} = \frac{C_{load} V_{DD}}{k_p \left(V_{DD} - \left|V_{tp}\right|\right)^2}$$

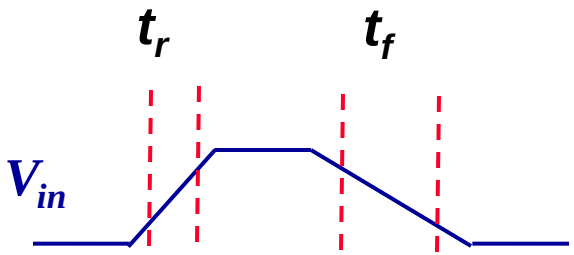
- **Short channel devices (alpha-power current equations)**

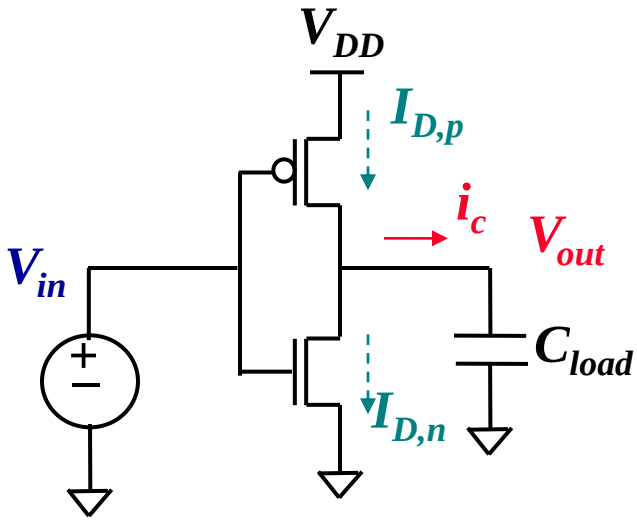
With $1.3 \le \alpha \le 1.6$,

$$\tau_{pHL} = \frac{C_{load} V_{DD}}{k_n \left(V_{DD} - V_{tn}\right)^{\alpha}}$$

$$\tau_{pLH} = \frac{C_{load} V_{DD}}{k_p \left(V_{DD} - \left|V_{tp}\right|\right)^{\alpha}}$$

Gate Delay for Ramp Input





$$t_{df,ramp} = \sqrt{t_{df,step}^2 + \left(t_r/2\right)^2}$$

$$t_{dr,ramp} = \sqrt{t_{dr,step}^2 + \left(t_f/2\right)^2}$$

Fast Ramp Inputs

- Let $V_1 = V_{in} - V_{tn}$ while V_2 denote output voltage when input voltage reaches its final value
- <u>Fast input transitions, i.e,</u>

$$T_{r,in} < 2\tau_{pHL,ramp} \text{ or } T_{f,in} < 2\tau_{pLH,ramp}$$

  - This corresponds to the case when the driver transistor is still saturated when the input voltage ramp reaches its final value (here $V_2 \geq V_1$)

$$T_{f,out} = 2\,\tau_{pHL,step}$$
$$T_{r,out} = 2\,\tau_{pLH,step}$$

$$\tau_{pHL,ramp} = \tau_{pHL,step} + \frac{T_{r,in}}{6}\left(1 + 2\frac{V_{tn}}{V_{DD}}\right)$$
$$\tau_{pLH,ramp} = \tau_{pLH,step} + \frac{T_{f,in}}{6}\left(1 + 2\frac{|V_{tp}|}{V_{DD}}\right)$$

Slow Ramp Inputs

- Slow input transitions, i.e.,

$$T_{r,in} \geq 2\tau_{pHL,ramp} \text{ or } T_{f,in} \geq 2\tau_{pLH,ramp}$$

  - Driver transistor leaves saturation while the input voltage is still ramping (here $V_2 < V_1$)
  - For delay calculation there are two cases to consider: $V_2 < V_{DD}/2$ and $V_2 > V_{DD}/2$. The exact expressions are intricate and involve the *erf* and *ln* functions, respectively
  - Output transition calculation requires a complicated derivation based on solving differential equations with appropriate initial values for different regions of transistor operation

Approximate Gate Delay and Transition Time Calculation for Slow Ramp Inputs

- Approximate expressions for slow input transitions, ignoring the Miller capacitance which causes over/undershoots and also causes short circuit current flow during the output transition:

$$\tau_{pHL,ramp} = \tau_{pHL,step} + \frac{T_{r,in}}{2} \cdot \frac{V_{tn}}{V_{DD}}$$

$$\tau_{pLH,ramp} = \tau_{pLH,step} + \frac{T_{f,in}}{2} \cdot \frac{|V_{tp}|}{V_{DD}}$$

$$T_{f,out} = 2\,\tau_{pHL,step} \cdot \frac{1 - \frac{V_{tn}}{V_{DD}}}{\frac{1}{2} + \frac{\tau_{pHL,ramp}}{T_{r,in}} - \frac{V_{tn}}{V_{DD}}}$$

$$T_{r,out} = 2\,\tau_{pLH,step} \cdot \frac{1 - \frac{|V_{tp}|}{V_{DD}}}{\frac{1}{2} + \frac{\tau_{pLH,ramp}}{T_{f,in}} - \frac{|V_{tp}|}{V_{DD}}}$$

- Notice that:

$$T_{r,in} = 2\tau_{pHL,ramp} \Rightarrow \tau_{pHL,ramp} = \frac{\tau_{pHL,step}}{1 - \frac{V_{tn}}{V_{DD}}}$$

$$T_{f,out} = 2\tau_{pHL,step}$$

An Example Calculation for Ramp Input

Consider an inverter driving load C_L with $t_{pHL,step}$=100ps . Calculate the gate delay and output fall time for a rising input with $T_{r,in}$=25ps. Assume V_{tn}/V_{DD}=1/4.

Repeat calculation for $T_{r,in}$=300ps.

Solution:

For fast ramp, $T_{r,in} = 25\,ps$,

$$\tau_{pHL,ramp} = \tau_{pHL,step} + \frac{T_{r,in}}{6}\left(1+2\frac{V_{tn}}{V_{DD}}\right) = 100 + \frac{25}{6}\left(1+\frac{2}{4}\right) = 106.25\,ps$$

$$T_{f,out} = 2\,\tau_{pHL,step} = 2(100) = 200\,ps$$

For slow ramp, $T_{r,in} = 300\,ps$,

$$\tau_{pHL,ramp} = \tau_{pHL,step} + \frac{T_{r,in}}{2}\cdot\frac{V_{tn}}{V_{DD}} = 100 + \frac{300}{2}\left(\frac{1}{4}\right) = 137.5\,ps$$

$$T_{f,out} = 2\,\tau_{pHL,step}\cdot\frac{1-\frac{V_{tn}}{V_{DD}}}{\frac{1}{2}+\frac{\tau_{pHL,ramp}}{T_{r,in}}-\frac{V_{tn}}{V_{DD}}} = 2(100)\left(\frac{1-\frac{1}{4}}{\frac{1}{2}+\frac{137.5}{300}-\frac{1}{4}}\right) = 200\left(\frac{0.75}{0.708}\right) = 211.76\,ps$$