University of Southern California

Viterbi School of Engineering

EE577A

VLSI System Design

Static Timing Analysis

References: syllabus textbook, online resources

Shahin Nazarian

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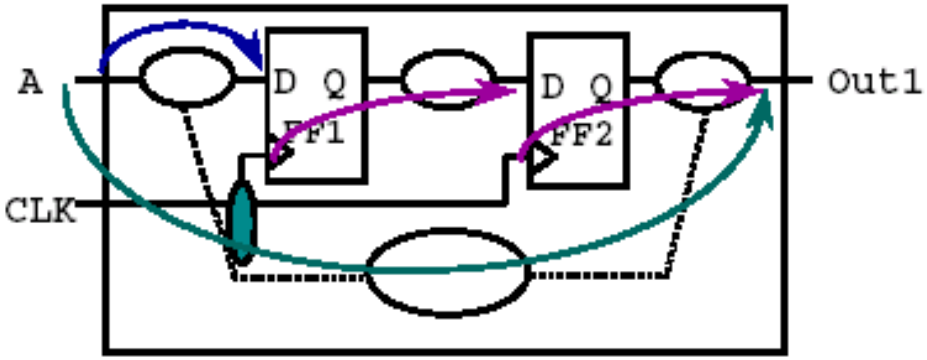
Background

- Objective
- Delay dependencies
- Timing models

Steps in Static Timing Analysis



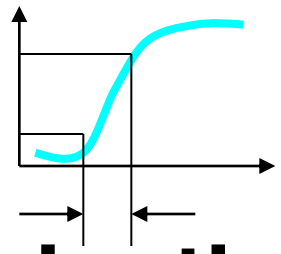
- Circuit is broken down into sets of timing paths
- Delay of each path is calculated
- Path delays are checked to see if timing constraints have been met

Delay Models

- Delay Model Classification
  - Linear
  - Nonlinear

K-Factor Gate Delay

- K-factor equation
  - Delay $t_d = k(t_{r/f}, C_{total})$
  - Output transition time $t'_{r/f} = k'(t_{r/f}, C_{total})$
- Example of K-factor form:
  - Delay= $a*t+b*C_{total}+c*t*C_{total}+d$
  - Obtained from SPICE simulation



NLDM Lookup Tables

```
cell_fall(delay_template_3x4) {
index_1 ("0.1, 0.4, 0.9"); /* Input transition */
index_2 ("0.11, 0.25, 1.31, 2.55"); /* Output capacitance */
values ( /* 0.11 0.25 1.31 2.55 */ \
/* 0.1 */ "0.0617, 0.1537, 0.5280, 0.9338", \
/* 0.4 */ "0.0918, 0.2027, 0.5676, 0.9547", \
/* 0.9 */ "0.1034, 0.2273, 0.6452, 1.0984");
}
```

NLDM Lookup Tables (Cont.)

- **Interpolation**

$$T_{IP} = x20 * y20 * T11 + x20 * y01 * T12 + x01 * y20 * T21 + x01 * y01 * T22$$

  - **where**

$$x01 = (x0 - x1) / (x2 - x1)$$

$$x20 = (x2 - x0) / (x2 - x1)$$

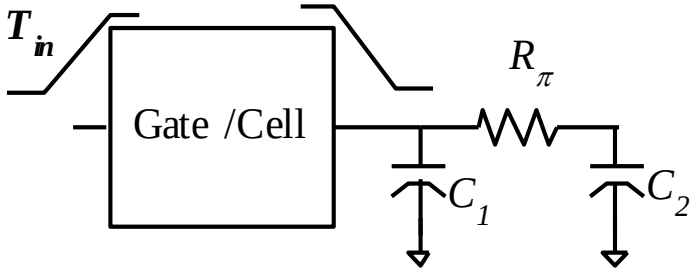
$$y01 = (y0 - y1) / (y2 - y1)$$

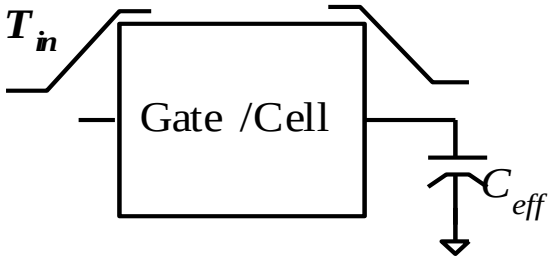
$$y20 = (y2 - y0) / (y2 - y1)$$

NLDM Lookup Tables (Cont.)

- Slew derating
  - Slew to represent the linear portion
  - Current vs old slew measurement
  - Example: Derating factor of 0.5 for (10%, 90%) measurement to (30%,70%)

Effective Capacitance





$$C_{eff} = C_1 + kC_2 \qquad 0<k<1$$

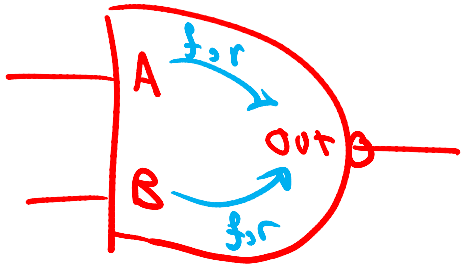
- **Because of the shielding effect of the interconnect resistance , the driver will only "see" a portion of the far-end capacitance C2**

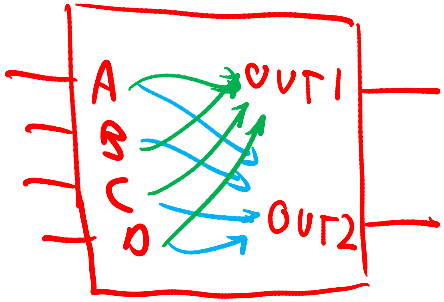
$$R_\pi \longrightarrow 0 \Longrightarrow k = 1$$

$$R_\pi \longrightarrow \infty \Longrightarrow k = 0$$

Timing Models – Combinational Cells

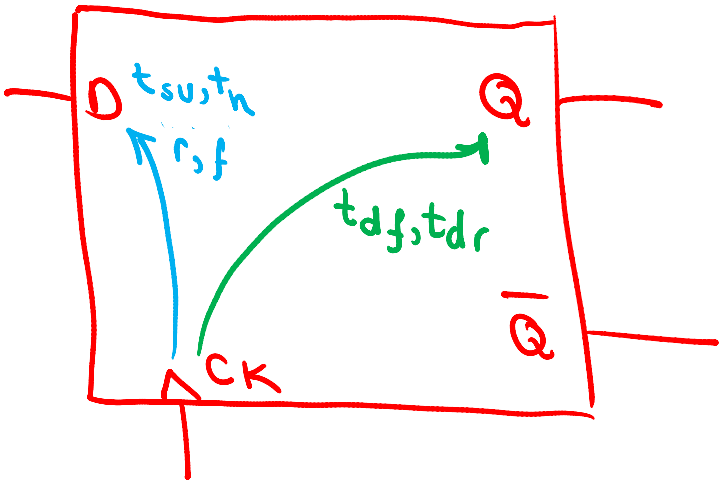
- Timing arcs: represent the propagation delays through the cell
  - Positive vs negative unate





Timing Models – Sequential Cells

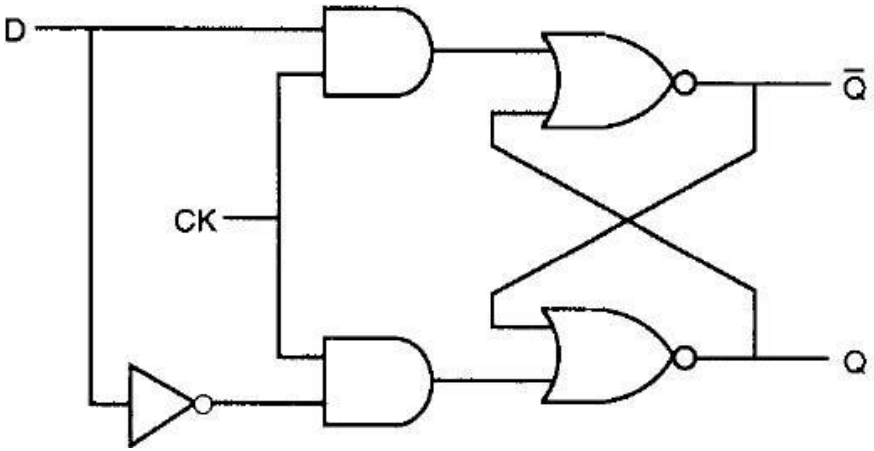
- Synchronous inputs
- Synchronous outputs

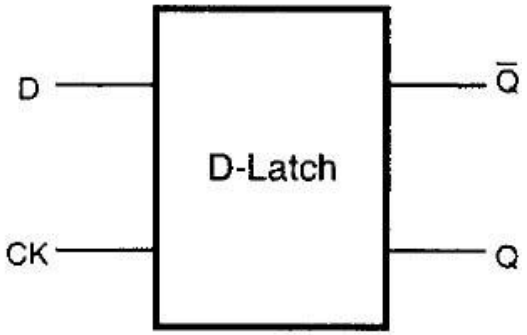


Sequential Elements

- Synchronous inputs
- Synchronous outputs

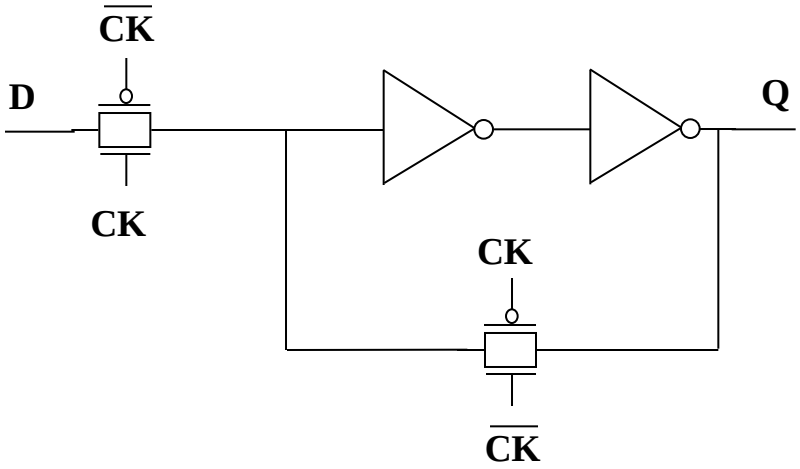
Sequential Cells - Latch



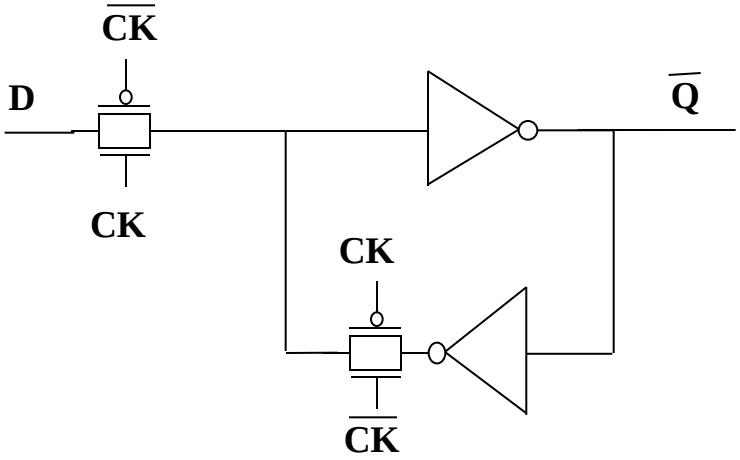


Sequential Cells – Latch (Cont.)

(a)

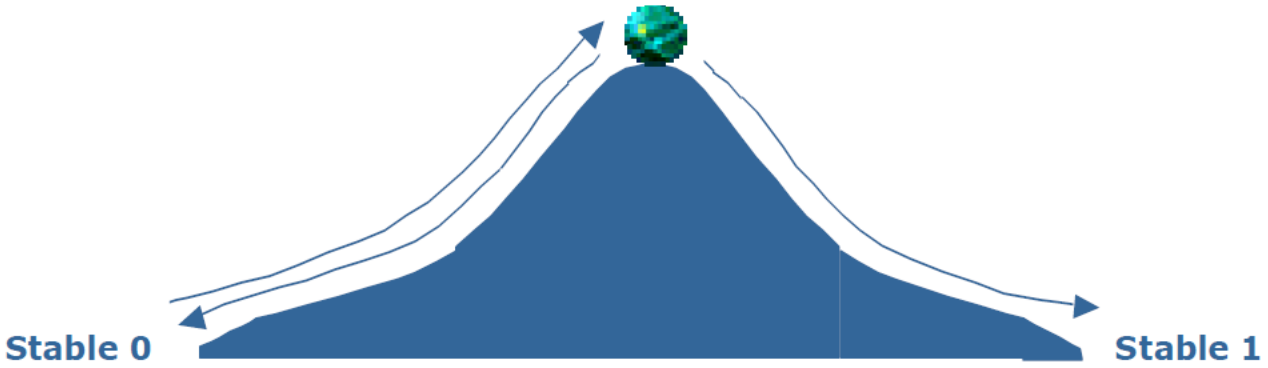


(b)

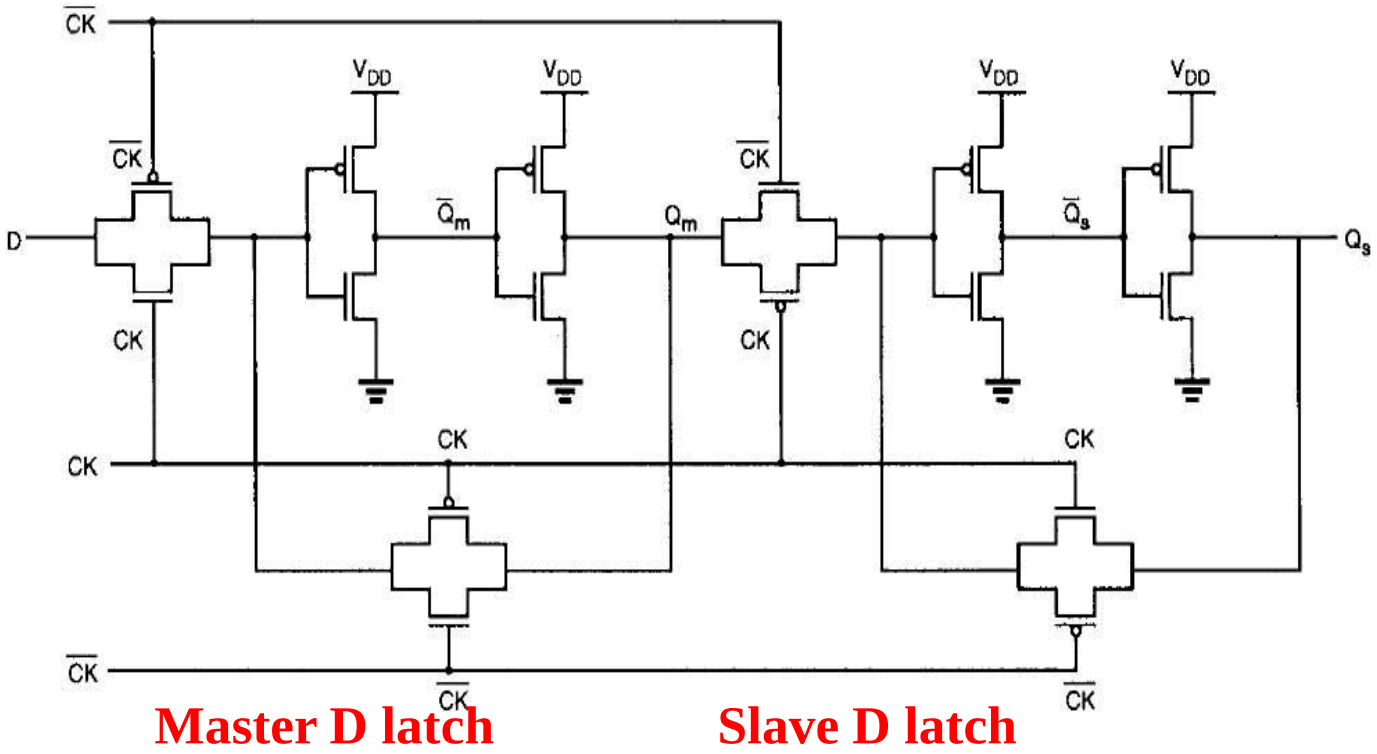


Sequential Cells – Metastability

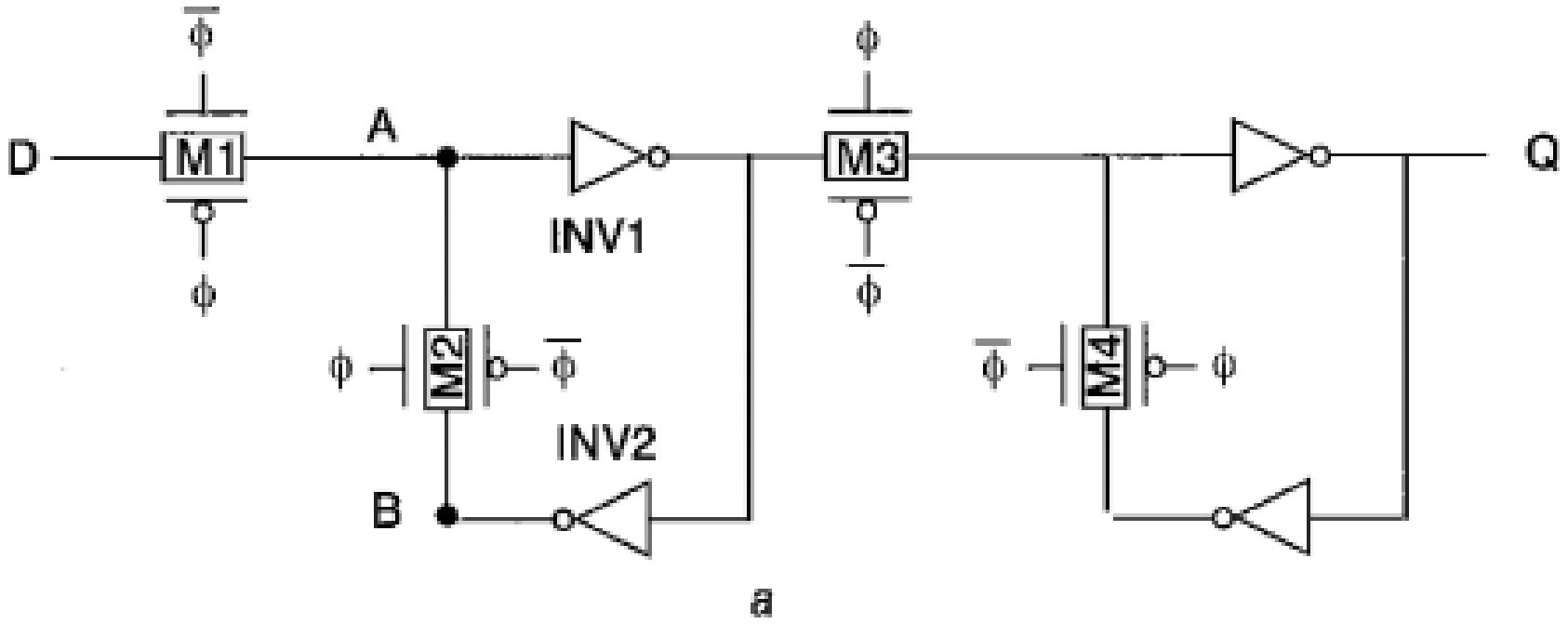
- Being in a metastable state, the flip-flop may be unable to stabilize and this may finally result in a faulty output



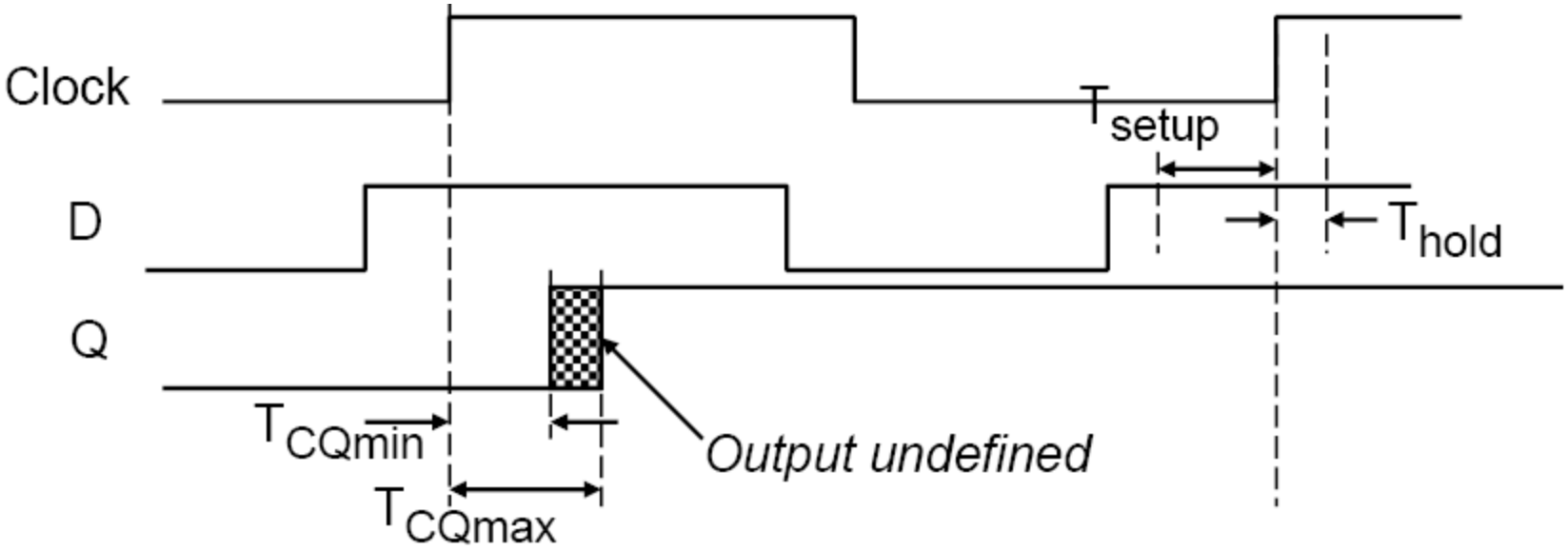
Sequential Cells – D Flip-Flop

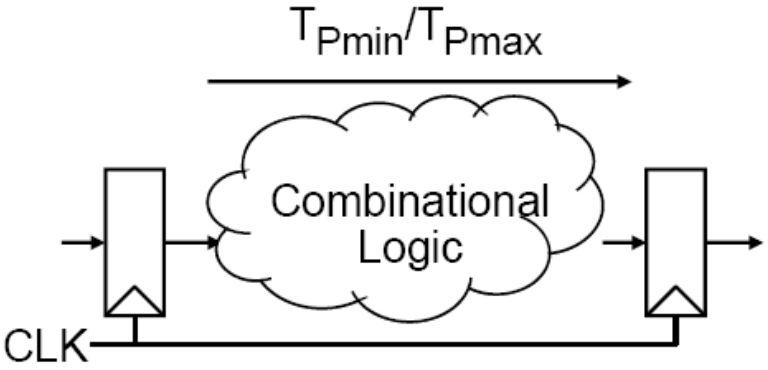


Sequential Cells – D Flip-Flop

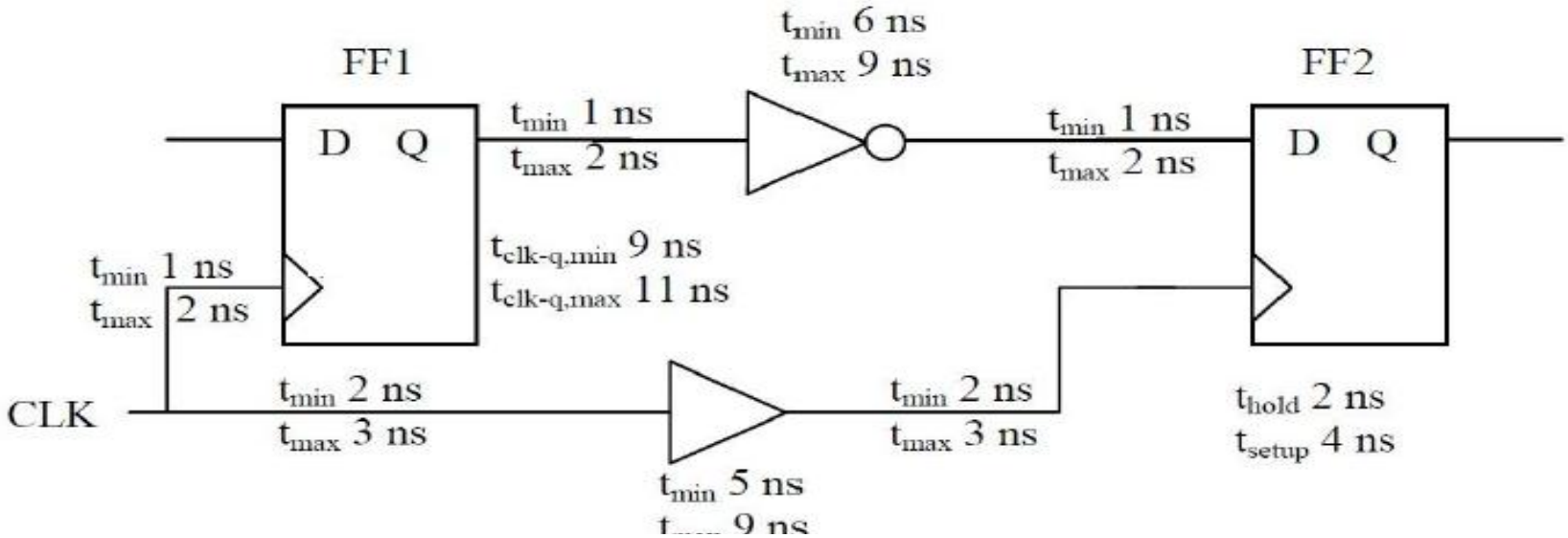


Clock-to-Q Delay and Timing Constraints





Setup and Hold Checks



For SETUP :

Delay in Data path = max(wire delay to the clock input of FF1) + max(Clk-to-Q delay of FF1) +max(cell delay of inverter) + max(2 wire delay- "Q of FF1-to-inverter" and "inverter-to-D of FF2")**=Td = 2+11+9+(2+2) = 26ns**

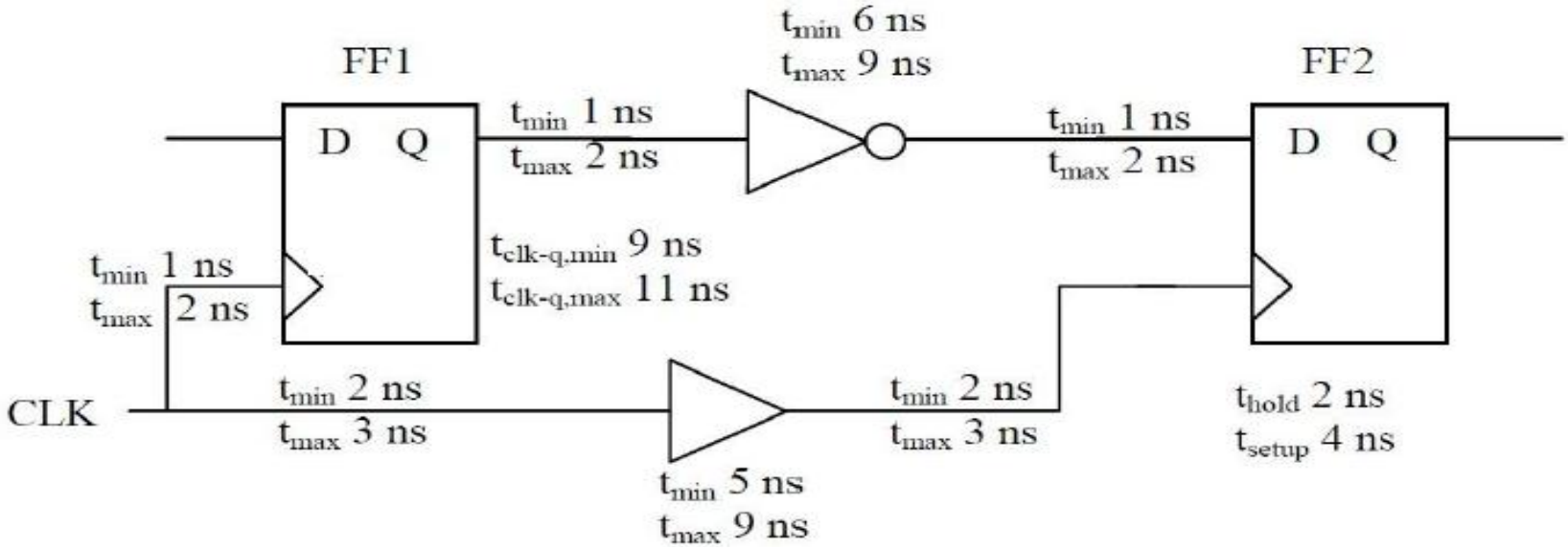
Clock path Delay = (Clock period) + min(wire delay from CLK to Buffer input) + min(cell delay of Buffer) + min(wire delay from Buffer output to FF2/CLK pin) - (Setup time of FF2)

=Tclk = 15+2+5+2-4=20ns

Setup Slack = Tclk - Td = 20ns - 26ns = -6ns.

Since Setup Slack is negative -> Setup violation.

Setup and Hold Checks (Cont.)



For HOLD :

Delay in Data path = min(wire delay to the clock input of FF1) + min(Clk-to-Q delay of FF1) +min(cell delay of inverter) + min(2 wire delay- "Q of FF1-to-inverter" and "inverter-to-D of FF2") **=Td = 1+9+6+(1+1)=18ns**

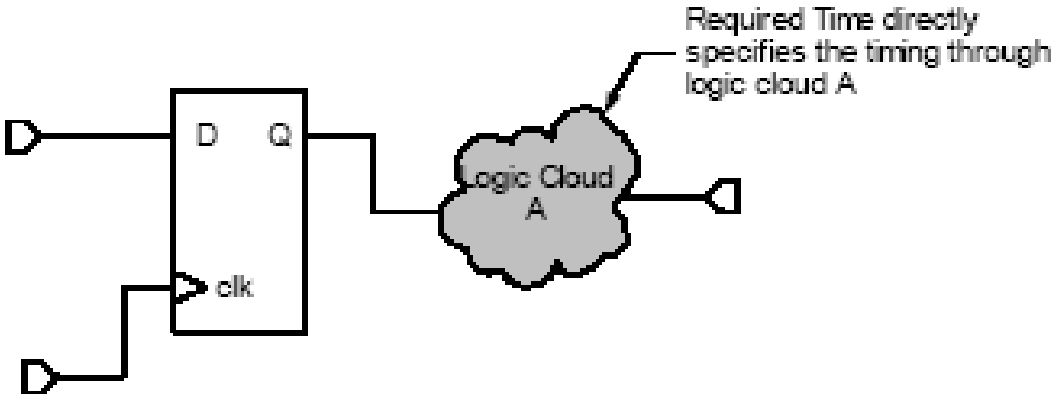
Clock path Delay = max(wire delay from CLK to Buffer input) + max(cell delay of Buffer) + max(wire delay from Buffer output to FF2/CLK pin) + (hold time of FF2)**=Tclk = 3+9+3+2 = 17 ns**

Hold Slack = Td - Tclk = 18ns -17ns = 1ns

Since Hold Slack is positive-> No hold Violation.

Output required time

- Output required time
  - Specifies the data required time on output ports



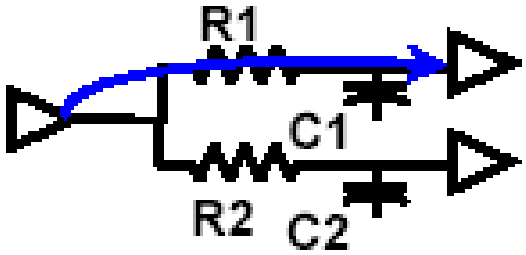
Slack and Critical path

- Slack is the difference between the required (constraint) time and the arrival time (inputs and delays)
  - Negative slack indicates that constraints have not been met, while positive slack indicates that constraints have been met
  - Slack analysis is used to identify timing critical paths in a design by the static timing analysis tool

- Critical path
  - Any logical path in the design that violates the timing constraints
  - Path with a negative slack

Interconnect (Net) Delay

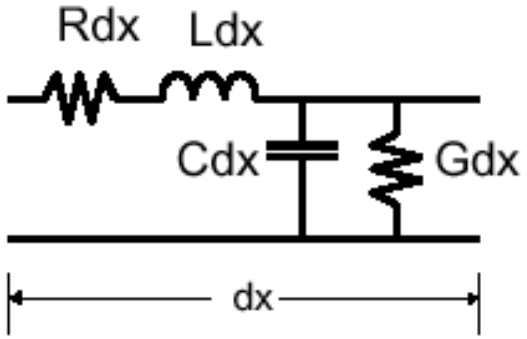
- "Net Delay" refers to the total time needed to charge or discharge all of the parasitics of a given net
- Total net parasitics are affected by
  - Net length
  - Net fanout
- Net delay and parasitics are typically
  - Back-Annotated (Post-Layout) from data obtained from
  - An extraction tool
  - Estimated (Pre-Layout)



Optional: Transmission Line Equations

- **Drop across R and L is :**

$$\frac{\partial V}{\partial x} = RI + L\frac{\partial I}{\partial t}$$



Infinitesimal Model of a Transmission Line

- **Current through C and G is :**

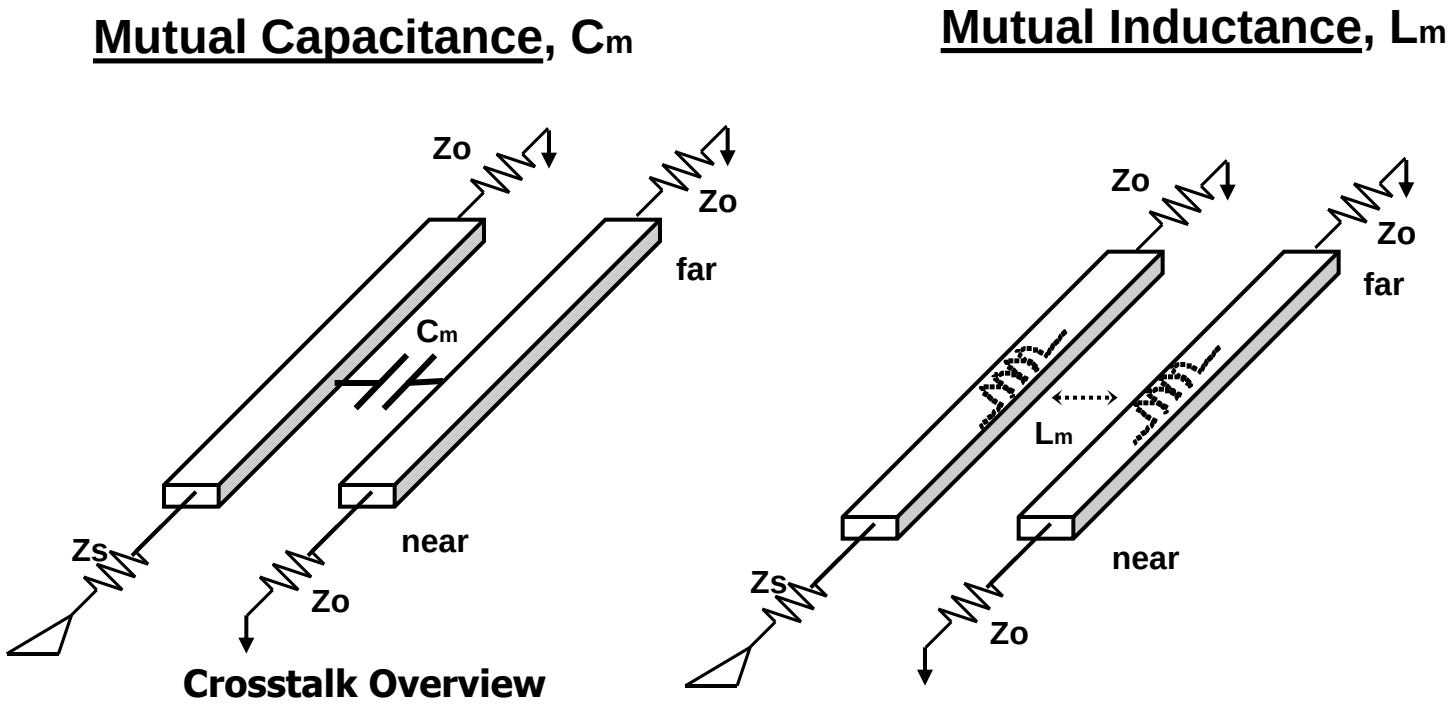
$$\frac{\partial I}{\partial x} = GV + C\frac{\partial V}{\partial t}$$

- **The resulting equation is as follows:**

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

Mutual Inductance and Capacitance

- Crosstalk is the coupling of energy from one line to another via:
  - Mutual capacitance (electric field)
  - Mutual inductance (magnetic field)



Mutual (Cont.)

- The circuit element that represents this transfer of energy are the following familiar equations

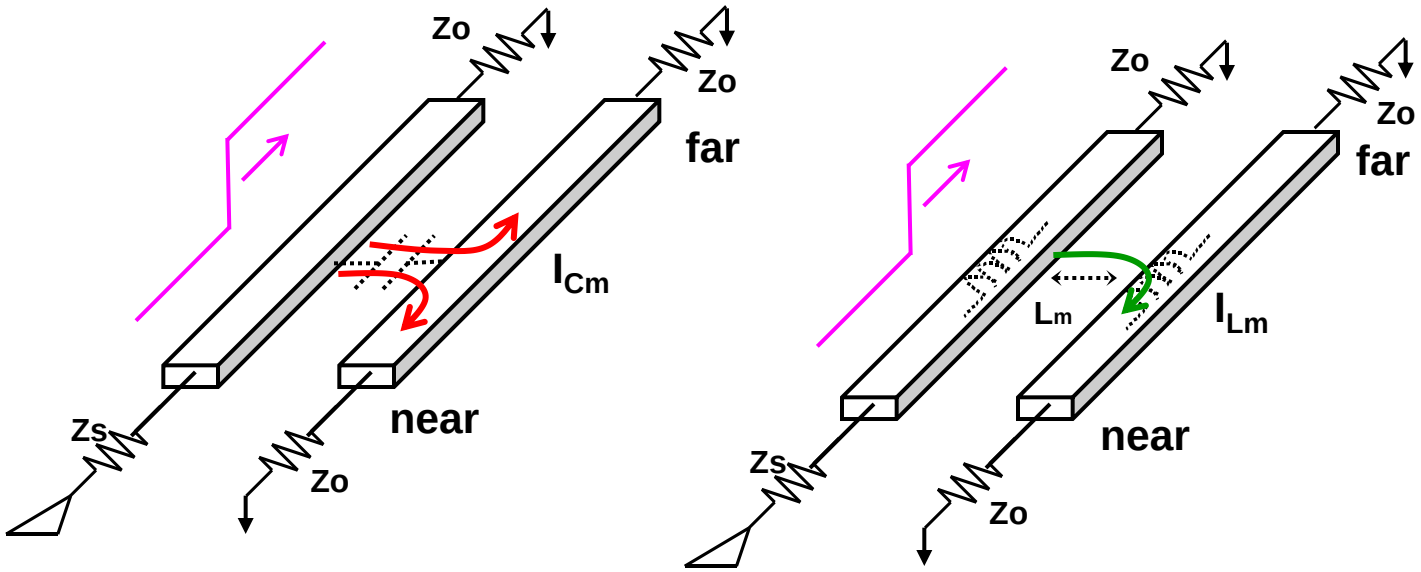
$$V_{Lm} = L_m \frac{dI}{dt} \qquad I_{Cm} = C_m \frac{dV}{dt}$$

- The mutual inductance will induce current on the victim line opposite of the driving current (Lenz's Law)

- The mutual capacitance will pass current through the coupling (mutula) capacitance that flows in both directions on the victim line

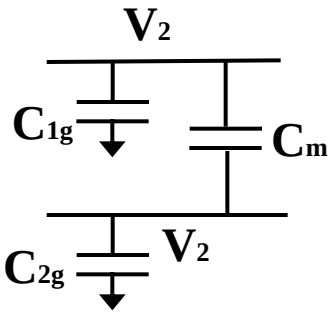
Crosstalk Induced Noise

- The near and far end victim line currents sum to produce the near and the far end crosstalk noise



$$I_{near} = I_{Cm} + I_{Lm} \qquad I_{far} = I_{Cm} - I_{Lm}$$

Crosstalk Induced Noise (Cont.)

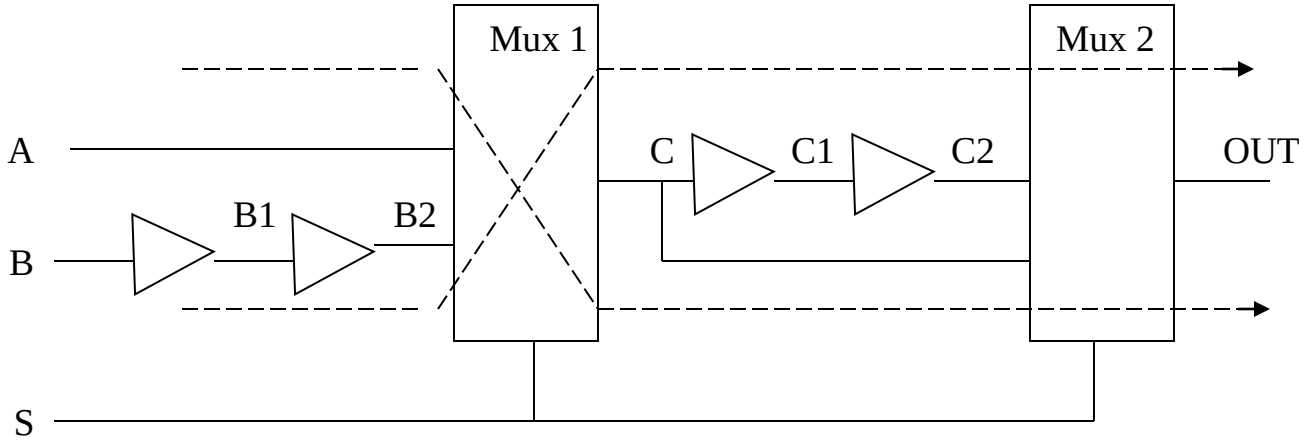


$$I_1 = C_{1g}\frac{dV_1}{dt} + C_m\frac{d(V_1 - V_2)}{dt} = (C_{1g} + C_m)\frac{dV_1}{dt} - C_m\frac{dV_2}{dt}$$

$$I_2 = C_{2g}\frac{dV_2}{dt} + C_m\frac{d(V_2 - V_1)}{dt} = (C_{2g} + C_m)\frac{dV_2}{dt} - C_m\frac{dV_1}{dt}$$

False Paths

- Paths that physically exist in a design but are not logic/functional paths
- These paths never get sensitized under any input conditions



Multi-cycle paths

- Data Paths that require more than one clock period for execution