

Digital Systems Design Lab (CSE 2162) End Sem Exam

Time: 75 minutes

Date: 10/1/22

Max. Marks: 20

Instructions:

- Upload the legible hand written answer sheets in a single pdf with file name <Reg. No.>_ CSE 2162_<Name>.
 - Write your name and signature in all the sheets.
 - 60 minutes for write up and 15 minutes for scanning and uploading.
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1. Design and draw a BCD down counter using T flip flop. Write the Verilog code for positive edge triggered T flip flop. Using this as a sub-circuit, write the Verilog code for your design of BCD down counter. Draw the wave forms for all the cases of T flip flop and all the counts of BCD down counter along with the clock.
 2. Implement the function $F(a, b, c, d) = \Sigma m(0, 2, 5, 9, 11)$ using a 4 to 1 multiplexer and any other necessary gates. Take a, b as select signals. Write Verilog code for 4 to 1 mux using conditional operator. Using this as the sub-circuit, write the hierarchical code for the design.