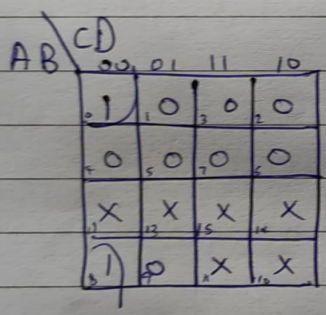
STUDENT'S NAME: Manoj M. Mallya		TOTAL MARKS OBTAINED
CLASS: 3rd sem	SUBJECT: DSDL end sem	
ROLL NO: 23	DATE: 10-01-2022	

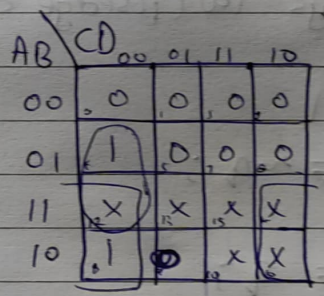
200905130
Manoj

1)

Inputs of CC				Outputs of CC				Inputs of T ff			
A	B	C	D	A	B	C	D	TA	TB	TC	TD
1	0	0	1	1	0	0	0	0	0	0	1
1	0	0	0	0	1	1	1	1	1	1	1
0	1	1	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	1	0	1	1	1
0	0	1	1	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1	1	0	0	1



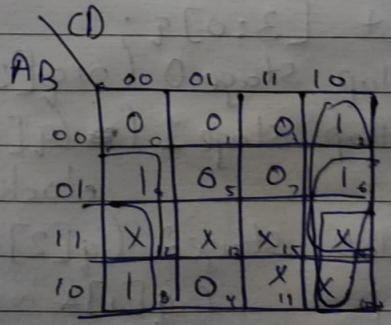
$TA = \bar{B}\bar{C}\bar{D}$



$TB = A\bar{D} + B\bar{C}\bar{D}$

$TD = 1$

$TC = B\bar{D} + A\bar{D} + C\bar{D}$



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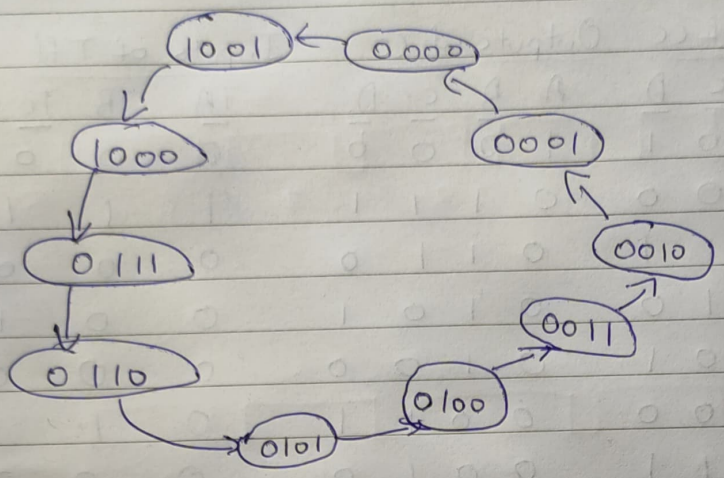


```
module tflipflop (t, clock, q);
input t, clock;
output q;
reg q;
always @(posedge clock)
begin
if(t)
q <= ~q;
else
q <= q;
end
endmodule
// {A, B, C, D} = q - (my code interpretation)
module bcddown (clock, q);
input clock;
output [3:0] q;
tflipflop stage0 (~q[2]&~q[1]&~q[0], clock, q[3]);
tflipflop stage1 ((q[3]&~q[0])|(q[2]&~q[1]&~q[0]),
                  clock, q[2]);
tflipflop stage2 ((q[2]&~q[0])|(q[3]&~q[0])|
                  (q[1]&~q[0]), clock, q[1]);
tflipflop stage3 (1'b1, clock, q[0]);
```

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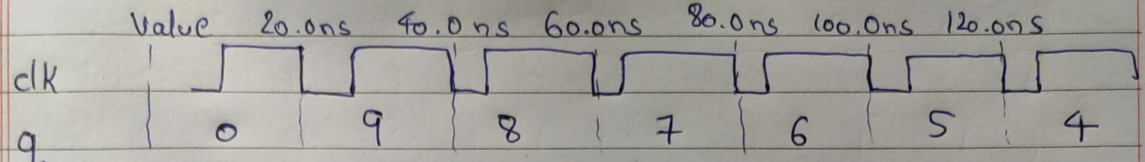
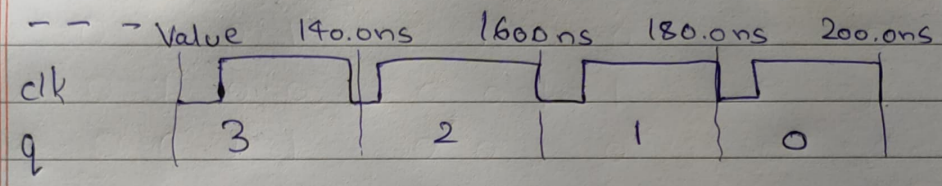
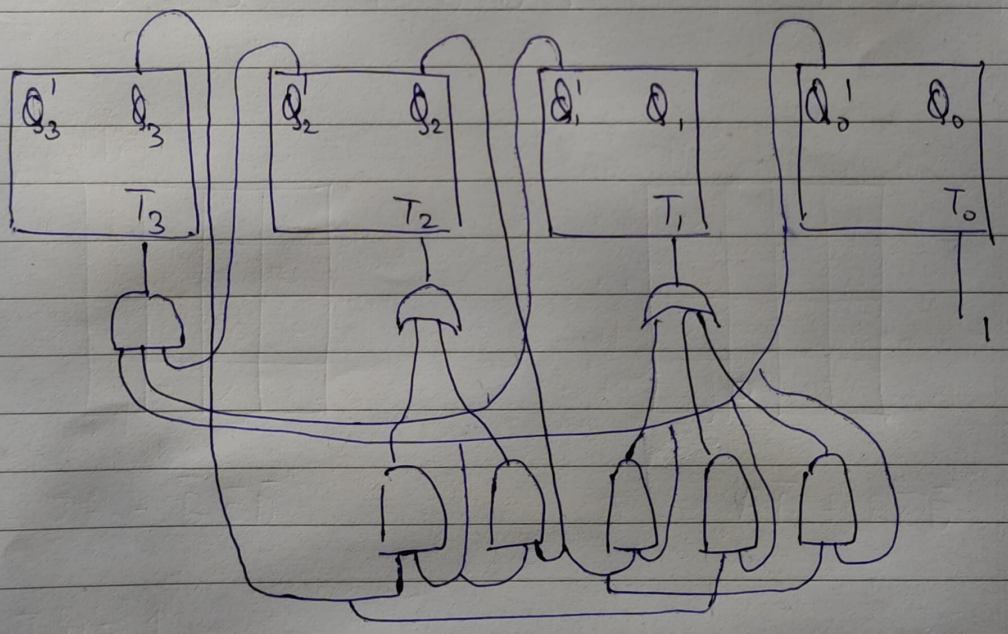
Waveform:-





Design:-



STUDENT'S NAME: Manoj M. Mallya		TOTAL MARKS OBTAINED
CLASS:	SUBJECT:	
ROLL NO:	DATE:	

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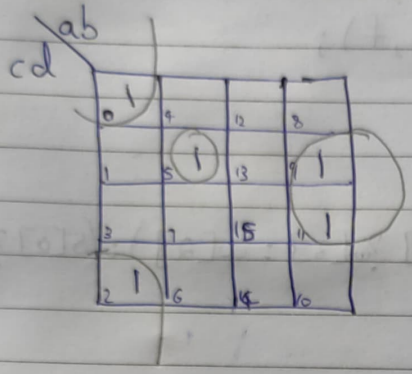
2) $F(a,b,c,d) = \Sigma m\,(0,2,5,9,11)$



$F = a\bar{b}d + \bar{a}b\bar{d} + \bar{a}b\bar{c}d$

Using shannon's expansion,

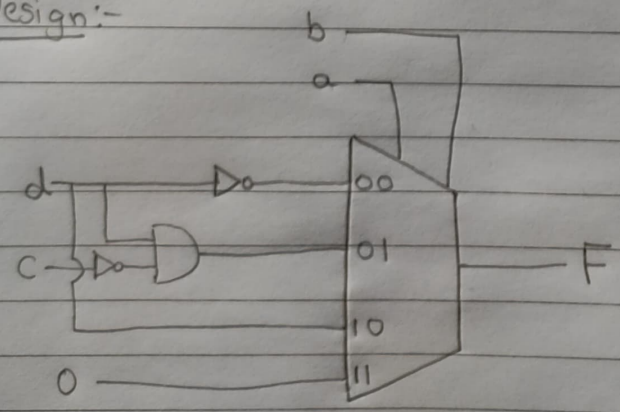
$F_{ab} = (1.0.d) + (1.0.d) + (0.1.\bar{c}.d)$
$= 0 + 0 + 0$
$= 0$

$F_{\bar{a}\bar{b}} = (0.1.d) + (1.1.\bar{d}) + (1.0.\bar{c}.d)$
$= 0 + \bar{d} + 0$
$= \bar{d}$

$F_{a\bar{b}} = (1.1.d) + (0.1.\bar{d}) + (0.0.\bar{c}.d)$
$= d$

$F_{\bar{a}b} = (0.0.d) + (1.0.\bar{d}) + (1.1.\bar{c}.d)$
$= 0 + 0 + \bar{c}.d$
$= \bar{c}d$

Design:-



Priya

20090S130
#Manoj

Manoj M. Mallya

Verilog code:-

```
module mux4to1(w, s, f);
input [3:0]w;
input [1:0]s;
output f;
assign f = s[1] ? (s[0] ?w[3] : w[2]) : (s[0] ? w[1] : w[0]);
endmodule

module examcode (a, b, c, d, F);
input a,b, c, d;
output F;
wire [1:0]s;
wire [3:0]w;
wire p, q;
assign p= ~d;
assign q= ~c+d;
assign s= {a,b};
assign w= { p, q, d, 1'b0};
mux4to1 stage1 (w, s, F);
endmodule
```