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Section : C2

Roll no : 23

DSDL – 7

Exercise :

1) Design and simulate the following counters

a) 4 bit synchronous up counter

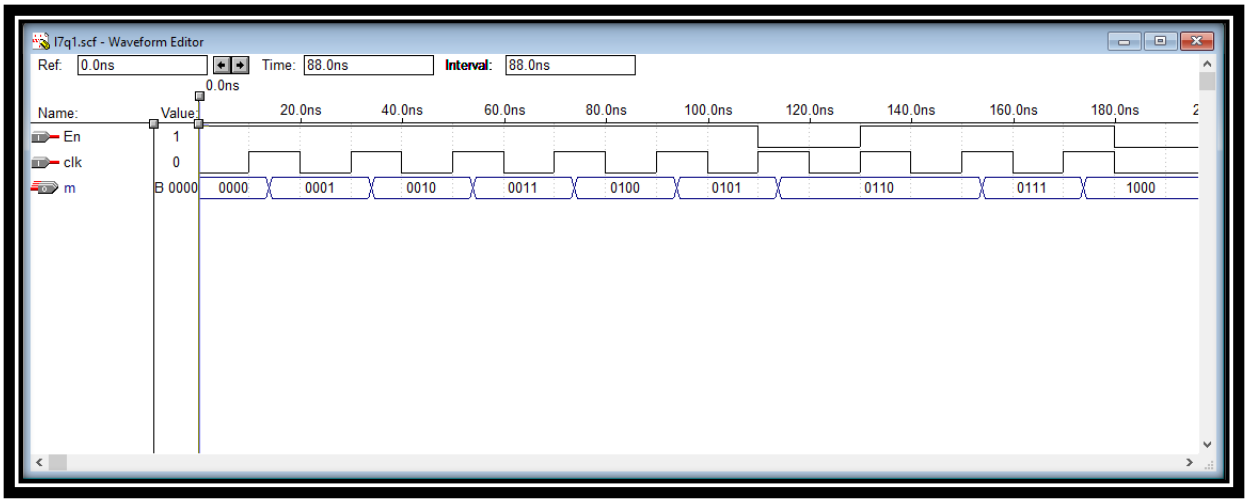
Verilog code :

```
module l7q1(m,clk,En);
 input En;
 input clk;
 output [3:0]m;
 tflipflop stage1(En,clk,m[0]);
 tflipflop stage2(En&m[0],clk,m[1]);
 tflipflop stage3(En&m[0]&m[1],clk,m[2]);
 tflipflop stage4(En&m[0]&m[1]&m[2],clk,m[3]);
endmodule

module tflipflop(T,clock,Q);
 input T,clock;
 output Q;
 reg Q;
 always@(posedge clock)
 if(T)
```

```
 Q<=~Q;
endmodule
```

Output :



b) 3 bit synchronous up/down counter with a control input up/down'. If up/down' = 1, then the circuit should behave as an up counter. If up/down' = 0, then the circuit should behave as a down counter.

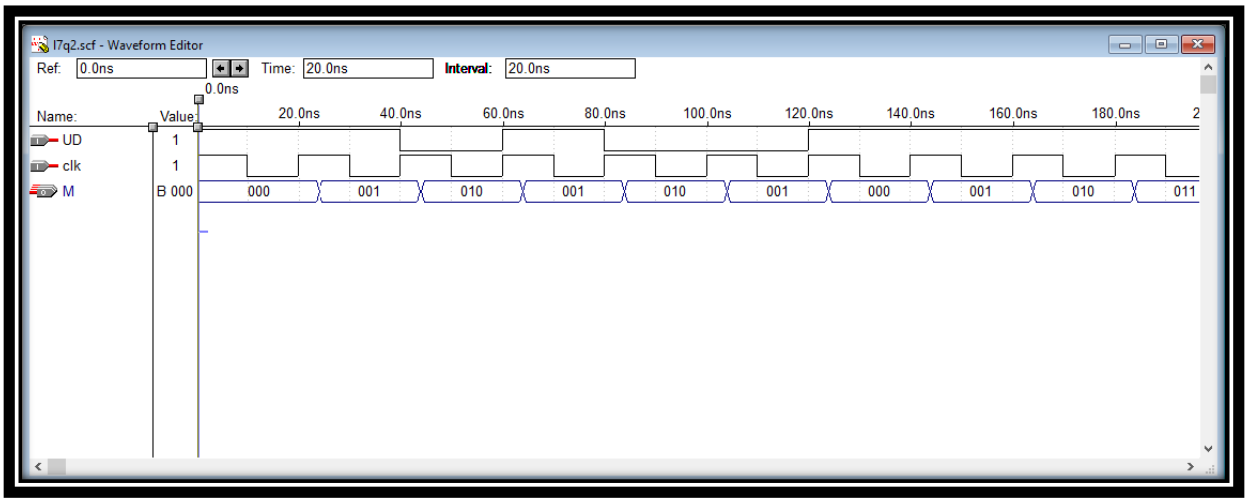
Verilog code :

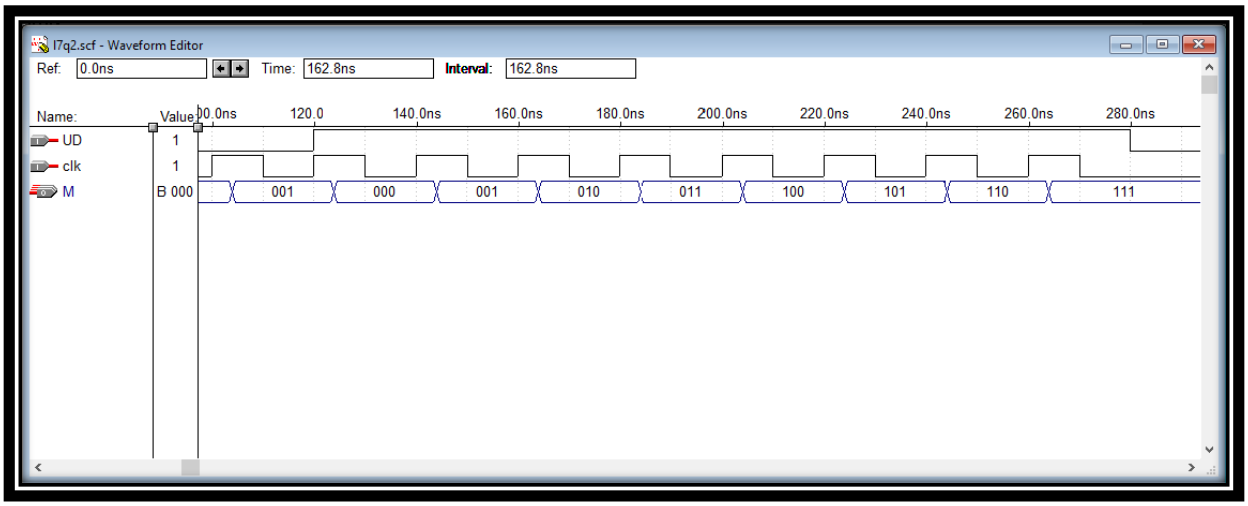
```
module l7q2(clk,UD,M);
 input UD;
 input clk;
 output [2:0]M;
 wire control;
 tflipflop stage1(1,clk,M[0]);
 tflipflop stage2((UD & M[0])|(~UD & ~M[0]),clk,M[1]);
 tflipflop stage3((UD & M[0] & M[1])|(~UD & ~M[0] & ~M[1]),clk,M[2]);
endmodule

module tflipflop(T,clock,Q);
 input T,clock;
```

```
output Q;
reg Q;
always@(posedge clock)
if(T)
Q<=~Q;
endmodule
```

Output :





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