Statement of Objectives

by Amitabh YADAV

Despite the availability of better healthcare today, mental illness is a topic left scarcely discussed in large parts of the world. In fact, according the Indian National Mental Health Survey[1], nearly 14% of Indians suffer from mental illness and what is more alarming is that nearly 70 to 92% are not able to express this due to surrounding social stigma and lack of infrastructure for treatment. This reality became strikingly evident to me in 2021 when my cousin's diagnosis of schizophrenia came to light. Witnessing the constant medication and institutionalization of a loved one, I first became painfully aware of how mental illness leaves behind a huge legacy, not just for the person suffering it but for those around them. Having lived in India all my childhood and most of my adult life, I have noticed that new technologies take time to be introduced to the Indian market. There is a dire need, especially in medical care, to enable these technologies to come to market faster than they currently do, in places like rural India. To this, I believe, I can contribute greatly by playing my part and applying my skills in circuit design, computer architecture design, machine learning and entrepreneurship for the development of biomedical electronic brain-machine interfaces (BMI). I aspire to accomplish this by developing innovative solutions that address neural ailments and can greatly improve the lives of individuals through neuroelectronic therapy and neural prostheses.

I believe that closed-loop BMIs are a promising device that can, not only help develop neural prosthesis using bioelectronic interfaces, but help us better understand human cognition and the underlying causes to mental issues like depression, addiction and anxiety. These BMIs with on-chip processing of iEEG and LFP signals from multi-site electrical recordings target the residual nerves or central nervous system of neurologically challenged individuals. Prior research has shown that, we can restore lost abilities[2,3,4], perception[5], treat neural ailments[6,7,8] and even enhance cognition[6, 9] through the ‘intelligent’ closed-loop BMIs. However, the complex nature of machine learning algorithms poses a critical tradeoff: such as, choosing the complexity and inexplainability of neural networks compared against the reduced accuracy of statistical inference methods (SVM, Bayesian Models); and which architectures for classification can achieve hardware efficiency? [10, 11] Such are the questions that are required to be answered and this is where I find an avenue to contribute. Looking at the larger picture, I find a gap in the systematic approach to accelerate the development time for BMI chip design, simulation, validation, and prototyping. We can automate this through Design Space Exploration (DSE) through genetic algorithms[12, 13], simulated annealing[14], bayesian optimization[15], and deep reinforcement learning[16, 17] which are just some of the major avenues for research. Moving forward, developing closed-loop brain machine interfaces with pareto-optimal configuration for performance, reliability, scalability and ‘online’ programmability would embody just a few of the key metrics that would enable the wider adoption of implantable neural and neuroprosthetic devices.

My education and research experience to date have given me a strong basis with which to pursue higher studies. I have focused my career on taking on advanced projects at CERN, TU Delft and UC Berkeley in digital IC design, signal processing, physics, and in computer architecture and machine learning system design. Given my sound understanding of the subject matter, I was a teaching assistant for two of the digital design courses at TU Delft’s Microelectronics and the Computer Engineering Lab, respectively while working, in parallel, on my Master Thesis at the intersection of the two. This allowed me to learn skills in both, circuit design and fabrication of CMOS integrated circuits. Further on, my responsibilities at my current role at CERN exposed me to implementing fault-tolerant digital design on system-on-chip (SoC) for the CROME radiation detectors. We successfully implemented and tested these detectors not only at the LHC particle accelerator but also at CHUV Hospital in Lausanne for applications in Flash (Radiation) Therapy for Cancer Treatment. My research at CERN included implementing complex signal processing algorithms on Zynq SoC, emulating its future ASIC design, and development of embedded drivers, FPGA firmware and writing kernel modules for the CROME systems. The wide-ranging applications and the safety-critical nature of the project allowed me to develop skills in writing fault-tolerant HDL, C/C++ and Python code for our applications, develop extensive formal and UVM verification environments, and further develop standalone test PCBs for front-end readout.

I see my objective to prepare myself for the long-term goal of becoming a scientist, an innovator, and an entrepreneur in the high-tech domain to enable access of medical technology and education to even the most remote parts of the world. In the pursuit of this quest, I have always adopted a rigorous approach to attain an in-depth

understanding of my fundamentals, and learn by experimenting with the most advanced technologies I was able to get my hands on. During my undergraduate studies, I learnt the numerous communication protocols such as I2C, UART, SPI etc. and applied the same on ATMega and ARM32 for the development of aerospace avionics for competitions by Lockheed Martin and NASA, both of which received the best rank at the international stage. I further learnt to implement signal processing (data-compression) and SERDES to the SFP transmission protocol during my internships at BARC and CERN nuclear research facilities, respectively. In 2020, I was working with the ATLAS Computational and X-Ray Physics team, when I first learnt about BMIs owing to my colleague Mohd. Meraj Ghanbari working at Muller Lab at UC Berkeley. The sheer size and complexity of the integrated circuit[18] impressed me the most and immediately drew my attention towards thinking about its integration as an edge ASIC. In time, I have developed multiple ASIC emulations of (RISC-V) microarchitectures on FPGA[19] for performance, area and power. And I'm currently a founding member and developer in the NeurX IP design project which is a demonstrator project for an FPGA-based neural signal processor based on the 2021 research from HHMI[4]. As an electronics engineer, I have always discovered the power wall[20] to be the principal factor challenging the development of future edge computing systems. This is true for general computing, and more importantly, the intracranial integrated circuits put this to test at an even tougher compliance standard where stringent energy and area constraints on multi-channel neural implants with on-chip feature extraction and signal classification are a critical element of the closed-loop BMI[10,11,21].

Having gained considerable experience in algorithmics and computer architecture, I am now looking to advance my career as a microelectronics design engineer with a focus on ultralow power design for Neural Integrated Circuits. For that I realize that I need to deepen my understanding of the practical DRC-compliant implementation aspects involved in creating custom and semi-custom ASICs and invent better ways to accelerate their design and development time. Therefore, at EPFL I aspire to join the machine learning and microelectronics design effort at the Integrated Neurotechnologies Laboratory (INL) to work under Dr. Mahsa Shoaran to elucidate the study of neural pathways by designing, validating and testing computational units of neural integrated circuits for application in neural coding and neural prosthesis. By designing machine learning algorithms embedded on integrated circuits we can probe high-dimensional data efficiently to extract useful information for analytical, prosthetic and therapeutic applications of BMIs. I am particularly interested in applying principles of ultra-low power circuit design (voltage scaling, clock gating, power gating, electromigration (di/dt) analysis, DVFS/AVFS etc.)[22] and DSE/Datapath optimization (resource sharing, model compression, network pruning, Vector/Systolic Array, and I, O or Weight stationary architectures etc.)[23] and scaling the number of input channels of the application-specific core. As a doctoral student, I aim to pursue the end-to-end development of a system-on-chip – ranging from theoretical consideration of machine learning algorithms to quantify the distinguishable parameters for hardware efficiency (such as metrics for parallelization, resource utilization, programmability, and performance prediction[24, 25]), to the practical implementation in the form of tape-out of the ASIC.

Campus Biotech stands at the forefront of human brain research and its microelectronics facilities holds the status of a highly reputed for enabling the development of groundbreaking integrated systems and the investigation of advanced CMOS scaling. Here I would further receive an excellent platform and guidance from neuroscientific experts, microelectronics colleagues and computer scientists to learn advanced concepts in neural interfaces and beyond CMOS technologies. Microelectronics Engineering, being the challenging endeavor it is, requires creativity, practice, and experience; and after working for nearly three years in industry I believe I am prepared and highly driven to pursue a doctoral program to master this craft and become a leader in bringing new semiconductor technologies to the society. I realize this is an ambitious goal and for that, I am willing to make the personal sacrifices of time, leisure, and immediate reward and dedicate the next four years to specialize under experts and esteemed faculty members at your institute. In return, I shall receive the greater personal rewards of intellectual satisfaction of learning and discovery, the gratification of being able to make countless lives better through my research on neural coding, and becoming a contributor to knowledge through my research. I believe that my holistic education, mathematical maturity, perseverance, and research experience has equipped me well to embark on this arduous journey and make significant original contributions to ongoing research. And it is with these objectives in mind, I hereby, submit my Ph.D. application for your consideration.

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