RISC-V: The Open Era of Computing

Calista Redmond
CEO, RISC-V International

Our world is shaped

- through positive inventions and negative disruptions
- through advances in technology and new business models
- through economic and political setbacks

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Reshaping history
is about removing barriers,
coming together, and
taking a united approach
RISC-V

RISC-V is the free and open Instruction Set Architecture...

- ... Driven through open collaboration
- ... Enabling freedom of design across all domains and industries
- ... Cementing the strategic foundation of semiconductors

Disruptive **Technology**

Barriers	Legacy ISA	RISC-V ISA
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions, open and proprietary cores
Software ecosystem	Extensive	Growing rapidly

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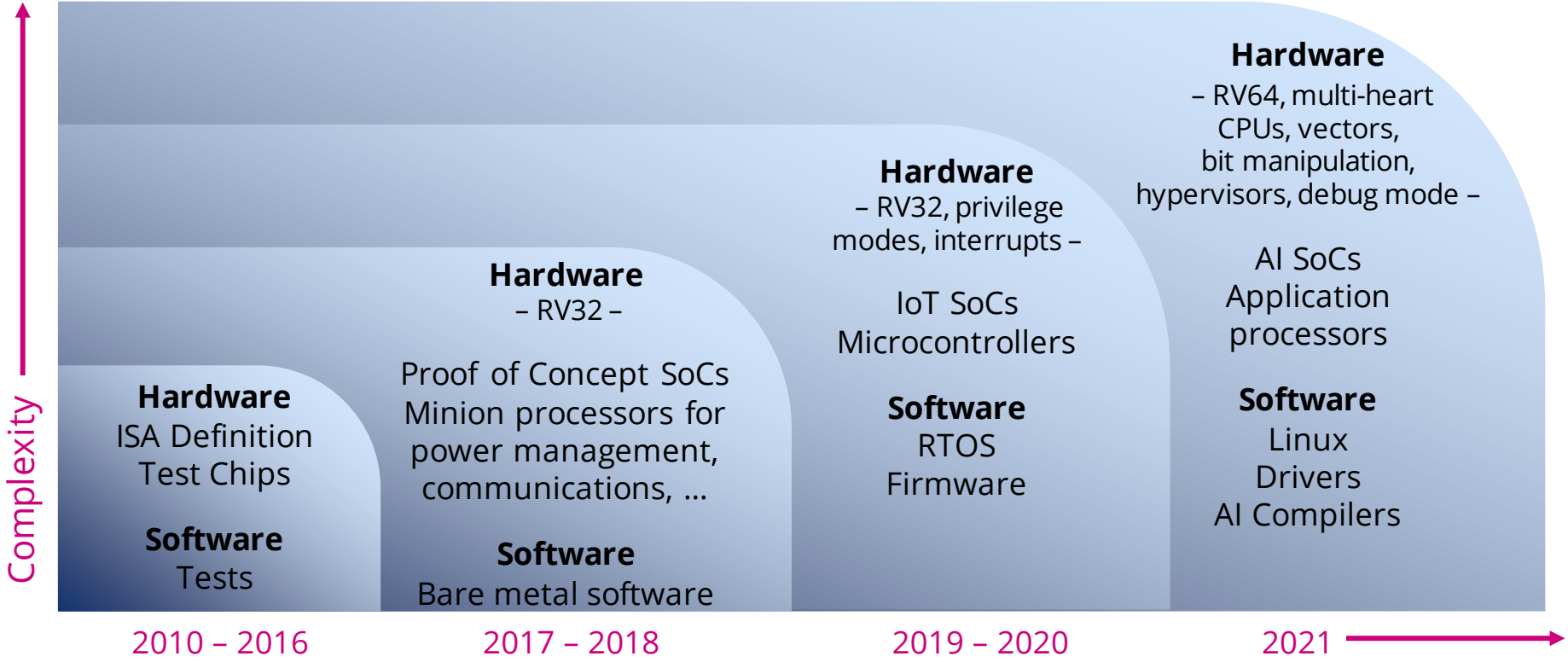
Industry innovation on RISC-V



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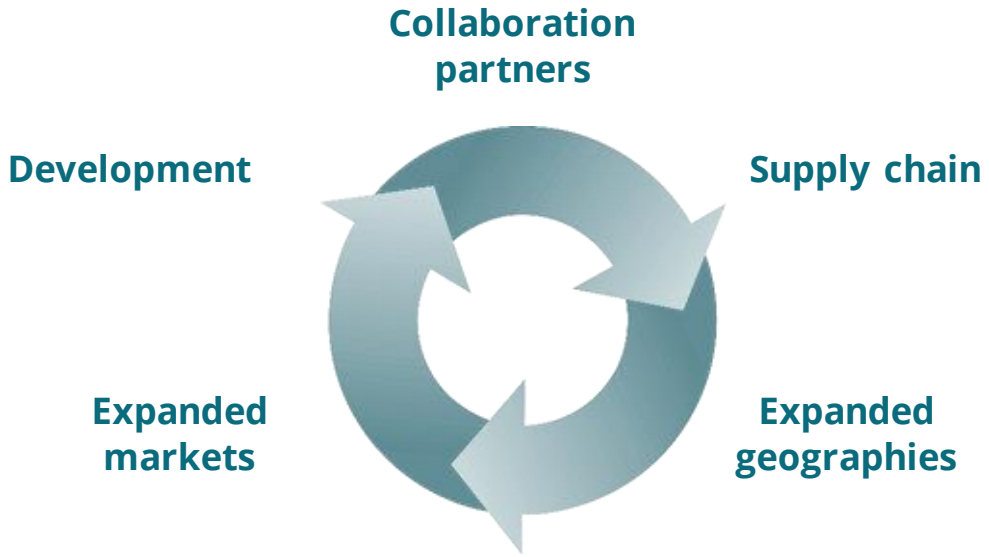
Unconstrained **Opportunity**

Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

RISC-V Business Model



Beyond removing barriers, RISC-V fuels our community to seize growing opportunities

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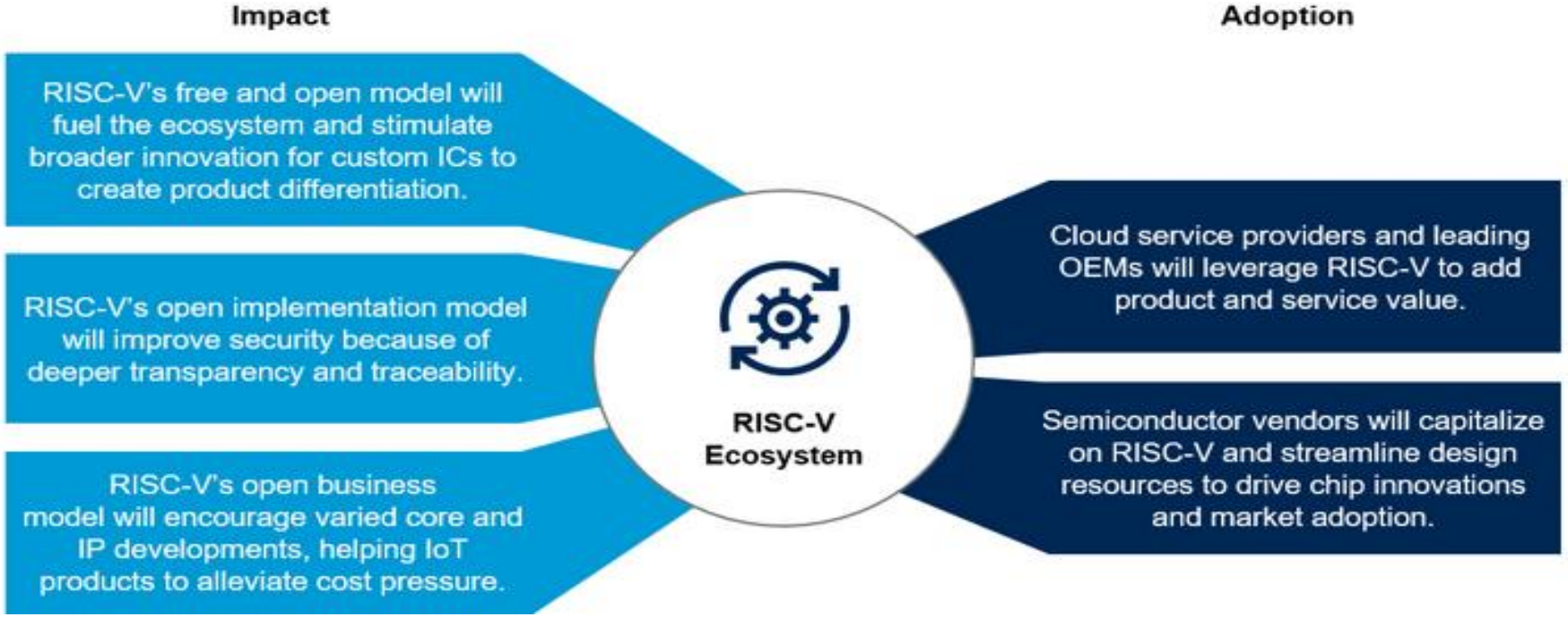
By 2025, 40% of application-specific integrated circuits (ASICs) will be designed by OEMs, up from around 30% today.

Custom ICs Based on RISC-V Will Enable Cost-Effective IoT Product Differentiation

Gartner, June 2020

Source: Gartner

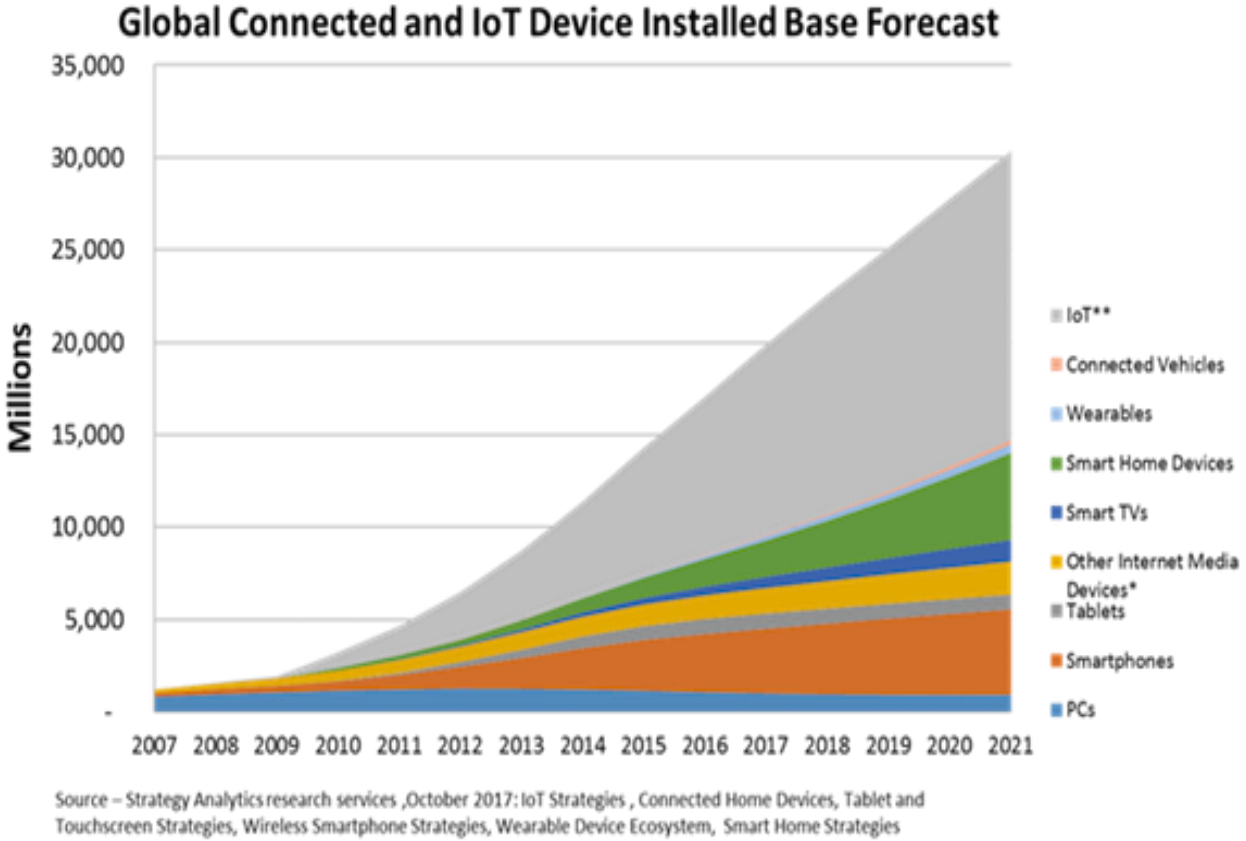
RISC-V's open model will spur adoption by cloud service providers and streamline resources for chip vendors



Source: Gartner
ID: 46523_C

30 billion connected and IoT devices

demand security and custom processors



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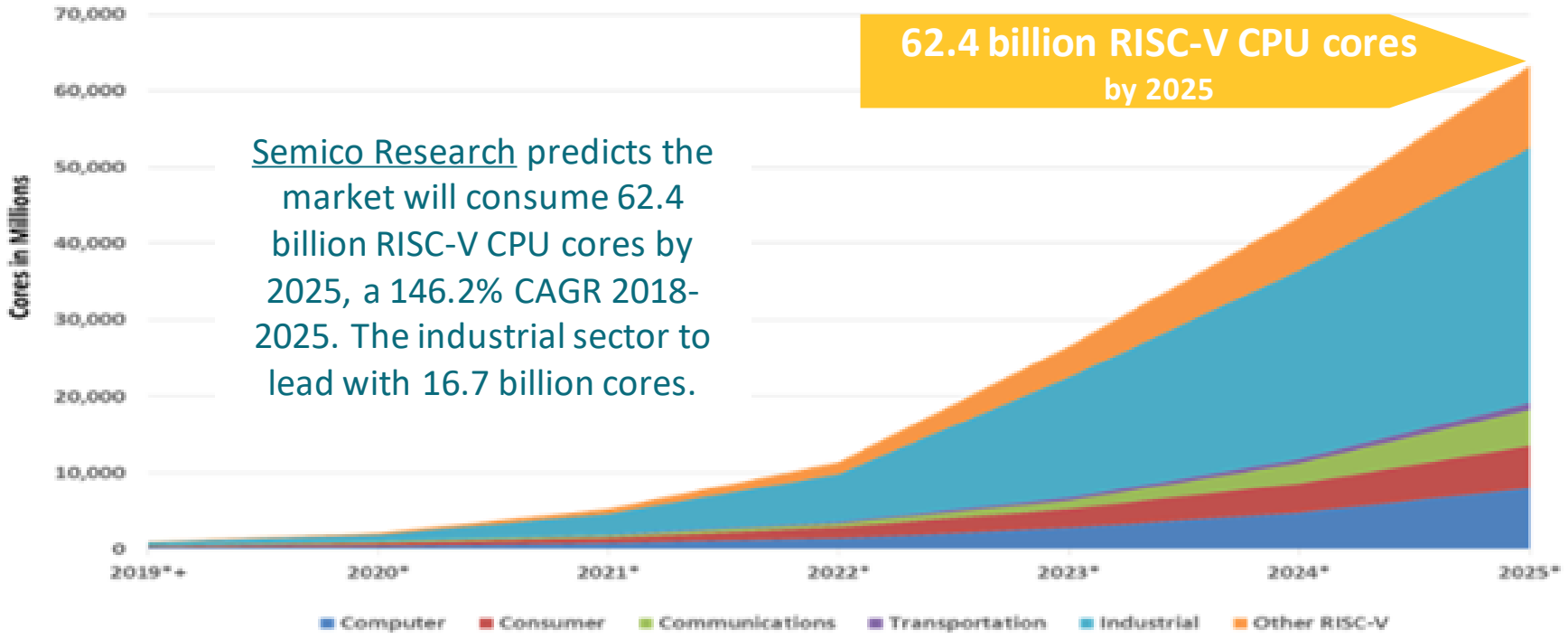
Source: Strategy Analytics

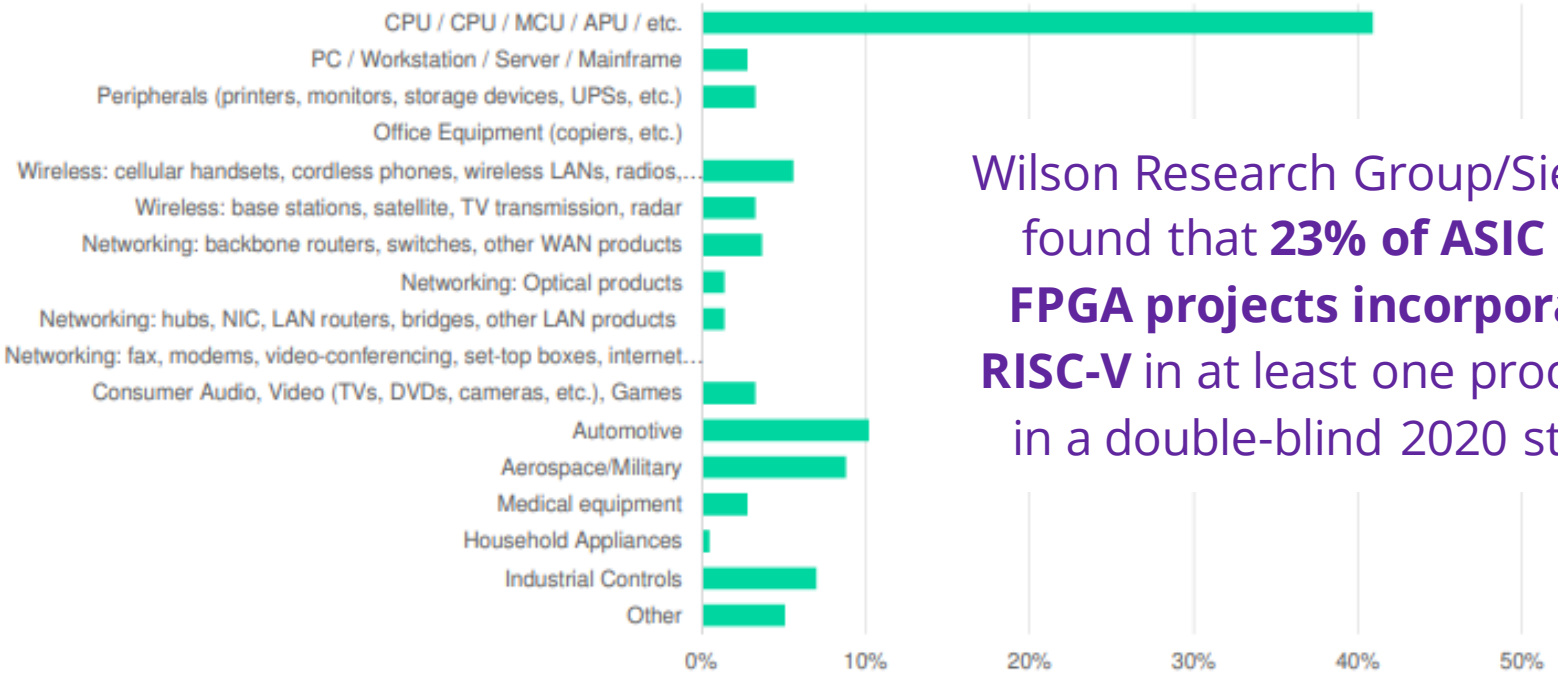
Rapid RISC-V growth led by industrial



Source: Semico Research Corp

Nearly a quarter of designs incorporate RISC-V

Projects Incorporating RISC-V by Market Segment



Wilson Research Group/Siemens found that **23% of ASIC and FPGA projects incorporated RISC-V** in at least one processor in a double-blind 2020 study.

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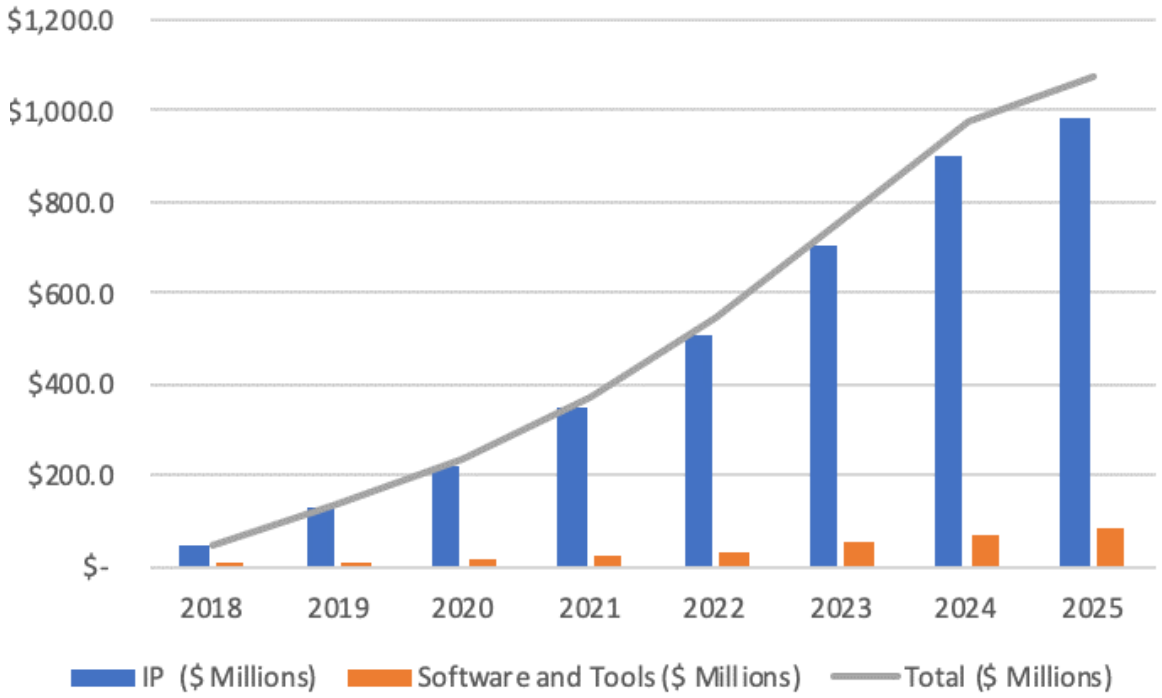
RISC-V IP, SW, and Tools build momentum

The total market for RISC-V IP and Software is expected to grow to $1.07 billion by 2025 at a CAGR of 54.1%



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Source: Tractica

RISC-V adoption spans industries and workloads

Cloud and data center
top providers like Amazon and Alibaba are designing their own chips.

Automotive
is transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.

Industrial IoT
incorporating artificial intelligence in manufacturing and industrial processes.

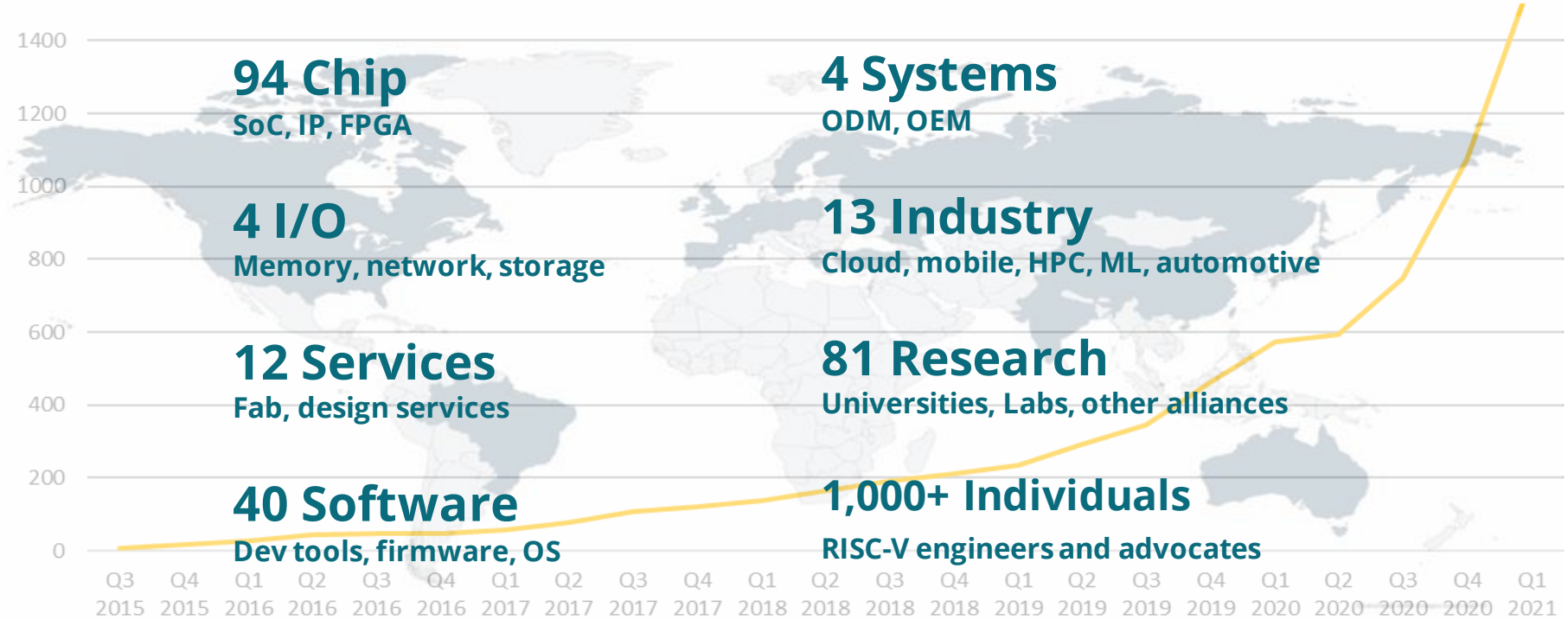
Mobile and wireless
continue rapid evolution with each generation of hardware and increased capability.

Consumer and IoT devices
bring incredible innovation and volume with billions of connected devices in the next 5-10 years.

Memory
was largest semiconductor category by sales with $158 billion in 2018, and the fastest-growing.

More than 1,500 RISC-V Members

across 70 Countries



94 Chip
SoC, IP, FPGA

4 I/O
Memory, network, storage

12 Services
Fab, design services

40 Software
Dev tools, firmware, OS

4 Systems
ODM, OEM

13 Industry
Cloud, mobile, HPC, ML, automotive

81 Research
Universities, Labs, other alliances

1,000+ Individuals
RISC-V engineers and advocates

In 2020, RISC-V membership grew 133%

Dedicated Community

Services Fab, design services

I/O Memory, network, storage

Software Dev tools, firmware, OS

Press and Analysts

Chip SoC, IP, FPGA

Universities and Research

Industry cloud, mobile, HPC, ML, automotive

Investors and Funding sources

Individual Advocates

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Incredible industry progress

- The European Processor Initiative finalized the first version of its **RISC-V accelerator architecture** and will deliver test chip in 2021.
- The RIOS Lab announced PicoRio, an affordable **RISC-V open source small-board computer** available in 2021.
- Imperas announced first **RISC-V verification reference model with UVM encapsulation**.
- Seagate announced **hard disk drive controller** with high-performance RISC-V CPU.
- GreenWaves **ultra-low power GAP9 hearables platform** enabling scene-aware and neural network-based noise reduction.
- Alibaba unveiled RV64GCV core in its Xuantie 910 processor for **cloud and edge servers**.
- Microchip released the first **SoC FPGA development kit** based on the RISC-V ISA.
- Andes released **superscalar multicore and L2 cache controller** processors.
- StarFive released the world's first **RISC-V AI visual processing platform**
- SiFive unveiled world's fastest development board for **RISC-V Personal Computers**.
- Micro Magic announced an incredibly **fast 64-bit RISC-V core** achieving 5GHz and 13,000 CoreMarks at 1.1V.

RISC-V is the foundation of the open era of computing

- **3,000+ individuals in 60+ RISC-V work groups** and committees
- **312 RISC-V solutions** online including cores, SoCs, software, tools and developer boards.
- **31 local RISC-V community** groups, with more than **5,700 engineers**
- We're in the news! We have **34k+ followers on social media** and so far this year, we have participated in **150+ news articles** along with amplifying RISC-V community news.

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Engaging the community in work that matters

- We are defining Profiles to standardize a set of instructions and state.
  - If an implementer then they should be able to run the same instructions on multiple implementations and get the same results.
  - The initial Profiles are RVA20 and RVM20 for extensions ratified in 2019 and RVA22 and RVM22 for extensions ratified in 2021 including vector, crypto scalar, and bit manipulation.
- We are defining Platforms to be a standard set of features for a complete execution environment (like Linux or FreeRTOS).
  - If you adhere to a Platform then you should be able to run the same executable on 2 different platforms and get the same results (excluding timing differences, etc.)
  - Platforms will include things like Profiles, Device tree, ABIs, etc.
- 2021 holds an exciting set of new extensions for vector processing, cryptography, bit manipulation, packed decimal, trusted execution environment, virtual memory, and more enabling sectors and industries from embedded to ML to HPC and everything in between.
- In addition, we are revamping our documentation with a new look, fully adopting AsciiDoc, enhancing the specifications with glossaries and indexes, and common formal diagram insertion.
- We have a number of programs underway
  - RISC-V Development Partners - institutions (CAS, RIOS, IITM) help develop ecosystem software for extensions
  - RISC-V Labs - institutions build labs with RISC-V based board and servers to both run regression testing and to provide the community with an area to sandbox
  - RISC-V Seed program - seed 1000 boards to academia and early adopters by June 2022
  - Joint working group on Coherence between Chips Alliance and RISC-V

Technical Deliverables

Guard against fragmentation
Build technical deliverables
Work groups

Compliance + Verification

Testing and compliance suites
Compliance tests

Visibility

Constant drumbeat through press, media, and original content
Industry and regional events
Dedicated RISC-V events

Learning + Talent

Multi-level online learning
Connecting universities with labs, tests, and curricula
RISC-V Training Partners

Advocacy

Technical advocate program
Local developer groups and events
RISC-V Ambassadors
Geo and industry alliances

Marketplace Exchange

Online marketplace of providers, products, and services
Technical developer forums

RISC-V delivers incredible member support

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RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement

Build RISC-V into your company strategy, and your personal mission

"**The future of American industry depends on open source tech**, … RISC-V is gaining traction in the hardware manufacturing space throughout the world, because it lowers barriers to entry and increases chip development speed."

-- Wired

"Though the architecture was created a decade ago by university professors, **RISC-V has been building its ecosystem for years and has started to hit its stride** with big licensees like Western Digital, SiFive, and even NVIDIA itself."

-- VentureBeat

"If it succeeds, RISC-V could lower the cost of developing a new chip and help **companies of all sizes to build exactly the processors they need**."

-- Engadget

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Thank you

www.riscv.org

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@Calista_Redmond

risc-v-international

calistaredmond

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Benefit of joining RISC-V

- ✓ **Accelerate technical traction** and insight
- ✓ **Contribute** technical priorities, approaches, and code
- ✓ Gain strategic and **technical advantage**
- ✓ **Increase visibility**, leadership, and market insight
- ✓ Fill and increase **engineering skills**, retain and attract talent
- ✓ Build **innovation partner** network and customer pipeline
- ✓ **Deepen, engage, and lead** in local and industry developer network
- ✓ **Showcase RISC-V products**, services, training, and resources

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Membership options

Premier Member Benefits

- Community level benefits plus…
- Use of RISC-V Trademark for commercialization
- Board seat and Technical Steering Committee seat included for $250k level
- Technical Steering Committee seat included for $100k level
- Solution listing on RISC-V Exchange
- 4 case studies a year, 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Inclusion in event promotions

Strategic Member Benefits

- Community level benefits plus…
- Use of RISC-V Trademark for commercialization
- 3 Board reps elected for tier, includes Premier members that do not otherwise have a board seat.
- May lead workgroup and/or committee
- Solution listing on RISC-V Exchange
- 1 case study a year, 1 blog per month
- 1 social media spotlight per month

Community Member Benefits

- Accelerated development, reduced risk through open source, ratified ISA.
- May participate in workgroups, influence strategy and adoption
- 6 support programs in Technical Deliverables, Compliance, Visibility, Learning, Advocacy, and Marketplace
- 1 voting Academic Board rep,
- 1 non-voting Community Board rep
- Member listing on RISC-V website
- Event registration discount

Premier Member Requirements

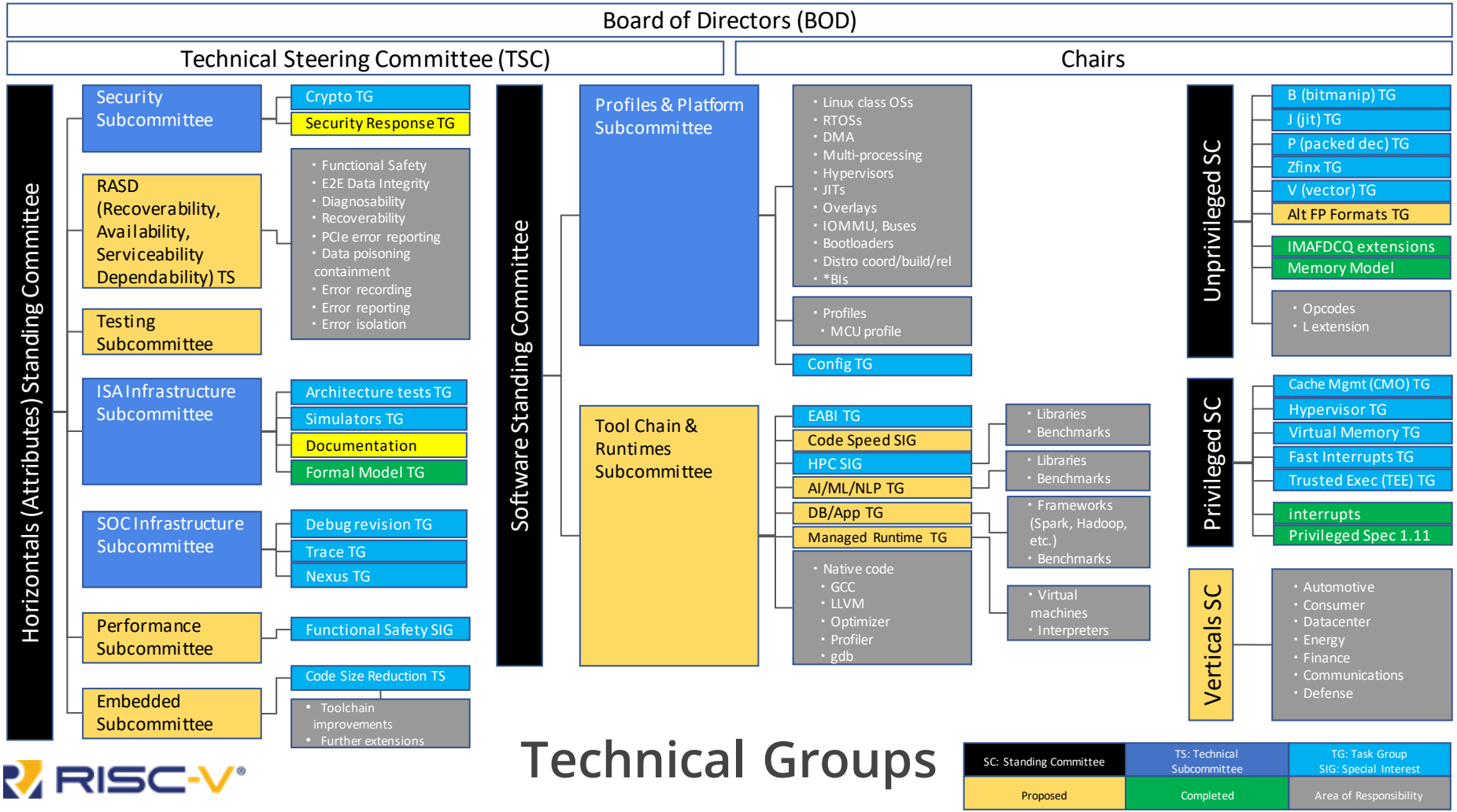
- Membership open to any type of legal entity, not open to individual members
- $250k Annual membership includes Board seat and Technical Steering Committee seat
- $100k Annual membership includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity, not open to individual members
- Annual membership based on employee size
  - $35k for 5,000+ employees
  - $15k for 500-5,000 employees
  - $5k for <500 employees
  - $2.5k for <10 employees / company <2 years old

Community Member Requirements

- Membership open to academic institutions, non-profits, and individuals not representing a legal entity
- No annual membership fee


Board of Directors (BOD)
Technical Steering Committee (TSC)
Chairs
Horizontals (Attributes) Standing Committee
Security Subcommittee
Crypto TG
Security Response TG
RASD (Recoverability, Availability, Serviceability Dependability) TS
Functional Safety
E2E Data Integrity
Diagnosability
Recoverability
PCIe error reporting
Data poisoning containment
Error recording
Error reporting
Error isolation
Testing Subcommittee
ISA Infrastructure Subcommittee
Architecture tests TG
Simulators TG
Documentation
Formal Model TG
SOC Infrastructure Subcommittee
Debug revision TG
Trace TG
Nexus TG
Performance Subcommittee
Functional Safety SIG
Embedded Subcommittee
Code Size Reduction TS
Toolchain improvements
Further extensions
Software Standing Committee
Profiles & Platform Subcommittee
Linux class OSs
RTOSs
DMA
Multi-processing
Hypervisors
JITs
Overlays
IOMMU, Buses
Bootloaders
Distro coord/build/rel
*BIs
Profiles
MCU profile
Config TG
Tool Chain & Runtimes Subcommittee
EABI TG
Code Speed SIG
HPC SIG
AI/ML/NLP TG
DB/App TG
Managed Runtime TG
Native code
GCC
LLVM
Optimizer
Profiler
gdb
Libraries
Benchmarks
Libraries
Benchmarks
Frameworks (Spark, Hadoop, etc.)
Benchmarks
Virtual machines
Interpreters
Unprivileged SC
B (bitmanip) TG
J (jit) TG
P (packed dec) TG
Zfinx TG
V (vector) TG
Alt FP Formats TG
IMAFDCQ extensions
Memory Model
Opcodes
L extension
Privileged SC
Cache Mgmt (CMO) TG
Hypervisor TG
Virtual Memory TG
Fast Interrupts TG
Trusted Exec (TEE) TG
interrupts
Privileged Spec 1.11
Verticals SC
Automotive
Consumer
Datacenter
Energy
Finance
Communications
Defense
Technical Groups
SC: Standing Committee
TS: Technical Subcommittee
TG: Task Group
SIG: Special Interest
Proposed
Completed
Area of Responsibility

- **RISC-V Technical Steering Committee** to govern technical strategy, build technical leadership and best practice decision-making
- **RISC-V Learn** encompassing university curricula, online learning and Training Partners
- **RISC-V Ambassadors and Alliances** to reach beyond our community for industry collaboration, leadership, and technical engagement.
- **RISC-V Exchange** to showcase RISC-V cores, SoCs, developer boards, software, tools and other resources.

From Embedded to Enterprise

- The EU Horizon 2020 **De-RISC platform for aerospace** has achieved several hardware and software milestones since it began a year ago.
- The School of Computing at the Tokyo Institute of Technology developed a portable Linux **RISC-V SoC design in just 5,000 lines of Verilog**.
- Huami released a new RISC-V based **AI chip for biometric wearables**
- CHIPS Alliance announced enhancements to the RISC-V SweRV Core EH2, the world's first **dual-threaded, commercial, embedded RISC-V core** and SweRV Core EL2, an **ultra-small, ultra-low-power RISC-V core**.
- Alibaba unveiled its RISC-V RV64GCV core that will be used for its Xuantie 910 processor aimed at **cloud and edge servers**.

April 22-23, 2021
9am - 17pm Japan Standard Time

Free Registration
Program
Slack: risc-v-association.slack.com

SiFive and Andes who are leading RISC-V IP products. DTS-Insight, a descendent of a part of Yokokawa Electric, is presenting their RISC-V system solution capabilities both in hardware and software. Espressif, presents their new RISC-V based WiFi BTLE chip. Synopsis presents RISC-V based AI accelerator. Effinix, an FPGA startup, is presenting their RISC-V solutions in their FPGA product. GigaDevice is presenting their award-winning flash microcontrollers. Syntacore is presenting their open-source and commercial RISC-V solutions. Cloudbear is presenting the use case of their RISC-V processor IP.

In the meanwhile, here in Japan, Renesas Electronics Corporation announced the adoption of RISC-V. Japanese researchers and companies are beginning to lead in software and hardware architectural research in RISC-V security.

Google is promoting open source EDA tools, open source process development kits (PDK), open source free shuttles. We see corresponding contributors in Japan who are presenting.