RISC-V: A Brief History

Saroj Rout, *Senior Member, IEEE*

***Abstract*—This article briefly introduces the history behind the rise and popularity of the RISC-V instruction set architecture (ISA). It starts with a design of a microcontroller and how RISC-V fits into it. Then it briefly covers the history of microprocessor and emergence of RISC ISA and finally the opensource ISA, RISC-V.**

***Index Terms*—RISC-V, RISC, Computer Architecture**

I. Introduction

SYSTEMS-ON-A-CHIP (SoC) with integrated processors are becoming ubiquitous. One such SoC is a microcontroller. It is hard to find a electronic system without a microcontroller in it eg. IoT, appliances, watches, toys and so on. They vary in complexity depending on the target applications. For example, Atmel's ATtiny series of microcontrollers are 8-bit processors starting with just 512-Bytes Flash and 32-Bytes of SRAM running at 10 MHz clock speed. On the other end of the spectrum are the STMicroelectronic's popular STM32 series microcontrollers which is based on Arm's Cortex-M 32-bit processor with up to 128kB of L2 cache and and more than 600-kB of SRAM running at 650 MHz.

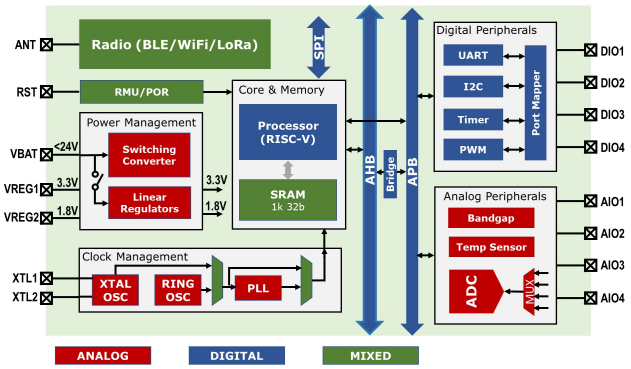

Fig. 1. Microcontroller for a IoT node

Fig. 1 shows an architecture of a microcontroller intended for IoT wireless nodes. It contains a core processor, a cache (SRAM), analog peripherals (bandgap voltage reference, temperature sensor and analog-to-digital converter(ADC)), digital peripherals (UART, SPI, PWM), power management, clock management (PLL, crystal oscillator), and RF Radio (Bluetooth, WiFi, LoRa). Apart from the processor, all other blocks (typically called IPs) can either be designed from scratch by mixed-signal engineers or licensed from a vendor. When it comes to the processor, it gets a little complicated. You can use a very old instruction set architecture (ISA) and implement it in your target technology. One such popular ISA is Intel's 8051 microcontroller architecture developed in 1980s. It has been around for several decades and has proven to be reliable, efficient, and versatile. Its compact size, low power consumption, and wide range of peripherals make it a popular choice for many embedded systems applications. Additionally, there is a large community of developers and engineers who are familiar with the 8051 architecture, which makes it easier to find support and resources for development.

Companies like Arm, IBM and Intel have very successful ISAs but patents on key aspects of their ISAs prevent others from using them without licenses which imposes a prohibitive cost for most educational, research organization or companies trying to target low-volume markets. Note, ISA is neither an implementation of the hardware or the software (OS, drivers, compilers). It is a standardization of the interface specification so development tools and design implementations can be reused and shared provided they are open and free. And, both hardware and software can be implemented in three ways: proprietary, licensed open-source, or free open-source.

There are three free and open-source RISC ISAs currently available for use:

1) *SPARC V8* from Sun Microsystems that was made into a IEEE standard in 1994.
2) *OpenRISC* is a GNU open-source effort started in 2000, with the 64-bit ISA being completed in 2011.
3) *RISC-V* (pronounced "RISC 5") a BSD open-source effort started in 2010 at University of California at Berkeley by Krste Asanović, David A. Patterson and their graduate students Andrew Waterman and Yunsup Lee partly inspired by ARM's IP restrictions together with the lack of 64-bit addresses and overall baroqueness of ARM v7.

Before we look at the history of RISC-V and why it prospored compared to it's predecessors SPARC V8 and OpenRISC, it's worth taking a quick look at the history of microprocessors and how RISC has emerged as the goto architecture for power-conscious devices such as tablets, mobile phones and embedded systems.

II. Brief History of Microprocessors

I wish you the best of success.

mds
August 26, 2015

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III. Conclusion

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APPENDIX A
PROOF OF THE FIRST ZONKLAR EQUATION

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APPENDIX B

Appendix two text goes here.

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The authors would like to thank...

REFERENCES

[1] H. Kopka and P. W. Daly, *A Guide to LaTeX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.

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Michael Shell Biography text here.

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