Machine Learning in Analog IC Design Automation

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Abstract

Generative AI has already made a significant impact on software, and its use in digital hardware design is nearing mainstream adoption. However, its application in analog circuit design remains in its early stages. In this tutorial, we will start with a simple yet widely used analog circuit, a low-power operational transconductance amplifier (OTA) to highlight the complexities involved in this area. Next, we will explore key research and recent advancements in applying Machine Learning (ML) to analog circuit design and automation. We will also demonstrate the use of the well-known Berkeley Analog Generator (BAG), a popular tool for analog circuit generation. Finally, we will introduce AiEDA, a cutting-edge agentic AI methodology designed to automate analog circuit design. This approach uses large language models (LLMs), agentic AI techniques, and open-source EDA tools to create Large Action Models (LAMs), which aim to improve efficiency and accuracy in analog circuit design processes.

Topic : AI for Electronic Design Automation

Area of the Tutorial : Analog IC Design, Generative Artificial Intelligence (GenAI), Machine Learning (ML), Integrated Circuit (IC) Design, Electronic Design Automation (EDA).

Keywords : Analog IC Design, GenAI, EDA, Machine Learning (ML).

Target Audience

- Analog IC designers interested in using GenAI for circuit and layout synthesis.
- EDA tool developers and researchers working in the area of Analog synthesis and GenAI.
- System-on-Chip (SoC) architects interested in integrating GenAI in the design flow.

Learning Objective

VLSID International Conference is one of the foremost global forum for presentation of advances in VLSI and Embedded Systems. The conference is attended by over 2000 engineers, students & faculty, industry, academia, and researchers from around the world. This year's theme of VLSID is "Silicon meets Artificial Intelligence (AI)" which is an apt focus given AI has permeated every facets of life including every domain of VLSI as well.

When it comes to generative AI (GenAI), it's influence on software is well known now and digital hardware synthesis using GenAI is on the verge of becoming mainstream. But when it comes to analog design automation using GenAI, it is still in its infancy.

Outline of the Tutorial

In this tutorial, we will start with a simple and typical analog circuit—a low-power OTA—to demonstrate the complexity of the problem. Subsequently, we will explore the key research and innovations in analog circuit design and automation utilizing Machine Learning (ML). Next, we will demonstrate the use of a widely-utilized Berkeley Analog Generator (BAG) for analog circuit design. Finally, we will introduce AiEDA, a new agentic AI flow methodology that automates analog circuit design, utilizing large language models (LLM) combined with Retrieval Augmented Generation (RAG) technique.

Learning Outcomes

A semiconductor student, researcher, or professional unfamiliar with this specific topic will gain a general understanding of the issue and the latest advances in research and development. A designer of analog ICs seeking to incorporate ML into the design process will be introduced to two tools and methodologies to achieve this. A developer or researcher in EDA will gain an understanding of the present status of tools and methods for creating analog design automation tools using ML.

Prerequisite knowledge of the audience

This tutorial will cover the topics assuming minimum knowledge of the topic. Having said that, some experience in analog circuit design and a general knowledge how AI models work will definitely help the audience.

Lead Speaker

Saroj Rout, Ph.D., Senior Member IEEE

Biography Dr. Saroj Rout received the Ph.D. degree in Electrical Engineering from Tufts University, Massachusetts, USA, in 2016, where he worked on terahertz metamaterials for his doctoral dissertation. He received his B.Eng. in Instrumentation and M.Eng. in Microelectronics from Birla Institute of Technology and Science (BITS), Pilani, India, in 1996 and 1998, respectively. He is an Additional Professor of Electronics Engineering Dept. at Silicon University, India. He is the co-founder of Boston Microtechnology, a semiconductor startup in the Greater Boston area developing power management ICs. He has more than 25 years of experience in analog IC design with 16 complete SoC experience. Two of the products, DAA and ProSLIC, have sold more than 2 billion units. He holds 8 patents in the area of IC design and metamaterials. He is a published researcher with more than 450 engineering citations and the author of "Active Metamaterials", a Springer-Nature publication for applied physicists. He was the Principal Investigator, SBIR Phase-I, a National Science Foundation (NSF-USA), grant. He is a Senior Member of IEEE.

Analog IP/SoC Experience Direct access (DA) IPs for a HBM SoC in 14nm CMOS. • Power management IPs for a Spiking Neural Network (SNN) SoC in 28nm CMOS. • A transformer-less AC-DC converter in the 350V SOI CMOS process, • A SPI-accessible SRAM in 0.6μm CMOS for low-power IoT applications. • A Power and Area Efficient CMOS Bandgap Voltage Reference in 0.6μm CMOS. • Analog Front-End (AFE) for a 3-axis MEMS gyroscope SoC in 0.13 μm CMOS. • A focal-plane array for 320 GHz metamaterial based imager in 0.18 μm CMOS. • A 450 GHz metamaterial modulator using HEMTs in 0.5μm GaAs technology. • VGA-based Limiter for GSM/DCS EDGE PA SoC in 0.13 μm CMOS. • Baseband IPs for FM Radio Tuner SoC in 0.13μm CMOS. • Verilog-AMS modeling for a baseband IPs in a GSM SoC. • Analog IPs for Direct Access Arrangement(DAA): Transformer-less Modem SoC in 0.25μm CMOS + external bipolars. • LO IPs for a Digital Satelitte Radio Tuner SoC in 0.25μm CMOS. • Analog Front-End (AFE) IPs for a ProSLIC SoC, a complete analog telephone interface in 0.45μm CMOS + external bipolars.

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Co-Speaker

Arun Ravindran, Ph.D., Associate Professor, University of North Carolina at Charlotte, USA

Biography Dr. Arun Ravindran received his Ph.D. in Electrical Engineering from The Ohio State University, Columbus, OH, USA, in 2003. He received his M.Eng. in Microlectronics and B.Eng. in Instrumentation from Birla Institute of Technology, Pilani in 1996 and 1997 respectively. He is currently an Associate Professor of Electrical and Communication Engineering Department at the University of North Carolina at Charlotte, USA. Dr. Ravindran has over 20 years of experience in research and teaching in various domains, such as analog mixed signal design, high-performance computing, edge computing, deep learning, and generative AI. With more than 65 peer-reviewed journal and conference publications, his work has received funding from both the US National Science Foundation (NSF) and industry. Currently, his research and consulting interests focus on the foundational techniques and applications of generative AI.

AI Experience (2018 - 2023): Designed and implemented collaborators an edge-based distributed custom deep learning human-action detection and alerting system in the $2.2 million NSF project "SCC: Building Safe and Secure Communities through Real-Time Edge Video Analytics". • (2022 - 2024) Collaborated in designing and implementing a compute-efficient, edge-based deep learning vehicle tracking algorithm and its simulation framework for dense urban road networks. • (2023 - present) Currently implementing generative AI-based custom support chatbots for clients across various industries, including software, legal, and banking. • (2023 - present) Leading multiple research projects focused on fundamental generative AI decision-making, as well as its applications in VLSI design and cybersecurity.

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Please note that the details regarding each author's contribution to the tutorial are outlined in the section "Basic Structure of the Tutorial" below.

Basic Structure of the Tutorial

Speaker Legend

SR Saroj Rout

AR Arun Ravindran

Introduction A brief review of analog synthesis in general. **[SR][5min]**

Problem with analog synthesis In order to highlight why analog synthesis remains a challenging problem and hasn't yet become mainstream, we will utilize a straightforward and widely used analog circuit—a low-power OTA—designed using the g_m/I_D methodology. **[SR][10min]**

A review of analog synthesis using Machine Learning (ML) techniques We examine the impact of ML on analog EDA over the past ten years. Our focus will be on three key areas:

- **Neural Networks (NN)** of different complexities using both supervised and reinforcement learning techniques. **[AR][10min]**
- **Global optimization** strategies assisted by heuristic and stochastic methods include simulated annealing, genetic algorithms, Gaussian processes, Bayesian techniques, and particle swarm optimization. Although these are technically not ML techniques, they are potent optimization methods that can be incorporated within an ML framework. **[AR][10min]**
- **Hybrid** techniques that integrate global optimization with neural network methodologies to enhance results compared to pure optimization techniques. **[AR][10min]**

Berkeley Analog Generator (BAG) A well-known Python-based Analog and Mixed-Signal (AMS) circuit and layout generator developed by the University of California, Berkeley. Discuss the structure of BAG, now in it's 3rd version BAG3.0 and it's integration in Cadence Virtuoso front-end. Demonstrate the tool using the low-power OTA analog design. **[SR][20min]**

AiEDA our new agentic AI based design framework for hardware synthesis will be introduced.

- **Introduction to Agentic AI Flow** General architecture of the flow will be introduced and the power LLM when combined with Retrieval Augmented Generation (RAG) technique will be demonstrated. **[AR][10min]**
- **Case Study** we will demonstrate the generation and optimization of a low-power OTA—designed using the g_m/I_D methodology. **[SR][10min]**

Conclusion Concluding remarks along with future direction for AI-assisted analog circuit generation. **[SR][5min]**