Ιόνιο Πανεπιστήμιο – Τμήμα Πληροφορικής

Αρχιτεκτονική Υπολογιστών

2020-21

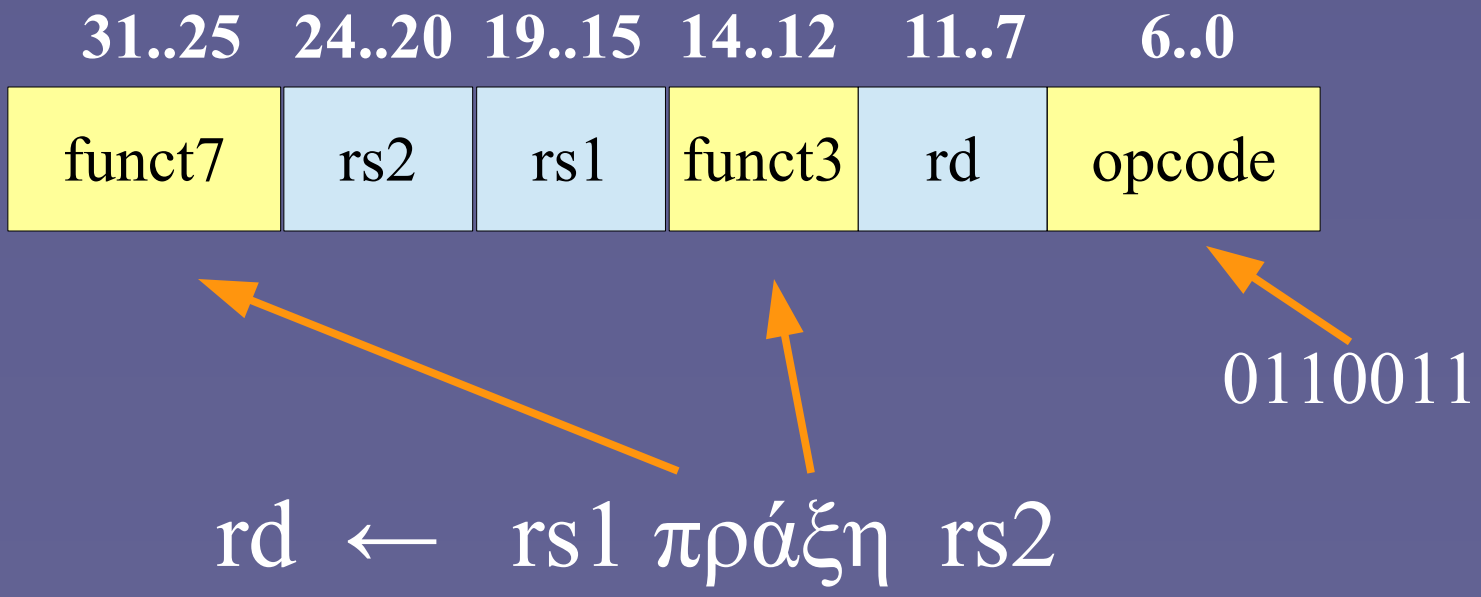
Παραδείγματα ISA

(η βασική 32-bit αρχιτεκτονική RISC-V)

http://mixstef.github.io/courses/comparch/

Μ.Στεφανιδάκης

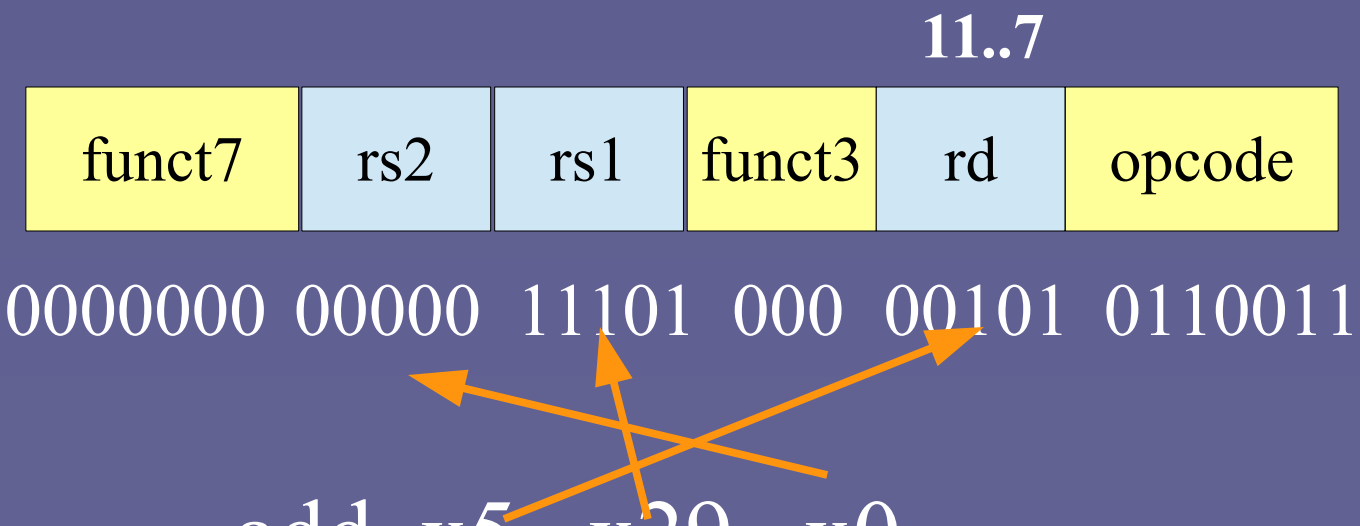
RISC-V RV32I R-type



Επιλογή πράξης

funct7	funct3	πράξη
0000000	000	ADD
0100000	000	SUB
0000000	001	SLL
0000000	010	SLT
0000000	011	SLTU
0000000	100	XOR
0000000	101	SRL
0100000	101	SRA
0000000	110	OR
0000000	111	AND

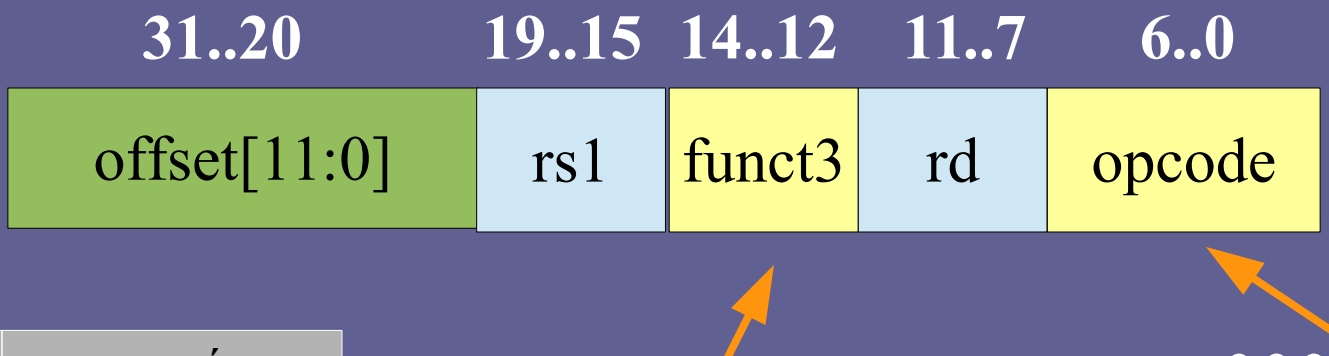
Παράδειγμα



add x5, x29, x0

bytes εντολής: 00 0E 82 B3

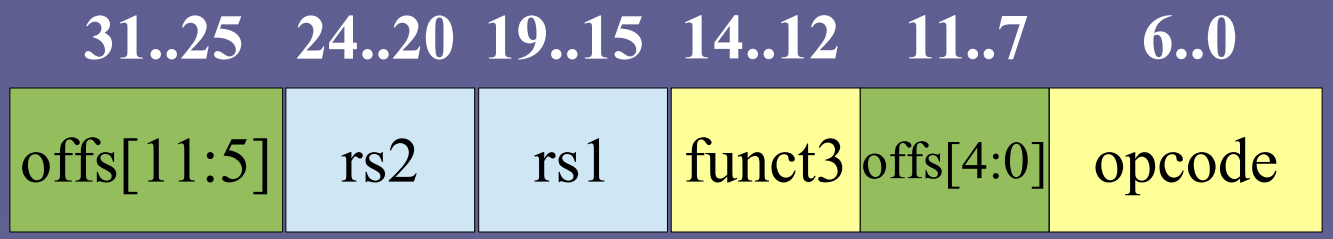
RISC-V RV32I Load



funct 3	μεταφορά
000	LB (8 bits)
001	LH (16 bits)
010	LW (32 bits)
100	LBU (8 bits)
101	LHU (16 bits)

$$rd \leftarrow mem[rs1 \pm offset]$$

RISC-V RV32I Store



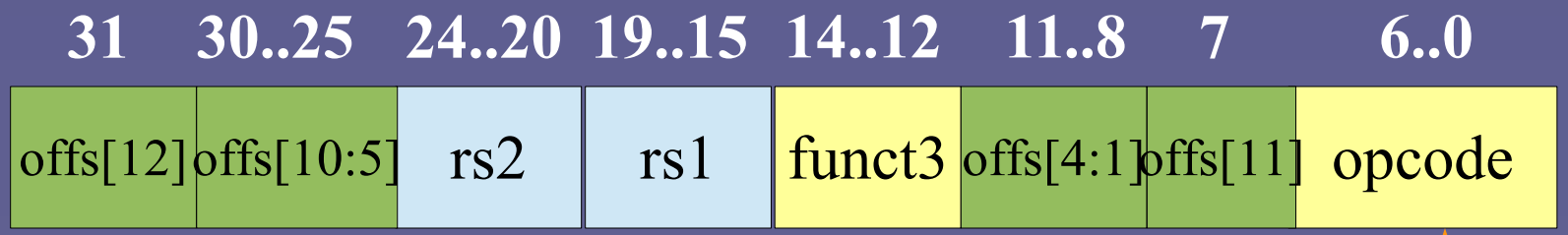
funct 3	μεταφορά
000	SB (8 bits)
001	SH (16 bits)
010	SW (32 bits)

εύρος μεταφοράς

0100011

rs2 → mem[rs1 ± offset]

RISC-V RV32I Branches



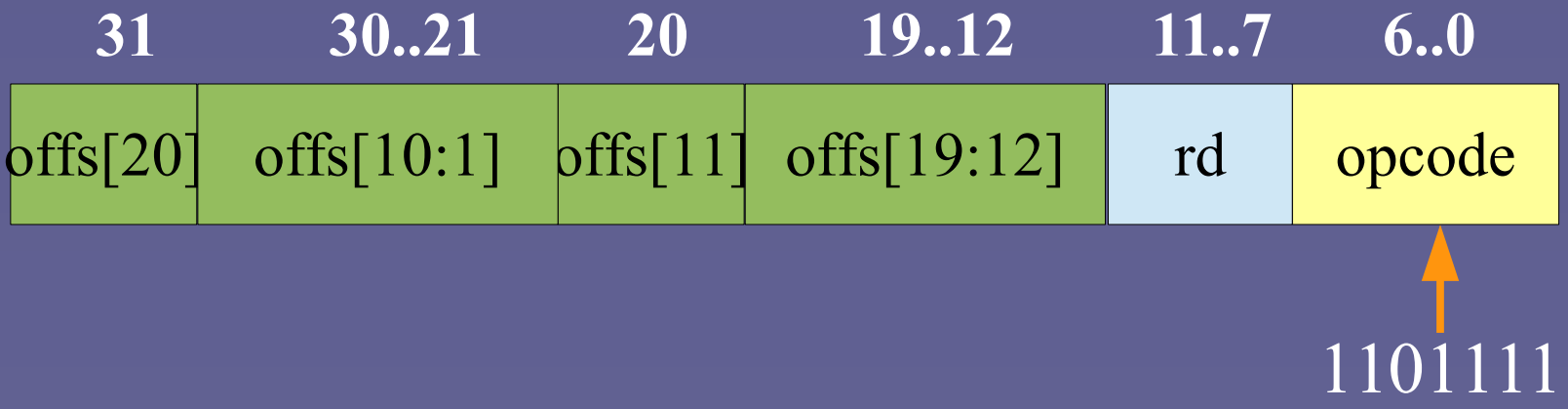
funct 3	σύγκριση (cmp)
000	BEQ (==)
001	BNE (!=)
100	BLT (<)
101	BGE (>=)
110	BLTU (<)
111	BGEU (>=)

είδος σύγκρισης

1100011

pc ← pc ± offset
if rs1 *cmp* rs2 is true

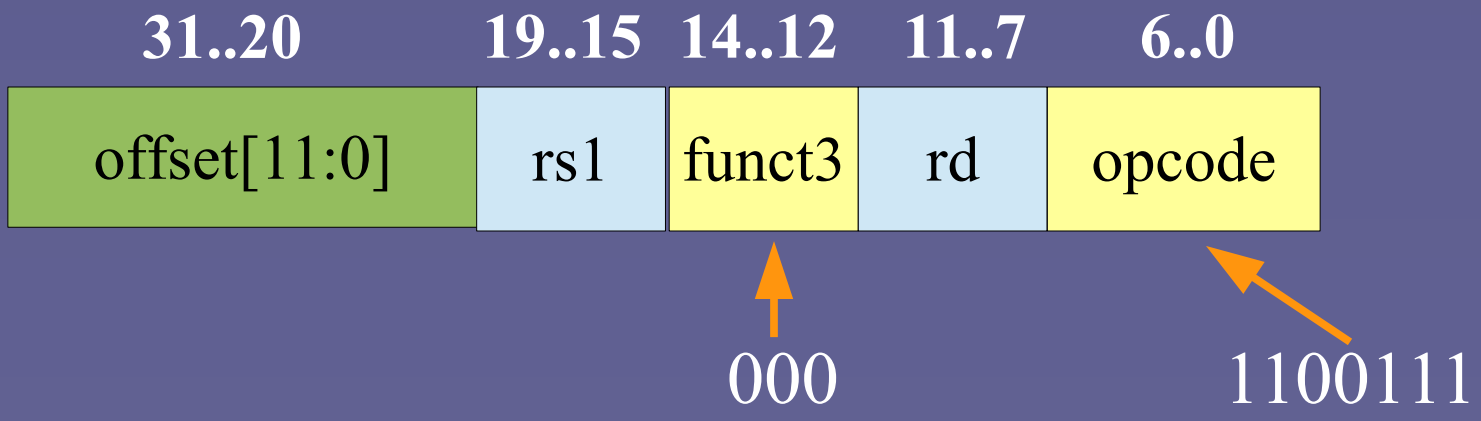
RISC-V RV32I Jump and link (JAL)



rd ← pc + 4 (next instruction)

pc ← pc ± offset

RISC-V RV32I Jump and link register (JALR)



rd ← pc + 4 (next instruction)

pc ← rs1 ± offset