Practical – 05

Class: - B.E.E&TC **Subject: - VLSI Design and Technology**

Aim: - To implement an inverter (not gate), NAND, NOR gate & 1 Bit Half Adder using CMOS technology

Theory :-

A] CMOS Inverter:

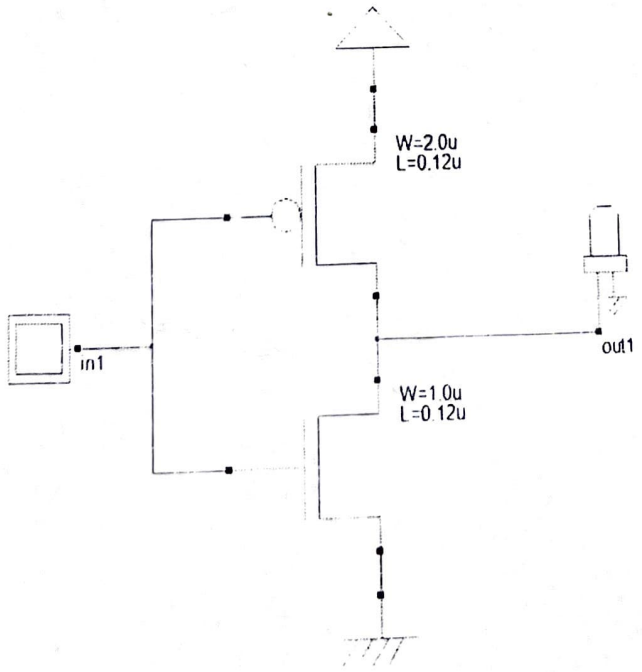
A logic inverter can be constructed by using one P-MOS and N-MOS inverter when there is '0' at input , then output is '1' and vice versa. In general a fully complementary always ha san n-Switch in pull down at output.

Truth table of Inverter:-

INPUT	OUTPUT
0	1
1	0

This is truth table of logic inverter where when there is a '0' at the input the output is '1' and when there is '1' at the input one output will zero.

Schematic of CMOS Inverter



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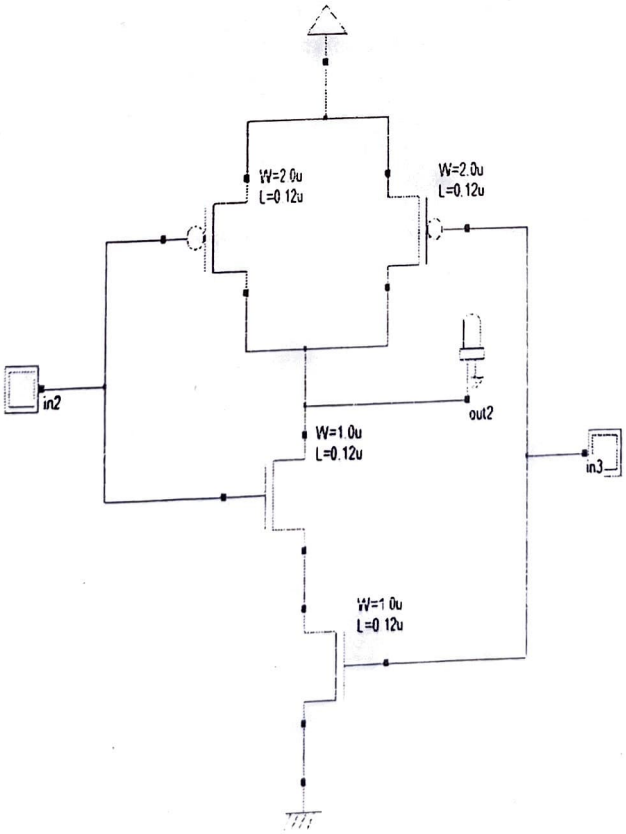
B] CMOS NAND Gate

Theory :- NAND Gate is formed by connecting an inverter i.e. NOT gate at the output of an AND gate

Truth Table:-

Input		Outputs
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Schematic of CMOS NAND Gate:



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Observation Table:

- **Effect of Capacitor on Power Dissipation**

Sr No	Capacitor	Power Dissipation
1	Without Capacitor	5.909 uW
2	With Capacitor (0.01pF)	17.908 uW

Conclusion: -

In this experment we implement NAND gate using Cmos inverter

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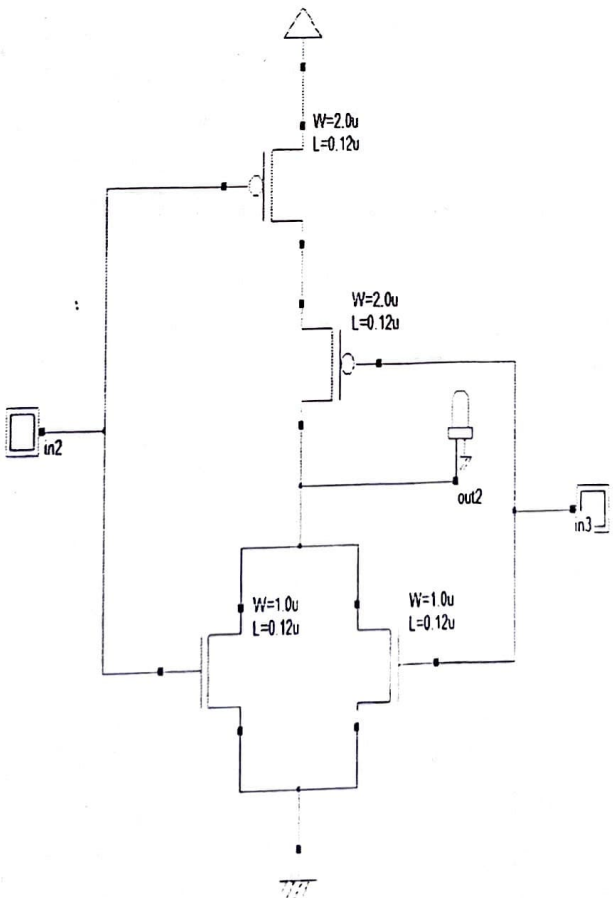
C] CMOS NOR Gate:

Theory :- A 2 input NOR gate can be constructed using NMOS & PMOS .

Truth Table:-

Input		Outputs
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Schematic of CMOS NOR Gate:



Observation Table:

- **Effect of Capacitor on Power Dissipation**

Sr No	Capacitor	Power Dissipation
1	Without Capacitor	5.028 uW
2	With Capacitor (0.01pF)	12.295 uW

Conclusion: - In this experiment we implement NOR gate using Capacitor and without capacitor

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Practical - 06

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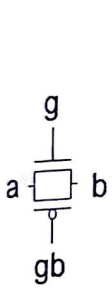
Aim: - To design and implement CMOS 2:1 multiplexer using Transmission gate & also comment on no. of pass transistors required to implement the same.

Theory: -

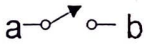
Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

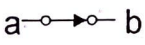


Input Output

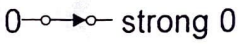
g = 0, gb = 1



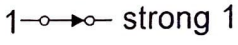
g = 1, gb = 0

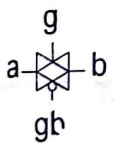


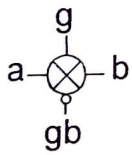
g = 1, gb = 0

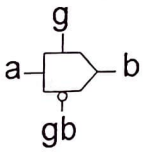


g = 1, gb = 0





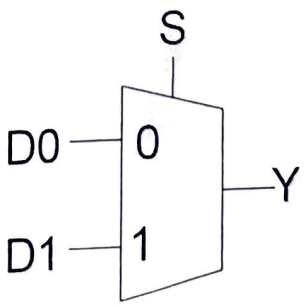




Multiplexers Using Transmission Gate

- 2:1 *multiplexer* chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0



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Practical - 07

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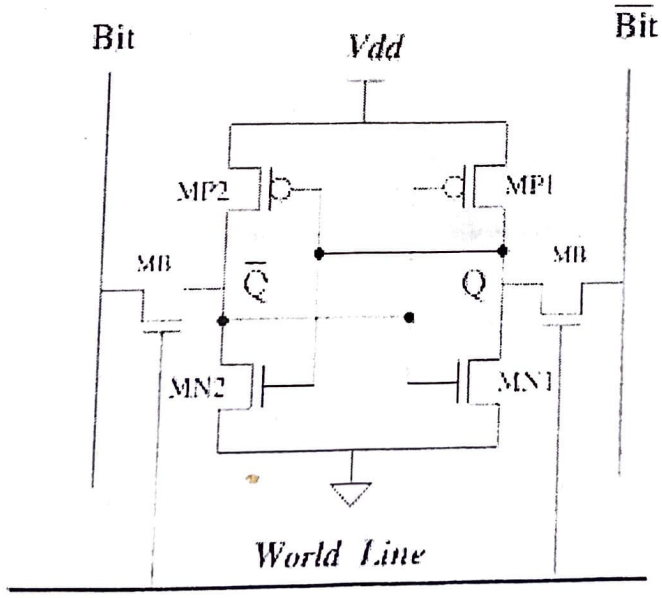
Aim: Design of CMOS single bit SRAM cell layout and verify the functionality by simulation

Procedure:

Prepare the CMOS layout of single bit SRAM cell. Do the functional simulation and verify the results.

Comment on the effect of no load and capacitive load on rise time and fall time.

Circuit Diagram:



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