Integrated Voltage Converters: Promise and Pitfalls

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Abstract

As computing becomes increasingly mobile, CPU power efficiency is as important as performance. Power sources operate at 3-12V to reduce resistive loss and must be stepped down to the CPU's 0.6-1.2V. As CPUs increasingly integrate functionality into a single System on Chip, power distribution is complicated by the disparate voltage requirements of the 30+ power distribution networks.

Integrated DC/DC converters are an emerging technology that target this issue. This paper examines the potential of these converters to address challenges of on-chip integration and I/O pin optimization. Directions for future work are proposed based on the state of the art in device technology and converter architecture.

1 Introduction

Consumer interest in high performance mobile computing drives high research activity in the field of power efficient CPUs. A popular chip design is a multi-core CPU combined with increasing levels of peripheral integration to form System on Chip (SoC) devices. This method offers energy efficient computation [9] and effective use of transistors that would otherwise be dark silicon [48]. However today's model has an unsustainable trend in the power to I/O pin ratio [44] and requires ever more complex power supply design. These SoCs typically integrate functionality but do not implement a unified power distribution network, exemplified by around 30 independent supplies for internal peripherals in the 2010 Nvidia Tegra 200 series CPU [34].

DC/DC voltage converters act as the bridge between system power source and chip supplies. Power sources generate voltages ranging from 3-12V but CPU core voltage ranges from 0.6-1.2V. Traditionally a voltage converter chip is mounted along with voltage filtering passives such as capacitors and inductors on a motherboard. These circuits are efficient, with losses under 10% and are essential for sustaining improving chip performance per watt trends. Distributing system power with high voltage PCB traces is desirable because trace power loss is proportional to I^2R. However, high chip power domain counts require increasing numbers of converters and filtering components. With a PCB mounted converter method, consequences are higher cost, increased hardware complexity and larger system area.

Chip integrated DC/DC converters offer a promising alternative and have been a topic of great research interest. Miniaturizing the converter circuit and implementing it on-chip can maintain system power efficiency with high voltage power sources while reducing area and component cost. In addition, the problem of unsustainable power I/O ratio can be addressed by aggregating supply lines. A recent example is Intel's Haswell CPU which features an integrated converter and reduces VDD pins by 20% over the previous architecture [20] [19].

Integrated converters also offer the potential for improvements in I/O and CPU performance. Since I/O performance is limited by PCB signal trace and I/O buffer power supply integrity, a research question is the bandwidth improvement possible due to finer control of the buffer supply. Additionally, integrated converters can change output voltages faster than off-chip versions, enabling finer-grained dynamic voltage and frequency scaling (DVFS). The rest of this paper is organized as follows.

Section 2 outlines the operation of the step-down DC/DC converter and its critical design parameters. Section 3 describes the pitfalls of integrating DC/DC converters on die. Section 4 provides a summary of recent research in integrated DC/DC converters. Section 5 identifies the promise of optimizing I/O and integrated circuit (IC) pin out with integrated DC/DC converters and pro-

poses directions for future work. Section 6 summarizes the state of the art and open research questions of integrated DC/DC converters.

2 How DC/DC converters work

DC/DC conversion can either increase or decrease input voltage with step-up or step-down topologies respectively. Since typical systems convert from high to low voltage (e.g. 12V to 0.6V) we focus on step down converters. The related work examines two primary types of converters: Switched Capacitor and Inductor-Capacitor (a.k.a. Buck). We review the literature to highlight critical properties that determine the feasibility of on-chip integration.

2.1 Switched Capacitor step-down converter operating principle

The first type of converter is the switched capacitor (SC) converter. A simplified canonical $\frac{1}{2}$ series-parallel step-down topology is shown in Figure 1. The converter is known as series parallel because in one phase of its operation, capacitors are in series and in the other they are in parallel. This is shown in Figure 2

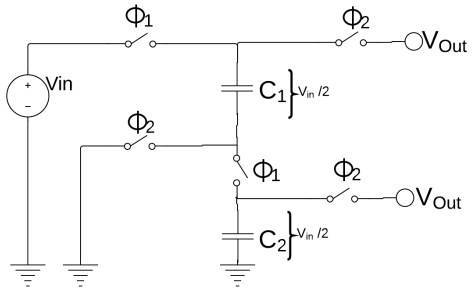

Figure 1: A $\frac{1}{2}$ step-down SC topology

We consider the circuit with electrically ideal components. C denotes some capacitance such that $C_1 = C_2$. switches are controlled by mutually exclusive clocks, ϕ_1 and ϕ_2. These clocks are non-overlapping.
The circuit has two phases of operation as shown in Figure 2. In phase 1, the charging phase, ϕ_1 switches are closed and ϕ_2 switches are open. C_1 and C_2 are in series. Since the capacitors are the same size, the voltage across both capacitors is $\frac{1}{2}$ of V_{in}.
In phase 2, the discharging phase, ϕ_2 switches are closed and ϕ_1 switches are open. Now Cf_1 and Cf_2 are in parallel. Since they are matched in size, the voltage across each capacitor remains at $\frac{1}{2}V_{In}$. Note that the voltage offset of Cf_1 moves from $\frac{1}{2}V_{In}$ to $0V$. Therefore,

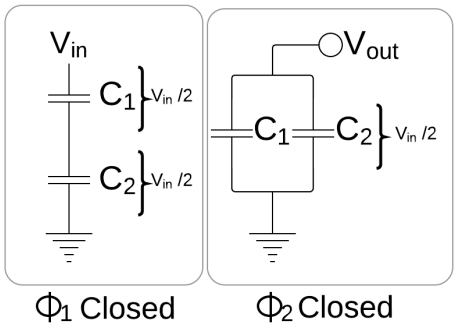

Figure 2: $\frac{1}{2}$ step-down SC topology capacitor configurations

$\frac{1}{2}V_{In}$ is seen at terminal V_{Out} since this is the voltage of both parallel capacitors.

2.2 Inductor-capacitor step down converter operating principle

The second converter is the inductor-capacitor step-down (Buck) converter. A simplified canonical topology is shown in Figure 3.

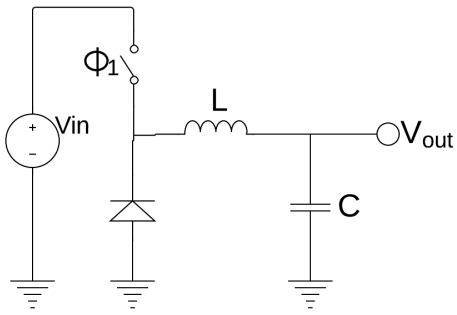

Figure 3: An inductor capacitor Buck topology

The voltage step-down principle is that V_{Out} is the same as V_C. Consider C in a discharged state. By closing ϕ_1 for a short period of time, V_C can be charged to a voltage lower than V_{in}. This works because L impedes the sudden change of current when ϕ_1 closes just as a resistor would, however an electrically ideal inductor does not dissipate heat to impede current and so no power is lost.

In its steady state, the buck circuit can be viewed as a low pass filter. ϕ_1 is a clock used to generate a square wave voltage of amplitude V_{in}. If this square wave is

at a frequency sufficiently higher than the 3db cut-off frequency of the filter, only the DC component of the square wave is observed at V_{Out}. Because of this, Buck converters may change their voltage step-down ratio during operation, by modulating ϕ_1. For a converter when current always flows in L (CCM mode), V_{Out} is defined by the duty cycle "D" [27] of ϕ_1 where: $V_{out} = V_{in} \times D$. In other words, if the square wave entering L is high for $\frac{2}{3}$ of its period, $V_{out} = \frac{2}{3} \times V_{in}$ and $D = \frac{2}{3}$.

2.3 Integrated Converter critical parameters

An integrated DC/DC converter implements the switch, capacitor and inductor power train components seen in Figure 3 and 1 within an integrated circuit package. This differs from traditional converters which implement the power train components on a PCB board external to the IC being powered by them.

A fully integrated converter implements the complete power train in the silicon IC, whereas a semi-integrated converter implements at least one part in the package the IC is mounted on. The package is also known as the substrate, e.g. ball grid array (BGA) package.

Integrated converters are challenging to implement because they require physically smaller components than discrete PCB substrate mounted DC/DC converters. Additionally, these components must be fabricated in a way that complies with the silicon fabrication processes' design rules and makes use of the materials that are available in that process. These implementations typically have different properties and loss mechanisms than the discrete versions mounted on a substrate or on a PCB.

The following subsections overview major loss mechanisms of converters and critical parameters that mitigate these losses during converter operation.

2.4 SC converter parasitics

2.4.1 Optimum topology

The energy that a SC converter can transfer per charge cycle is $E = CV^2$. We could therefore express $P = E \times F_\phi$.

For a design with a given V_{in} and ideal components, the designer has two degrees of freedom in designing a converter to power a load: C and F_ϕ.

We re-draw Figure 1 with non-ideal components in Figure 4.

We illustrate in Figures 4 and 5 that F_ϕ and C are critical parameters that must be optimized to minimize losses.

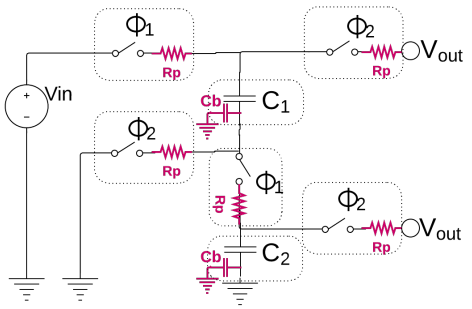

Figure 4: An SC topology with major parasitic components

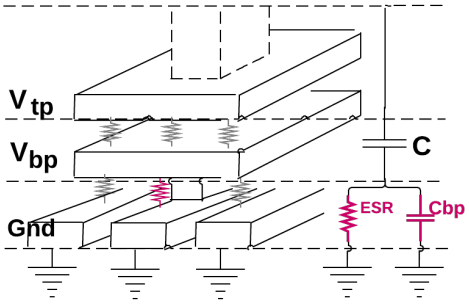

Figure 5: Bottom Plate parasitic capacitance

Determining values for F_ϕ and C depends on which loss mechanism is dominant in the converter. We now overview the constituent components and their losses in integrated converters as primer for understanding the tradeoffs.

2.4.2 Switching losses

Losses associated with switches are comprised of dynamic loss during the non-overlapping period of ϕ, and conduction loss due to the equivalent series resistance (ESR) of switches. Dynamic loss is examined in context in Section 3.

Conduction loss reduces the supply voltage seen at the capacitors by a factor δV, where $\delta V = V_{InSwitch} - V_{OutSwitch}$. Conduction loss is therefore correlated with the step-down ratio. Increasing the step-down ratio increases the number of series switches between all capacitors during the charging phase. For example a ratio of $\frac{1}{3}$ has 2 series switches, one of $\frac{1}{4}$ has 3 series switches and so on.

2.4.3 Capacitor losses

Another source of loss is parasitic capacitance losses. A parasitic capacitance known as bottom plate capacitance (C_{bp}), is depicted in Figure 5. Although the capacitor has an ESR, resistive losses are negligible compared to capacitive loss. C_{bp} exists between one plate of each capacitor and ground. The voltage of the parasitic capacitor is a virtual ground and reduces the supply voltage seen at the capacitors by δV_b. Their charge can leak to true ground but cannot reach a load. As they are smaller than useful capacitance, they are significantly charged and discharged on each cycle of the converter. Loss is therefore expressed as $P_{Loss} = E_{Cbp} \times F_\phi$ where $E_{Cbp} = \alpha C V^2$ [11]. The literature reports this to be the second highest loss mechanism in SC converters with bottom plate capacitance up to 5% of C_{tot} [39]. We also note that F_ϕ is adjustable at runtime yet C is not. Parasitic capacitance increases with capacitor area or the size of C; while I_{out} is proportional to both C and F_ϕ [11]. Strategies to reduce bottom plate loss are therefore attractive since they lead to more efficient large capacitors, which in turn reduces the required F_ϕ. Reducing F_ϕ is attractive because it reduces dynamic switching loss (detailed in Section 3.2).

2.4.4 Circuit noise

SC converters are relatively noisy compared with Buck converters because they do not have the built in output filter of the Buck. Output noise is therefore strongly related to high inrush current to the power capacitors [54]. Thus, noise depends heavily on switch and capacitor device parameters, and must be mitigated through careful switch design and timing control to reduce high frequency noise.

2.5 Inductor-capacitor converter parasitics

Buck converters experience similar switching and capacitive loss mechanisms as SC as both circuits feature these components. Accordingly this section focuses on the inductor losses unique to buck converters. Because Buck transient behavior is more complex than SC, a brief overview of power and noise in the circuit is given as an aid to understanding trade-off for the critical circuit parameters.

Figure 6 represents Figure 3 with major parasitics.

An extra MOSFET switch is common in the literature and replaces the diode of Figure 3. ϕ_1 and ϕ_2 are mutually exclusive and when ϕ_2 is closed, a clockwise current loop is induced by the charged inductor, as occurs in the diode circuit of Figure 3. Introducing this device gives Buck and SC converters a common power switch loss mechanism at each phase of operation, but

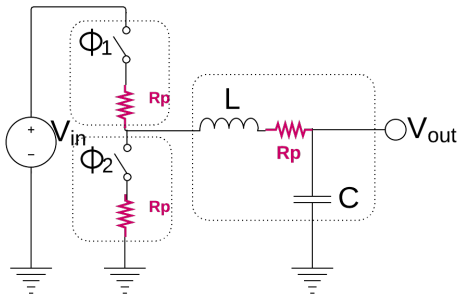

Figure 6: A Buck topology with major parasitic components

the basic Buck features fewer switches contributing to losses than even the most basic SC.

2.5.1 Inductor Losses

Losses associated with the inductor are dominated by equivalent series resistance (ESR). Standard CMOS only permits for a planar inductor, shown if Figure 7. Increasing inductance is accomplished with a spiral coil

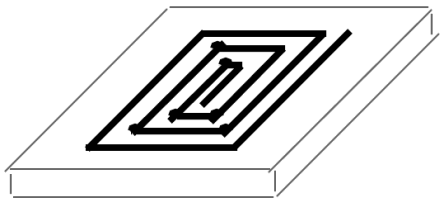

Figure 7: A typical CMOS spiral inductor metal pattern

to increase flux linkage High inductance requires high numbers of thin coils per unit area, which translates to increased series resistance (ESR) through the coil.

Besides the ESR, the series connection with capacitor C introduces impedance Z_{LC} determined by the switching frequency (F_{Sw}) of the Buck. It is critical to match L to F_{Sw} and C to minimize this impedance, but the ESR may never be removed.

2.5.2 Circuit noise

With the voltage step-down principle in mind we consider the circuit in Figure 3 from a current perspective. We cannot directly apply Kirchoff's law due the AC variation of current (I) with time (T). However $P_{In} = P_{Out}$ for conservation of energy. Power can only enter the system when current flows through the closed

switch from V_{In}. Due to either the diode in Figure 3 or open circuit switch in Figure 6, its path to the load must be through the inductor. Inductors impede current less as they are charged, therefore for some T_{On} a high P system can be realized if either:

1. L **is small relative to** T_{On}: A very small inductor is charged significantly over a short time
2. T_{On} **is large relative to** L: A large inductor is charged for a very long time

We consider that during T_{Off}, the inductors charge dissipates through the rest of the circuit as current driving the load and parasitic components. Let $T = T_{On} + T_{Off}$ and $F_{Sw} = \frac{1}{T}$ so now 1 and 2 correspond to designing a Buck with either;

- A high F_{Sw} and small L for scenario 1
- A low F_{Sw} and high L for scenario 2

With the voltage step-down principle is in mind, it follows that the choice of L determines the choice of C to minimize Z_{Out} for the desired DC operating points of V_{Out} with a given fixed F_{Sw}.
Another intuitive observation is that lower P requirements result in L and F_{Sw} values that are easier to realize for given technology limitations, since $P \propto L \times F_{Sw}$. More precisely $P = V_{Out} \times \frac{V_{In}(1-D)}{2L} DT$ for the maximum load condition.

As is common in analogue circuit design, transient operating points complicate the choice of components. A brief overview of solutions provides context for evaluating component loss and trade-off.
A given digital circuit load has operating conditions that must be satisfied. The following parameters are used to design operating point behavior for a Buck:

- **Current ripple,** Δi_{Out}**:** Tolerable current variation through the load
- **Voltage ripple,** Δv_{Out}**:** Tolerable supply voltage noise at the load
- **Switching frequency** F_{Sw}**:** Nominal switching frequency of the power switches, lower reduces power loss but increases Δv and Δi
- **Operating voltages** V_{In}**,**V_{Out}**:** Nominal input and output voltage of the converter
- **Maximum drive power** P**:** Converter Power at the highest DC load. $P = V_{Out} \times I_{Max}$

Δi,Δv,V_{Out} and P are constraints specified by the load. V_{In},F_{Sw} along with the passive components C and L must be chosen to satisfy the load constraints as well as technology constraints.
Δ_i **Current ripple:** Digital circuits require low supply ripple for deterministic operation. Supply current ripple is defined as

$$\Delta i_{Out} = \frac{(V_{In} - V_{Out})D}{2LF_{Sw}} \text{ [27]}$$

With the current flow principle of the Buck in mind, it follows that this formula does not involve C.
Δ_v **Voltage ripple:** Digital circuits require low voltage ripple for reliable operation. Typically $\frac{V_{Load}}{10}$ is specified. Supply voltage ripple is defined as

$$\Delta v_{Out} = \frac{(V_{In} - V_{Out})D}{16LCF_{Sw}^2} \text{ [27]}$$

Because the Buck works as a low pass filter it follows that this formula involve F_{Sw}, L and C

In summary the loss mechanisms in the Buck converters offer more degrees of freedom for optimization than SC designs because of the additional component type of the inductor. The ripple formulae are useful in limiting aggressiveness applied to any particular parameter and can be used to balance the losses of power train components.

2.6 Converter load regulation concept

Load regulation is matching output impedance "Z_O" of a power converter to a current load. Because $I = \frac{V}{Z_O}$ and maintaining V for a digital circuit is critical, converter output impedance must track quickly with the load condition to keep V constant. The responsibility of tracking load and adjusting Z_O belongs to control circuits. A block diagrams is shown in figure 8
Buck converters can reduce Z_O by increasing conductance. This is done by increasing "D" [27]. Because the asymptote is impedance of the filter at F_S, Z_O may also be increased by reducing F_S [2].
SC converters power loads capacitively. Because the capacitors supply a DC load in parallel, Z_O cannot be lowered below $Z_C + Z_{Sw}$ at the nominal F_{Sw}. Modulating F_{Sw} can increase impedance in practice, because the capacitors can be purposely under-charged [43].

3 Pitfalls of Integrated DC/DC Converters

Practical integrated converters are emerging and designed with different goals. A taxonomy of reviewed lit-

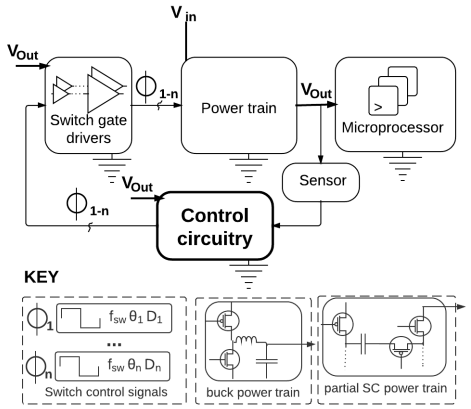

Figure 8: Basic DC/DC converter control loop where: f_{sw} = switch frequency θ_x = phase, D_x = duty cycle

erature identifies two groupings:
1: Power system replacement converters. The research aim is to remove external converters with an equal performing integrated subsystem.
2: LDO replacement converters. The research aim is an incremental improvement of the Low-drop-out (LDO) regulators that have long been integrated on chip. The LDO is a linear voltage converter that reduces voltage using a variable resistance. It does not require any capacitors or inductors so can be integrated with transistors alone.
These differing goals result in different design trade-offs. We focus on group 1 because of an efficiency reason. We focus on Power System replacement converters because LDO maximum efficiency is only 50%, too low for use as integrated dc-dc converters.

Early examples of a CMOS integrated SC converter [51] and CMOS integrated Buck converter [3] show the pitfalls of CMOS only basic converters.

3.0.1 SC drawbacks

Naive Integrated SC converters have a low power density. Power density is measured in watts per square mm (W/mm^2) and is important to keep high. If a converter power density is equal to its loads power density, the IC must double silicon area for an adequate power supply. This means in practice converter power density must be much higher than the load for a cost effective use of silicon. Viraj et al [51] realize an on die capacitance of 1.6nF with a converter power density of $1.7mW/mm^2$. In comparison the baseline Buck [3] realize on die capacitance of 1.1nF with a power density of $20mW/mm^2$.
The baseline SC converter also realizes much lower efficiency than Viraj et al. expected. 80% is predicted in the work, but only 62% is achieved due to unmodeled parasitic losses.
Only a single step-down voltage ratio is implemented, since the fixed SC circuit topology described in section 2.1 is used. As such, impedance matching is not possible in this work

3.0.2 Buck drawbacks

Although power density is higher than the baseline SC, it is still too low for many contemporary processors. As an example the low voltage embedded Freescale MPC8640 requires around $1.1W/mm^2$ [13]. This is far lower than laptop and desktop CPUs but orders of magnitude above the baselines.
Naive Integrated Buck converters have a low efficiency. Alimadadi et al. [3] achieve a peak efficiency of 46%. Not only is this lower than the baseline SC [51], its lower than an LDO (50%).
Unlike the SC design, the baseline Buck can implement a range of step-down voltages in a basic topology. However the baseline has poor load regulation. At its lowest output voltage it has a 25% efficiency in its most sophisticated control mode. This drops to 13% in its standard mode.

3.1 Pitfalls specific to integrated converter type

Both baseline designs ([3] and [51]) have poor output impedance control or load regulation. This is unacceptable because SoC like CPU's implement power gating and other techniques that change the power converters load condition. Good efficiency is required for all possible power loads. Integrated SC and Buck circuits must have a unique solution to this problem because they have different ways of controlling impedance (discussed in Section 2.6). We review circuit architecture and control research addressing the problem of output impedance in Section 4.5 for integrated Buck and Section 4.4 for integrated SC circuits.

3.2 Common integrated converter pitfalls

At the ideal voltage conversion and loading operating point, poor performance of both integrated converters is due to power train component losses. At this ideal point, the pitfalls of baseline integrated Buck [3] overlap those of the SC baseline [51].

Table 1 of pitfalls highlights the benefit of improving power train components. Both converters share a need to

	CMOS SC [51]	**CMOS Buck** [3]
Switch	Secondary efficiency	Secondary efficiency
Capacitor	Primary energy density and efficiency	Secondary energy density
Inductor	Not applicable	Primary energy density and efficiency

Table 1: CMOS realized components and their loss contribution in integrated converters

reduce losses seen in baseline designs and share all components except the inductor. Pure CMOS components were shown to have poor energy density and or high loss in the baseline designs. We review reasons for the poor performance of CMOS components as primer for the literature that addresses component issues in Section 4.

3.2.1 CMOS Switches

CMOS switches suffer static and dynamic parasitic losses due to gate capacitance and non-idealities as shown in Figure 9. As integrated converters typically operate at hundreds of MHz ([3], [7], [46] etc.) dynamic loss strongly influences the problem of optimally balanced switching loss.

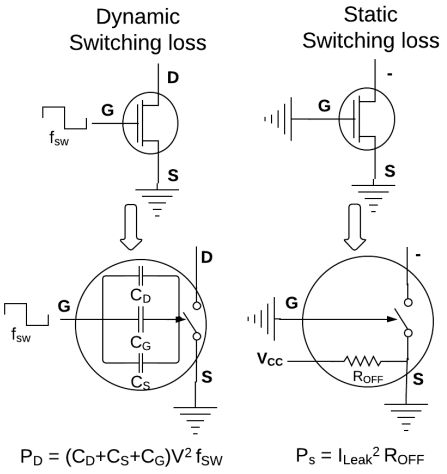

Figure 9: Diagram of major MOSFET switch losses

Static losses are constant no matter if the MOSFET switch is on or off. They occur because the MOSFET does not have an infinite open circuit resistance. Static loss is therefore technology node dependent and impossible to remove completely. Static losses are contributed to by components from sub-threshold leakage and gate oxide leakage currents.

These losses are intrinsic to all transistor based switches, however trade-offs possible in modern technology nodes for full integration are less optimal than older technologies. Aggressive technology scaling continuously increases transistor leakage[21], so that realizing the highest compute performance results in switches with the lowering efficiency in fully integrated designs.

Dynamic losses occur due to toggling the MOSFET switches. Power is consumed by changing the switch condition. As such, losses can be reduced by reducing switch toggling frequency, since for a given technology loss of the power switches and drivers increases by approximately $\sqrt{F_s}$[5]. However given fixed size energy transfer components, reducing F_s reduces the converters power rating since $P = F_s \times E$.

Conduction loss occurs because the MOSFET switch does not have a zero on resistance. At a DC operating point, the conduction loss is simply the resistance of the MOSFET. Resistance of a MOSFET may be reduced by decreasing its channel length, L_{ch} or increasing its channel width, W_{ch}. The minimum channel length is determined by process node e.g. 22_{nm} long in a 22_{nm} process, but channel width can be extended arbitrarily. However gate capacitance, $G_c \propto W_{ch} \times L_{ch}$. Reducing conduction loss therefore increases dynamic loss by increasing the power needed to charge G_c and toggle the switch.

As a final note, CMOS switches cannot usually operate reliably beyond the technology node voltage. This imposes limitations on the step-down voltage ratio that can be achieved if a switch is connected between power rails. Because of these limitations important problems are reversing the leakage trend [21] and increasing voltage above normal transistor levels.

3.2.2 Capacitors

On-chip capacitors suffer particularly from bottom plate capacitance as shown in Figure 5.

The loss problem is complicated by the frequency dependence of capacitor impedance/reactance. This is encapsulated with the capacitors "Q" quality factor. $Q_c = \frac{1}{\omega C R_c}$. If Q_c = 1, the capacitor is ideal and does not impede a voltage signal. The "Q" factor has a different level of criticality in SC and Buck designs. Buck designs can offset a low capacitor "Q_c" value with their inductor if properly designed.

Because integrated converters toggle their power

switches at a high frequency, parasitic capacitance loss is high (see 2.4). This is more critical for integrated SC designs since they must transfer all of their energy via capacitors with a large area in close proximity to the ground network. As was seen in the baseline SC, failure to model losses during design can greatly impact efficiency [51].

The loss mechanisms in a capacitor are fundamental and cannot be improved at the circuit level unless a circuit can be realized with different components or reduced capacitance. Therefore important research questions involve critical technology parameters. Because buck converters can use inductors as well as capacitors, they are less sensitive to low quality capacitors.

3.2.3 Inductors

Inductors have frequency dependent impedance similar to capacitors. As such, they have a quality factor, $Q_l = \frac{\omega L}{R_l}$. As in the case of the capacitor, $Q_l = 1$ represents a perfect inductor. In a standard CMOS process, $R_l \gg R_c$. This is because $L \propto \phi_{ind}$ where ϕ_{ind} is magnetic flux. In standard CMOS, ϕ_{ind} is increased by increasing the inductor length and hence increasing R_l. Contemporary CMOS has metal layers optimized for digital circuits, so design rule track spacing is likely sub optimal from a flux linkage perspective. Area is inefficiently used and R_l is high. Conversely for a capacitor, increasing C requires increasing plate area and hence reducing R_c. For this reason SC designs often cite low Q_l as their research motivation ([37], [40], [30] etc.).

Because the impedance of inductors is phase shifted from capacitors, Buck converters can be optimized at the circuit level through component sizes. However, given their low Q_l due to high resistive loss, important research questions concern technology parameters critical to improving ϕ_{ind} and reducing R_l.

4 Survey of recent literature

We evaluate recent literature addressing the previously outlined issues of baseline CMOS integrated converters. We begin with work on the common building blocks of passive components and power transistors, then move on to review system level advances for the different converter types.

4.1 CMOS Switches

Alimadadi et al.[3] propose an energy recycling mechanism to use the charge at the power switch gates as useful energy by pumping it to the load. The power PMOS and power NMOS gates are driven by stacked supply buffers to toggle the power switches. VSS of the power PMOS gate buffer is VDD of the power NMOS gate buffer via an electrical connection at a node, x. By connecting node x to the load via a forward-biased diode, energy used to charge power MOS gate capacitance can also charge the load node, rather than sink to ground. The drawback of this technique is that the $\frac{1}{2}$ VSS swing of the power MOS gate nodes limits the amount of step-down possible. It would therefore not translate to a high voltage step-down.

Bathily et al.[7] also focus on energy loss in switch toggling. They propose an LC tank that resonates at F_s such that the power MOSFET switch gate voltages oscillate at this resonant frequency. If the power switch gate voltage is low, the switching energy is stored in the tank inductor. If the power switch gate voltage is high, switching energy is stored at the switch nodes. The authors find improvements in switch efficiency ranging from around $12-25\%$ across the complete operating range. However the requirement is 16nH of inductance occupying 40% extra silicon area in a standard CMOS process. The technique is applicable in high voltage converters, but the $\approx$30% reduction of energy density makes it unattractive in medium to high power applications.

Hyunseok et al. [33] address the higher than operating voltage step-down issue with circuit design and CMOS layout techniques. The circuit design handles higher than operating voltage by stacking power MOSFET devices in series such that each device does not drop more than the CMOS operating voltage. The sum of series voltage exceeds the operating voltage however. This key novelty is the circuit design of the power MOSFET switching inputs, which are toggled by operating voltage, despite the switch stacking. Although an arbitrary voltage step-down could be achieved with power MOSFET stacking, this technique has diminishing efficiency for two reasons. Firstly, the conduction loss of the stacked power switches is summed, reducing efficiency. Secondly, the switch toggling energy of the stacked power switches is summed since it is capacitive. This reduces the maximum F_s and therefore increases the required C or L for a fixed power envelope. As such this technique is less attractive as input voltage increases.

In the same increased V_{In} vein, Bandyopadhyay et al[42] propose a Buck converter with stacked power MOSFET switches. However, they use a single drain extended NMOS (DEnMOS) for high voltage and stacked PMOS devices. DEnMOS increases the reverse break-

down voltage of a MOSFET so that it will not short circuit at voltage above the technology operating VDD. An advantage of DEMOS is that no special process steps are needed. The main disadvantage of DEMOS in high voltage converters is high on-resistance and sensitivity to process variation. The limit of voltage step-down and current flow is around 30V at 2A [16] at which point non-standard CMOS process is required for reliable operation.

With the limit of DEMOS in mind we consider the literature regarding switches suitable for high voltage and or high current.

For voltages above 20V at current above 1A, lateral Double-Diffused MOS (LDMOS) switches outperform DEMOS. Hower et al. [16] are paraphrased as follows: *LDMOS devices have lower on-resistance than DEMOS but have a fixed device length, so transistors cannot be folded geometrically*. LDMOS can be integrated into a low voltage technology node monolithically because they are compatible with bulk CMOS. The cost is an additional mask layer and therefore a non-standard process. A final drawback is LDMOS has a higher V_t, so they require more switching energy.

Finally in the high F_s, high power design corner we consider AlGaN/GaN switches. Although much research effort has been made to improve power density and breakdown voltage, AlGaN/GaN switches outperform LDMOS in high-power high frequency switching applications [15]. This is because these switches have unique semiconductor properties beneficial to high voltage power conversion, such as: high operating frequency, high current density and high breakdown voltage[10],[12]. Krausse's [25] summary of recent literature on power transistors is reproduced in Figure 10. This graph demonstrates the advantages of AlGaN/GaN devices over LDMOS in the high power domain.

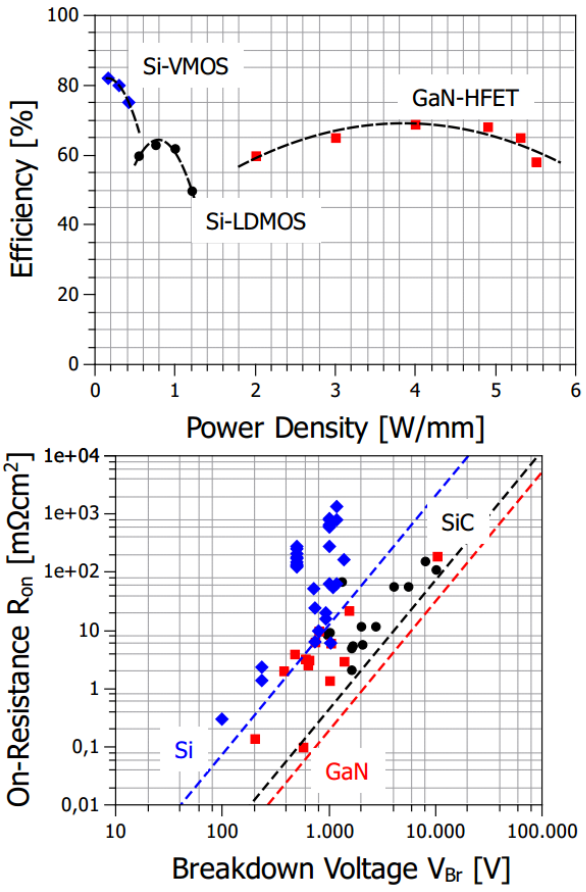

Figure 10: Comparative performance of power switch types, Reproduced from[25]. CMOS is increasingly undesirable as power density and voltage increase

To conclude discussion on power switches, the literature proposed novel circuit designs to improve switching efficiency. The limitations of these designs focus attention on the switch devices. The literature indicates as voltage and power density demands of a design increase, non-standard CMOS process and CMOS alternatives become increasingly attractive.

4.2 Capacitors

After Viraj et al. [51], much research effort was expended regarding converter capacitor energy density and impedance modulation. Kwong et al. [28] address both issues uniquely. The load is a sub-threshold processor, which allows low-energy density capacitors to provide adequate drive. Converter impedance is reduced with technology options and circuit topology. Metal Insulator Metal (MIM) capacitors are used as power passives. MIM capacitors are offered in some VLSI processes and form capacitors from two extra thick metal layers. These capacitors have the desirable qualities of being compatible with bulk CMOS and having a high Q_c. Their disadvantage is low energy density because of a relatively thick insulator layer.

With low energy density, impedance matching becomes increasingly important for a converter to have compelling performance. Viraj et al. [51] observed an exponential deterioration of efficiency with mismatched load impedance.

Because of the double issue of CMOS capacitor energy density and exponential efficiency decay with a simple SC converter, non-standard CMOS capacitors dominate contemporary integrated converter literature. Since energy density is improved by reducing loss, early work explored the limit of CMOS with circuit techniques. Besides their other innovations, Kwong et al. [28] fea-

Capacitor	Material	Permittivity (ε_r)
Bulk CMOS [41]	SiO2	3.9
High K CMOS [41]	HfSiO4	11
Deep trench [23]	PZT	1000
Ferroelectric [31]	BaTiO3	≈4600

Table 2: Capacitor permittivity. Special process deep trench and special material Ferroelectric capacitors are the most promising for energy dense integrated converters

ture a charge recycling circuit. The operating principle is similar to Alimadadi's work [3], but the energy source is parasitic capacitance and bond wire inductance. The technique was not implemented in later designs by the authors or others, so it may be a dead end.

Later work focuses on technology options for improving energy density. In CMOS compatible technologies, MIM [28] and Thin-gate MOS/fringe metal [37] capacitors are succeed by the exotic Deep trench [4] and Ferroelectric [11] capacitors as seen in Table 2.

These exotic capacitor types typically greatly increase C per unit area because they realize an extremely high permittivity (ε_r). Capacitance is calculated $C = \varepsilon_r \times \frac{A_p}{l_p}$ where A_p is the area of capacitive plates and l_p is the separation distance.

High ε_r can effectively negate bottom plate parasitic capacitance, since these parasitic capacitors could have an ε_r several orders of magnitude lower than the power capacitors.

To close on the topic of high ε_r, baseline ferroelectric capacitor designs such as El-Damak et al. [11] do not exhibit multiple order of magnitude power density improvements over others. In these capacitors, ε_r can vary greatly with temperature [31] and frequency [8], which adds challenge when applying ferroelectric technology. Deep trench has been demonstrated with multiple order of magnitude power density improvement by Andersen et al. [4]; however this converter design combines the capacitor structure with silicon on insulator (SOI) to enhance the capacitor Q_c. Demonstrated power density presently lags behind Buck designs, necessitating further research to determine capacitor limits in integrated converters.

Another class of converters has gained prominence due to the difficulties of energy density in capacitors. Semi-integrated converters ([36], [7], [50] etc.) use off-die capacitors as a charge source. Provided such capacitors can be connected to the rest of a converter with a very low inductive path, these designs offer higher drive capability at the cost of an extra component.

In summary of capacitors, early CMOS circuit level approaches to energy density have been superseded by non-standard CMOS.

4.3 Inductors

Since total inductance is improved by increasing mutual inductance within a conductor structure, researchers have made several attempts to improve Q_l with custom inductor layout. Angular spiral inductors which implement the spiral inductor of Figure 7 with a polygon spiral of 5 sides or more were shown to have inadequate Q_l for efficient fully integrated power converters[3][6]. Researchers are therefore exploring alternate structures and materials. Meere et al. [32] characterized fully integrated racetrack style inductors for Buck power converters. They find the Cu resistivity ($\Omega \times \frac{A}{l}$) to dominate loss and to increase exponentially with F_s. They conclude 7mA as the supply limit of a converter with such inductors.

As with capacitors, the Q_l problem was also explored using semi-integrated converters. Researchers realized the parasitic inductance of bond wires could be re-purposed to become active power delivering inductance [52], [1]. This work received much attention owing to the high L of bond wire relative to integrated Cu spiral and racetrack inductors. In addition, since package inductance is a large contribution to power loss, end to end efficiencies have been realized up to 84.7% [18]. Owing to the relatively low resistivity of bond wire, energy density is also greatly improved with an I_{Out} of 1.2A reported [18].

Researchers have also combined innovations. L is enhanced when the core of an inductor is a high permeability material, since $L \approx \frac{N^2 \mu A_L}{l_L}$ where μ is the permeability of the core. To this end Hongwei et al. [22] propose applying a ferrite epoxy to bond wire inductors, with Wang et all. proposing ceramic (ferrite) tape for 2.5D semi-integrated passives. Although neither author was able to match the energy density of Cheng's work, a more fundamental issue prevents bond wire inductor converters from attaining reduction in pin count. Consider the example pin configurations in Figure 11.

If A power delivery operates at the current failure limit of wires, with power transfer efficiency less than 100%, Topology b, with no switching converter in Figure 11 is able to deliver more power per pin than topology a, which features bond wire inductors.

Attacking the above mentioned limitations, researchers have integrated high permeability materials in to custom VLSI inductor layouts. Recent advances in device physics have yielded thin film inductors [35] with orders of magnitude energy density improvement over those in prior art [32]. Sturcken et al. [46] propose a converter with such devices able to drive 6.3A and Intel reports 400A [49] using the same inductor technology. This is the highest reported drive of all integrated

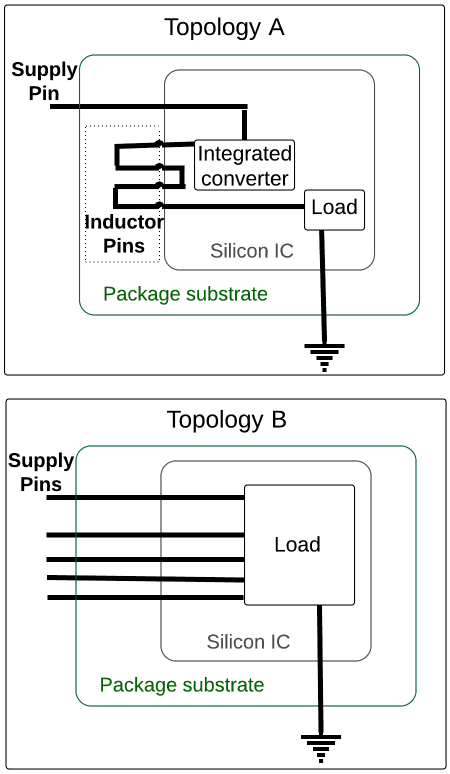

Figure 11: The power limitation of bond wire inductors. Wire current limit means Topology B can supply more current to the load if Topology A is $< 100\%$ efficient

converters to the authors knowledge. Thin film inductors are presently subject to a significant caveat. Due to their geometric structure and unique ferroelectric core they are not integrated into bulk CMOS in the literature, instead being built on a separate interposer.

In summary, inductor research focuses on improving Q_l. Thin film inductors are the current state-of-the-art and enable much higher energy density than capacitors alone.

We distil the component literature as a whole as follows. Power switches offer many options for design trade-off, depending on the operating requirements of a digital circuit. The upper limits of voltage and energy density are reached with CMOS alternative transistors. Passive components were limited in energy density with standard CMOS. Recent advances in device physics have succeeded in miniaturizing energy dense inductors and capacitors, but these require additional doping material and process steps to create on bulk Si. As with power switches, the upper limit of energy density is not demonstrated in bulk CMOS

4.4 SC Architecture

Integrated SC architecture research focuses on addressing the poor load regulation and line noise of the basic circuit topology described in Section 3.

4.4.1 Improving load regulation

Basic SC converters have no load regulation. Load regulation is desirable as it improves the exponential decay in efficiency outside of the basic topology operating point(s). This is because increasing Z_O for light loads means less power is burned in the converter, since for a fixed operating voltage, the end to end DC impedance is higher and therefore end to end DC current is lower.

As seen in Viraj et al. [51], integrating SC converters to digital processor dies allows for complex capacitor and switch topologies, since bulk capacitance can be sub-divided.

Le et al. [29] propose a novel converter circuit topology with more granular impedance modulation control than that of Viraj. By splitting C into 4 parallel SC converter modules, Z_O is adjusted by modulating the phase difference between the F_s of these modules. The converter also features the re-configurable step-down voltage circuit for coarse grain voltage control reported in Kwong's work [28]. Peak efficiency is far higher than Viraj's work[51] at 82%, and the efficiency curve has linear regions as opposed to the purely exponential worsening of Viraj.

Although other work ([38] etc.) implements capacitance modulation, Le et al. is notable for additionally implementing switch conductance modulation.

Conductance modulation of the power switches allows finer control of converter impedance, since the MOSFETs are analogue devices. However since the operating principle is equivalent to an LDO, it is unattractive in terms of efficiency.

4.4.2 Improving line noise

Basic SC converters have high voltage ripple because of exponential discharge of the power capacitors to the load. Improving the voltage line stability is important as digital circuits have low line noise tolerances.

Line noise is addressed in the literature by sub-dividing the load driving capacitance as was seen in load regulation improvement techniques. The converter modules operate out of phase, as employed by Le et al. [29] with the exception that phase shift is fixed. Superposing the exponential voltage discharges of multiple modules at maximum phase shift on the power bus smooths V_{Out}. Success of this technique motivated aggressive

exploration of capacitance module phase slicing in the literature. Pique [37] reports a load driving capacitance sliced into 41 phase shifted parallel converters and find line noise to improve around 16× compared with 10 phase prior art.

4.5 Inductor Buck architecture

The basic Buck topology offers superior impedance modulation relative to SC designs by employing pulse width modulation (PWM) of V_{In}. Earlier discussion focused on Continuous Current Mode (CCM), where conductance is varied by altering the duty cycle D of the switch at V_{In} in Figure 3. Increased conductance improves Buck voltage droop for heavy loads since the converters impedance can be reduced for power transfer at a maintained operating voltage as the load increases.
For light loads, efficiency is improved with increased impedance. Impedance is increased by shortening the inductor charge pulse. In DCM, inductor current is "discontinuous" because the charge pulse in the PWM is so short the inductor fully discharges into the filter capacitor F_c and load. In DCM mode, DC V_{Out} is no longer simplified to $D \times V_{in}$ because C supplies both current and voltage after the inductor is discharged. Resolving V_{Out} is therefore non trivial for Buck control circuitry.

Integrated Buck converters can feature complex digital control loops and the literature explores this space. The two challenges are precisely controlling the operating point in DCM and switching between DCM and CCM at optimum intervals for a load in flux.
Wens et al. [53] report a novel SCOOT control system for alternating between CCM and DCM. SCOOT differs from the bulk of literature on this topic by splitting the passive components into a grid of sub modules, a technique applied in integrated SC architectures. However unlike capacitance, inductance reduces for electrically parallel modules, such that the four constituent converters quiesce in DCM mode. The superposition principle allows Wens to simulate CCM in this quiescent mode by adding a phase shift of $\frac{\pi}{2}$ for each module relative to its two adjacent neighbors. DCM can be forced by reducing the duty cycle D. The benefit of this approach is reduced ripple voltage at V_{Out} compared with monolithic passives. SCOOT varies module phase along with D in attempts to optimize the operating point to load, however the latency of the passives and control circuitry appears to oscillate efficiency around the load operating point in an undesirable way.

The imprecise operating point of DCM is addressed with control techniques on monolithic passive designs.
DCM control operates on a hysteresis principle since D does not govern V_{Out} in DCM mode. Non-integrated Buck converters can adjust T_{On} of the power train switch(es) after sensing V_{Out} in a timely fashion since these converters feature large passive devices. Switching speeds typically occur in the KHz regimen. The small passive size of integrated converters requires switching speeds of hundreds of MHz ([3], [7], [46] etc.). With control circuit blocks operating in the nS range, simple hysteresis control of integrated Bucks has received attention in the literature.
Feng et al. [47] propose a delay compensation hysteresis controller for integrated DC/DC converters, however their approach requires overcharging the load for faster operation of the control comparator circuitry. This is unattractive from an efficiency perspective, since the goal is to increase converter impedance in DCM. Cheng et al. [18] address this by using a short discharge pulse of the load. They calibrate the control loop timing for different light load conditions using difference in the sensed V_{Out} before and after discharge to determine an optimum T_{On} to restore V_{Out}. As Cheng's method increases output impedance, it is more attractive in DCM mode than Feng's. The 84.7% efficiency is the highest reported for a chip integrated Buck converter, however the architecture cannot be applied to moderate and heavy loading conditions.

Researchers have applied circuit design to improving performance characteristics besides efficiencies. An additional flying capacitor added to the basic circuit can reduce the total capacitance by 50% according to Cheng [17]. Flying capacitor Buck converters vary in topology depending if the target passive for reduction is capacitive [17] or inductive [24], but all create a more complex filter and energy storage network. The Additional components allow greater freedom in creating the circuit transfer function enable researchers to operate at a target load range with smaller passives, by focusing filter attenuation to the switching frequency more precisely.

To summarize converter architecture research, integrated Buck and SC topologies improve performance with common techniques such as passive slicing and control phase shift techniques applied to modular converter designs. Both types of converter are able to improve control of impedance, Z_O however the SC design is still fundamentally limited to higher impedance than the Buck.
In addition, circuit techniques in the literature are shown to reduce the passive sizes beyond those required for a basic topology.

5 Promise of integrated DC/DC converters

High performance I/O pins in digital circuits have a bandwidth constrained by both the electrical performance of the transmission line and I/O buffers. We consider the possibilities of improving I/O bandwidth limits with integrated converters in this section.

5.1 DC/DC converters and I/O pin performance

The I/O performance benefit of integrated DC/DC converters is due to a much faster control loop. This is shown in Figure 12.

The high switching speed and bursty nature of high

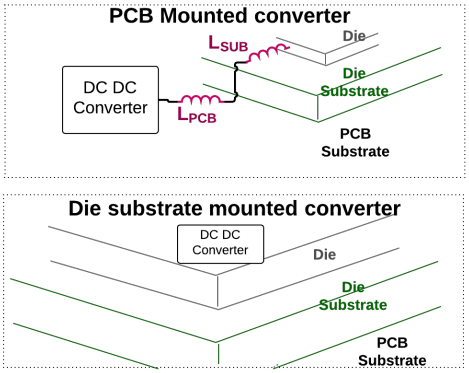

Figure 12: Inductive path between converter and load. The control feedback path is much slower in the PCB mounted converter.

speed I/O, such as processor to processor interfaces creates a performance corner requirement for DC/DC converters. For reliable chip operation, the converter must be able to respond to transient I×R drop at the I/O buffers V_{CC}. Because of the long control sense and signal path between an off chip converter and I/O buffer, large parasitic inductance along this connection increases delay in this power converters response time to transient I×R drop. This delay attenuates I/O signals by reducing the drive strength of I/O transmission buffers and reduces the maximum speed of I/O. Integrated converters can respond to transient droop faster and so improve signal integrity.

5.2 Saving pins with DC/DC converters

The literature demonstrates integrated power converters capable of replacing external converters. A small subset of this literature considers input voltage above those common to Li-Ion batteries. Although the component literature and select converter architectures identified in section 4 show promise for application to this problem, many combinations from this collection of parts have not been explored. Therefore the performance of integrated converters in high voltage is an open research question.

Practical high power, high voltage integrated converters are the enabler for pin count optimization as they define the lower bound of pins required for a given power envelope.

Literature previously reviewed in this paper finds active and passive components capable of driving a spectrum of processor power loads. Reviewed literature has also reported integrated converters capable replacing external converters. However up to this point the report has focused on systems operating at input voltages of $4.5V$ and lower. With high voltage switches reviewed, state of the art in high voltage integrated converters are reviewed in this section.

As high power density passives are nascent, there is a dearth of literature on high voltage integrated converters owing to their impracticality as LDO replacements. Two representative designs are reviewed below that attempt to circumvent the limitations of commonly available low power integrated passives.

5.2.1 High voltage SC-Buck

Pilawa et al. [36] Implement a twin stage step-down converter that is a hybrid SC and Buck design. high voltage input is stepped down by an SC phase as pre-regulation. The output of the pre-regulator is input to a secondary Buck phase, which cleans the noisy SC voltage with its filter and provides an analogue range of low voltages.

Pilawa et al. [36] implement a semi-integrated design. They achieve relatively high power density of 0.8W with off die passive components. High input voltage is handled with LDMOS (triple well) switches, which increases the operating voltage at the cost of switching speed. Since the Buck stage operates within nominal bulk supply voltage, its power switches operate much faster. This improves the realizable Z_O regulation speed. LDMOS switches are a technology option of the CMOS process chosen in the work. They limit the design input voltage to 5V and are a significant source of loss.

With more closely integrated passives and improved switches, the ideas of this work could mature into a practical candidate for high voltage integrated power converters.

5.2.2 High voltage substrate transformer-Buck

High voltage DC/DC converters (5v+) miniature power converters exist as PCB substrate integrated devices. With semi-integrated converters emerging as viable replacements for off chip converters, we consider the limit of semi-integration. Much of the reviewed literature integrates passive components on to die substrate ([36], [7], [50] etc.). Gong et al. [14] is an example of substrate integration for high voltage, high energy density power converters. The design embeds a miniature transformer coil and inductor coil in a 6 layer PCB substrate. The control IC, power switches and capacitor are mounted on this substrate. This design operates in the high voltage high power, high efficiency corner. Metrics are respectively 48V, 300W and 96% peak.
This level of substrate integration and power output has several drawbacks. The primary issue for pin count optimization is substrate area consumed by planar power components blocks vias and constrains pin routing.
Designs such as that of Gong offer a potential means for high voltage efficient converters but have a high component cost and area penalty in the substrate. This limits their appeal for increasing pin count, despite their demonstrated utility in supplying power.

We conclude on the state of the art by identifying a lack of exploration in high voltage integrated converters. Practical semi-integrated approaches were found but have limited power capabilities or limited appeal for pin optimization.

5.3 Directions for future work

An evolutionary comparison of work is presented in Table 3.
Moving beyond these works we define a research goal of high voltage, efficient and energy dense integrated power converters for investigating the lower bound power to I/O pin ratio of digital chips.
Several reviewed converter implementations can be eliminated given this goal:

- **Standard CMOS SC/Buck converters:** Standard CMOS converters do not operate efficiently enough to reduce the power to I/O pin ratio
- **Mini-transformer:** Planar substrate transformer and inductors block both I/O and power pins
- **Bond wire inductors:** Consuming substrate pin pads for power inductors can never reduce the power to I/O pin ratio

Some augmentation to the reviewed literature is now postulated.

5.3.1 LDMOS High voltage SC-Buck

Pilawa's work [36] is a potential application for relatively slow switching high voltage LDMOS.
LDMOS transistors cannot operate fast enough to provide the tightly controlled converter required for high bandwidth I/O, neither is an SC converter suited to an efficient transient load regulation. However the pre-regulated capacitors are excellent charge wells for decoupling. This allows a faster switching Buck regulator to provide a clean voltage with fast transient response, since there is negligible inductance between the charge well and filter. This is the main advantage of such a design.
Realizing the potential benefits require several research questions be addressed.

Power Density: Pilawa's semi-integrated solution to the power density issue of integrated capacitors may be questioned and alternate avenues explored. Although power density of Pilawa's work is relatively high it is below that of Cheng [18], Strucken [45], [46] and other semi-integrated converters. As such Pilawa's power density is presently unattractive. The semi-integrated approach of passives may also be further explored as Pliawa's design mounts the power capacitors to the die substrate, introducing a far larger parasitic impedance than Sturcken and Intel's *Si* interposer mounted inductors. The trade-off in energy density and charge cycle periods of deep trench [4] and ferroelectric capacitors [11] employed by El-Damak and others could be weighed against those of substrate and interposer mounted power capacitors.

Efficiency: The design has a double power train and therefore double parasitic losses. The design is also complex for component value optimization since the SC and Buck create a complex filter, however an observation is this complexity may be subject to component reduction architectural methods similar to flying capacitor Buck.

5.3.2 GaN Interposer Buck:

Silicon interposer Bucks represent the state of the art in performance [49], [46]. In addition the interposer enables I/O optimization to be explored aggressively via the directions of 3D and 2.5D integration.
Although the *Si* interposer design has an attractive output operating point envelope, research questions relating to its regulation capability of high voltage V_{In} should be addressed.

Design	Converter type	Integration	Special technology	Efficiency	Energy density
Substrate transformer [14]	transformer Buck	None	none	96% peak	$1.5W/mm^2$*
CMOS Buck [53]	Buck	Full	none	58% peak	$0.2W/mm^2$
Bond wire Buck [17]	Buck	Semi	none	82.4% peak	$0.86W/mm^2$
Deep trench SOI SC [4]	SC	Full	SOI & deep trench capacitors	86% peak	$4.6W/mm^2$
Thin film inductor Buck [46]	Buck	Semi	Interposer & thin film inductors	69% nominal	$22.6W/mm^2$
SC inductor Buck [36]	SC Buck	Semi	Unknown	81% peak	$0.08W/mm^2$

Table 3: Evolution of integrated DC/DC converter circuits **reduced to two dimensions by dividing over depth of substrate*

Power Density: The question of high voltage input may be explored via the 2.5D space of the *Si* interposer. Energy dense non standard passives and high voltage power switches reviewed in section 4 could be used to investigate an optimum pin ratio for high V_{In} while retaining a standard CMOS digital die. The performance of GaN switches and Ferroelectric deep-trench capacitors alongside thin film inductors is as yet unknown. All of these technologies could feature in a single integrated converter with an aggressive application of the interposer

The limit of I/O density: A tangential exploration of processor I/O density leveraging interposers is presented by Gokul et al. [26]. Interposers are used to reduce memory I/O pins on the die substrate by sandwiching a Si interposer between memory and digital logic. The interposer mounted inductors used by Strucken and Intel could be integrated into such an interposer, with the Buck converter used to optimize the I/O and memory bandwidth to digital logic.
However, the weakness of the interposer Buck with respect to a SC-Buck is its lack of a large local charge well, making the design rely on traditional decaps on the digital CMOS chip to mitigate transient $I \times R$ droop. A line of research inquiry may address this with the energy dense capacitors reviewed in Section 4.

6 Conclusions

Integrated step-down DC/DC converters show promise as a means to optimize I/O pins in terms of count and performance for high performance digital CMOS chips. Integrated converters may improve power efficiency and power integrity for digital circuits and I/O buffers as well as reducing the required number of core logic supply pins. The state of the art demonstrates some of this utility, but research is required to explore the full potential of integrated converters.
The limits of converter circuits and their components along with related research were reviewed.
Novel solutions and techniques applied to these limitations show potential in addressing the efficiency and energy density issues of integrated converter circuits. However the question of optimally integrating the reviewed work for a given digital CMOS chip design remains open owing to the dearth of collaboration between specialists in each problem area.

With a goal of I/O pin optimization, we conjecture on advancing knowledge in the area based on the power integrity problems of high speed I/O and the reviewed work. The low latency $I \times R$ droop response and high quality output regulation required may be possible by furthering the twin stage converter work of Pilawa [36] as this architecture features a coarse grain low latency charge well in the SC phase in support of a low drive strength high quality output line in the Buck phase.
Alternatively, the better performing interposer Buck of Sturcken [46] could be further augmented with high performance passives identified in Section 4 to operate at higher input voltages with high performance on-chip decoupling capacitors to address transient $I \times R$ droop.
In closing, this review suggests that at it's core, miniaturizing DC/DC converters is governed by advances in device physics. A disruptive discovery in this field could rapidly change the focus and goals of researchers working to advance I/O bandwidth by leveraging integrated DC/DC converters in the future.

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