

# Saving pins and power with integrated voltage converters

Michael Barrow

*mbarrow@eng.ucsd.edu*

*University of California, San Diego*

## Abstract

Recently, demand for increased processor performance coupled with reducing power budget has been addressed using emerging parallel processors. Parallel computation is an energy efficient (**cite chandrakasan**) way of increasing performance but requires wider interconnect busses. At the die boundary, the consequence is that systems face an IO bottleneck. The connection between silicon and substrate ends the scope of Moores law in a system, with IO density of packages increasing at a slower rate than on chip.

Compounding this problem, addressing performance by increasing parallel units result in increasing energy density due to the end of Dennard scaling (**cite**). Devices therefore require an increasing number of power pins, further limiting IO pin availability. **HOW ABOUT COMPELLING EXAMPLE?** We examine integrated power converters in this context. A review of the literature suggests with further research this technique could address the IO bottleneck of future processors.

## 1 Introduction

Against a backdrop of declining PC and growing smartphone sales, mobile devices drive demand for low power, high performance architectures. Emerging applications such as augmented reality, location aware services, high performance games and novel machine interfaces place an increasing demand for expanded IO capabilities and memory bandwidth from generation to generation of these devices. With the number of popular software stacks being lower than the number of major hardware vendors, device battery life is an important product differentiator. Research interest has therefore increased in power efficient architectures that can meet the IO and memory bandwidth requirements of the mobile segment.

package IO density is a well known problem to

architects. Marbell et al [4] review 130 hardware designs over 30 years and conclude the historical trend of package pin count and power pin count increase at an unsustainable rate. Promising solutions have been proposed, with Chang et al [3] identifying a subset of practical approaches in 2010. They conclude that voltage scaling as proposed by Dennard et al [1] is feasible, but enabled by a sum of techniques in different disciplines.

At the architectural level, power converter integration is advised in the worst case, where challenges of sub-threshold leakage prevent further reduction of CMOS voltage and power density prevents further integration of IO intensive system blocks such as memory. The observation in [3] is that reducing CMOS voltage has an exponential impact on loss through the power delivery pins. By maintaining pin voltage to devices and reducing operating voltage of CMOS using an efficient on die DC DC voltage converter bridge, an IC has a higher effective power density without increasing the number of power pins.

Research into integrated DC DC converters has been an active topic pre-empting [3] for other architectural benefits. As will be seen in detail in section **SECTION No**, DC DC converters typically feature bulky passive components. These increase the cost and footprint of mobile systems. Additionally, battery technology does not enjoy the improvement rate of CMOS, so operating voltage drops have opened a gulf between Battery supply voltage and IC input voltages. Techniques for extending battery life such as multiple voltage domains mean CPU's require multiple supply voltages. The symptoms of this are seen in the **Qualcomm snapdragon 800 which features 9 off chip DC DC converters CITE**. Against this backdrop, the feasibility of integrated DC DC converters shown by Kurson et al [2] invigorated research interest of integrated DC DC converters. A major motivation is removing the space and component costs of off chip converters **CITE A bunch of papers**

that feature this in abstracts.

State of the art in integrated DC DC converters is exemplified in Intel Haswell CPU's FIVR. Although a comparable DC DC converter exists in the literature [5], to the authors knowledge this is the only example of an integrated DC DC converter supplying a general purpose CPU.

Intel's literature [6] suggests the FVIR is employed primarily to remove external DC DC converters and improve power efficiency. However a comparison of the pinout between Haswell Cite and the non FIVR predecessor Ivybridge Cite suggests that some power pins were saved too. This is unsurprising as Kurson notes in [2] that power pins could be saved by integrated DC DC converters. As we note DC DC converters improve the IO density problem, we review the literature to asses the feasibility of optimizing power pins to IO pins by increasing supply voltage of an integrated DC DC converter greatly beyond typical CPU operating voltage.

The rest of the document is ordered as follows:

- The operation of the DC DC converter and its critical design parameters
- Challenges associated with integrating DC DC Converters on die
- Performance limitations of monolithic CMOS DC DC converters
- Practically implementing integrated DC DC converters
- Methods of optimizing IC pin out with integrated DC DC converters
- Conclusions

## 2 The DC DC converter

### Definition of the problem

Two popular stepdown converters in the literature are presented. A review of the literature highlights critical properties the topologies must feature in order to integrate either on chip.

### 2.1 Switched Capacitor stepdown converter operating principle

Two types of DC DC step down converter are popular in the literature. Type 1 is the switched capacitor (SC) converter. a simplified canoical  $\frac{1}{2}$  series-parallel step-down topology is shown in Figure 1.

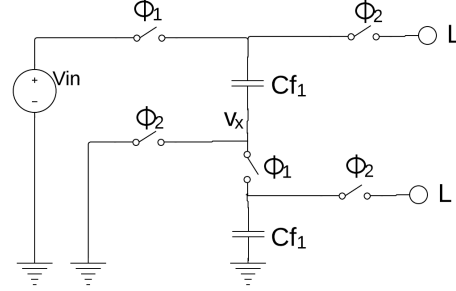


Figure 1: A  $\frac{1}{2}$  stepdown SC topology

Let us consider the circuit with ideal components.  $Cf$  denotes some capacitance such that  $Cf_1 = Cf_2$ . switches are controlled by mutually exclusive clocks,  $\phi_1$  and  $\phi_2$ . These clocks are non-overlapping.

The circuit has two phases of operation. In phase 1, the charging phase,  $\phi_1$  switches are closed and  $\phi_2$  switches are open.  $Cf_1$  and  $Cf_2$  are in series. Since the capacitors are the same size,  $V_x$  is  $\frac{1}{2}$  of  $V_{in}$ .

In phase 2, the discharging phase,  $\phi_2$  switches are closed and  $\phi_1$  switches are open. Now  $Cf_1$  and  $Cf_2$  are in parallel. Since they are matched in size,  $V_x$  remains at  $\frac{1}{2}$  and is seen at terminal  $L$ .

### 2.2 Inductor-capacitor stepdown converter operating principle

The second popular converter is the inductor-capacitor stepdown (buck) converter. A simplified canoical topology is shown in Figure 2.

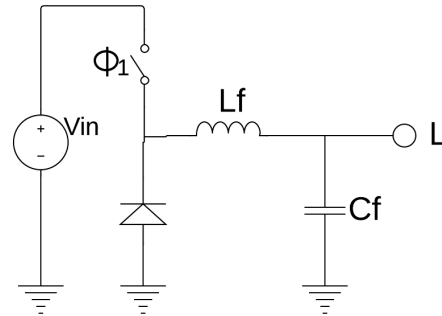


Figure 2: An inductor capacitor buck topology

The voltage conversion principle is understood by considering the inductor and capacitor as a high pass filter.  $\phi_1$  is a clock used to generate a square wave voltage of amplitude  $V_{in}$ . If this square wave is at a frequency

sufficiently higher than the 3db cutoff frequency of the filter, only the DC component of the square wave is observed at  $L$ . Because of this, buck converters may change their voltage stepdown ratio during operation, by modulating  $\phi_1$ . For a properly designed converter,  $V_L$  is defined by the duty cycle "D" ?? of  $\phi_1$  where:  $V_{out} = V_{in} \times D$ . In other words, if the square wave entering  $L_f$  is high for  $\frac{2}{3}$  of its period,  $V_{out} = \frac{2}{3} \times V_{in}$  and  $D = \frac{2}{3}$ .

## 2.3 SC stepdown converter critical parameters

We re-draw Figure 1 with non-ideal components in Figure ?? Note the **introduction of  $\phi_2$** . This is introduced so when  $Cf_2$  has discharged to the load,  $Cf_1$  may be connected to restore the supply voltage seen at node  $L$ . **we do this because the parasitic resistance of  $Cf_1$  and  $Cf_2$  is larger in series, maintaining  $V_{out}$  for longer (also fucks with your load impedance, why do it??!!)WE SEE THAT IT IS CRITICAL TO HAVE HIGH FREQUENCY IN ORDER TO MAINTAIN SUPPLY VOLTAGE**

## 2.4 Inductor-capacitor converter critical parameters

How it works, critical parameters

## 2.5 Problems of an Integrated DC DC Converter

**Definition of the system problem lives in**

History of research

System type 1(Switched capacitor AND HISTORY)

**Problems of bottom plate parasitic cap**

System type 2(Integrated buck AND HISTORY Kurson book)

Want to show how General CMOS components are made for this role and why they didn't work.

## 2.6 Performance drawbacks of Baseline DC DC Converters

**Taxonomy of problem (deeper drill and more specifics of the problem)**

what is wrong with the switches?

what is wrong with the control?

What is wrong with the capacitors?

What is wrong with the inductors?

## 2.7 Solutions

**System: well defined, class of problems: well defined, now we will see "fixed" systems**

- Switches fixes paper list and description DONT USE EXOTIC TECH! THESE WERE NEVER USED ON INTEGRATED DESIGNS!!!
- Control fixes paper list and description NOTE THAT THIS PROBLEM IS WELL UNDER CONTROL, CONCLUDE FROM THIS SECTION
- Capacitor fixes paper list and description NOTE THAT THIS PROBLEM CANNOT BE "SOLVED" FROM A SC TOPOLOGY POINT OF VIEW AND INDUCTORS ARE "BETTER" IN TERMS OF ENERGY DENSITY AND LINE REGULATION
- Inductor fixes paper list and description. NOTE THAT THIS IS "SOLVED" BUT FOR SEMI-INTEGRATED OR WHATEVER

## 3 Saving pins with DC DC converters

**Solutions & Stakeholders, why is there still work to be done?**

Need to define the problem of Signal to power pin ratio. We cannot optimize this today with DC DC converters, because the CMOS voltage stepdown means we need to have a lot of CORE power pins.

Our "stakeholder" is high voltage stepdown. If we do it we could reduce **DEFINE**"CORE POWER PINS" to an amount desirable for **DEFINE** signal integrity

### 3.1 The IO limit with integrated DC DC converters

**Defines stakeholder specific problem**

Think about this, it has to be differentiated from the section above

### 3.2 Solutions

Here we have to talk about:

3 the micro transformer solution to this problem (it could be made promising)

2 the MIT solution to this problem (it does not look promising)

1 the disruptive technology of Si on Insulator, and how it could be paired with interposers

In the mobile segment Silicon interposers can be used to solve the IO problem as seen in [Ultra-high I/O Density

Glass/Silicon Interposer for high Band-width Smart Mobile Application].

This interposer allows signal integrity to be maintained at low voltage from the interposer to memory. a High voltage from the substrate and DC DC converter integrated to the interposer allows power density to be met with fewer pins on the package. In this scenario, the package can be made smaller to allow denser integration, or the io bandwidth can be bound to signal integrity requirements...

**SHOULD HAVE SOME SIMULATION TO CHECK INSIGHT ON 1, 2 and 3**

### 3.3 Conclusions

Basically conclude that given the solutions simulation we could reach a situation where IO pressure is lifted from core power perspective, but that isn't so great tbh.

### References

- [1] DENNARD, ROBERT H., F. H. G. V. L. R. E. B., AND LEBLANC., A. R. Design of ion-implanted mosfet's with very small physical dimensions. *Solid-State Circuits, IEEE Journal of* 9.5 (1974), 256–268.
- [2] KURSUN, VOLKAN, S. G. N. V. K. D., AND FRIEDMAN., E. G. Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 11.3 (2003), 514–522.
- [3] L CHANG, D FRANK, R. M. S. K. B. J. P. C. R. D., AND HAENSCH., W. Practical strategies for power-efficient computing technologies. *Proceedings of the IEEE* 98.2. (2010), 215–236.
- [4] STANLEY-MARBELL, PHILLIP, V. C. C., AND LUIJTEN., R. Pinned to the walls: impact of packaging and application properties on the memory and power walls. *Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design*. 50 (2011), 51–56.
- [5] STURCKEN, NOAH, E. O. N. W. P. H. B. W. L. R. M. P., AND SHEPARD, K. A 2.5 d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer delivering 10.8 a/mm<sup>2</sup>. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International* (2012), 400–402.
- [6] TED-DIBENNE II, J., M. P. R. P. M. C. K. W. P. Z. T. F. L. X. M. S. W. S. E. F. R., AND PAUL., F. A 400 amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors., 2010.

### Notes

<sup>1</sup>Remember to use endnotes, not footnotes!