Saving pins and power with integrated voltage converters

Michael Barrow
mbarrow@eng.ucsd.edu
University of California, San Diego

Abstract

Recently, demand for increased processor performance coupled with reducing power budget has been addressed using emerging parallel processors. Parallel computation is an energy efficient **(cite chandrakasan)** way of increasing performance but requires wider interconnect busses. At the die boundary, the consequence is that systems face an IO bottleneck. The connection between silicon and substrate ends the scope of Moores law in a system, with IO density of packages increasing at a slower rate than on chip.
Compounding this problem, addressing performance by increasing paralell units result in increasing energy density due to the end of Dennard scaling **(cite)**. Devices therefore require an increasing number of power pins, further limiting IO pin availability. **HOW ABOUT COMPELLING EXAMPLE?** We examine integrated power converters in this context. A review of the literature suggests with further research this technique could address the IO bottleneck of future processors.

1 Introduction

Against a backdrop of declining PC and growing smartphone sales, mobile devices drive demand for low power, high performance architectures. Emerging applications such as augmented reality, location aware services, high performance games and novel machine interfaces place an increasing demand for expanded IO capabilities and memory bandwidth from generation to generation of these devices. With the number of popular software stacks being lower than the number of major hardware vendors, device battery life is an important product differentiator. Research interest has therefore increased in power efficient architectures that can meet the IO and memory bandwidth requirements of the mobile segment.

package IO density is a well known problem to architects. Marbell et al [38] review 130 hardware designs over 30 years and conclude the historical trend of package pin count and power pin count increase at an unsustainable rate. Promising solutions have been proposed, with Chang et al [25] identifying a subset of practical approaches in 2010. They conclude that voltage scaling as proposed by Dennard et al [8] is feasible, but enabled by a sum of techniques in different disciplines.
At the architectural level, power converter integration is advised in the worst case, where challenges of subthreshold leakage prevent further reduction of CMOS voltage and power density prevents further integration of IO intensive system blocks such as memory. The observation in [25] is that reducing CMOS voltage has an exponential impact on loss through the power delivery pins. By maintaining pin voltage to devices and reducing operating voltage of CMOS using an efficient on die DC DC voltage converter bridge, an IC has a higher effective power density without increasing the number of power pins.

Research into integrated DC DC converters has been an active topic pre-empting [25] for other architectural benefits. As will be seen in detail in section **SECTION No**, DC DC converters typically feature bulky passive components. These increase the cost and footprint of mobile systems. Additionally, battery technology does not enjoy the improvement rate of CMOS, so operating voltage drops have opened a gulf between Battery supply voltage and IC input voltages. Techniques for extending battery life such as multiple voltage domains mean CPU's require multiple supply voltages. The symptoms of this are seen in the **Quallcomm snapdragon 800 which features 9 off chip DC DC converters CITE**. Against this backdrop, the feasibility of integrated DC DC converters shown by Kurson et al [23] invigorated research interest of integrated DC DC converters. A major motivation is removing the space and component costs of off chip converters **CITE A bunch of papers**

that feature this in abstracts.

State of the art in integrated DC DC converters is exemplified in Intel Haswell CPU's FIVR. Although a comparable DC DC converter exists in the literature [40], to the authors knowledge this is the only example of an integrated DC DC converter supplying a general purpose CPU in such a power envelope.
Intel's literature [42] suggests the FVIR is employed primarily to remove external DC DC converters and improve power efficiency. However a comparison of the pinout between Haswell **Cite** and the non FIVR predecessor **Ivybridge Cite** suggests that some power pins were saved too. This is unsurprising as Kurson notes in [23] that power pins could be saved by integrated DC DC converters. As we note DC DC converters improve the IO density problem, we review the literature to asses the feasibility of optimizing power pins to IO pins by increasing supply voltage of an integrated DC DC converter greatly beyond typical CPU operating voltage.

The rest of the document is ordered as follows:

- Section 2 outlines the operation of the DC DC converter and its critical design parameters
- Section 3 describes the design and associated challenges of integrating DC DC Converters on die
- Performance limitations of monolithic CMOS DC DC converters
- Summary of recent research in integrated DC DC converters
- Methods of optimizing IC pin out with integrated DC DC converters
- Conclusions

2 Operation of the DC DC converter

Definition of the problem
Two popular stepdown converters in the literature are presented. A review of the literature highlights critical properties the topologies must feature in order to integrate either on chip.

2.1 Switched Capacitor stepdown converter operating principle

Two types of DC DC step down converter are popular in the literature. Type 1 is the switched capacitor (SC) converter. a simplified canoical $\frac{1}{2}$ series-parallel step-down topology is shown in Figure 1.

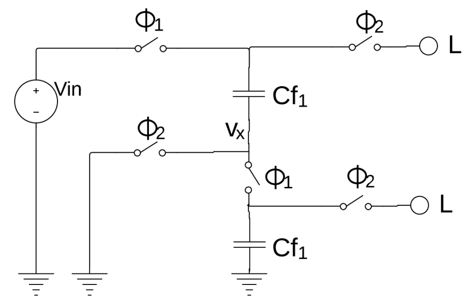

Figure 1: A $\frac{1}{2}$ stepdown SC topology

Let us consider the circuit with ideal components. Cf denotes some capacitance such that $Cf_1 = Cf_2$. switches are controlled by mutually exclusive clocks, ϕ_1 and ϕ_2. These clocks are non-overlapping.
The circuit has two phases of operation. In phase 1, the charging phase, ϕ_1 switches are closed and ϕ_2 switches are open. Cf_1 and Cf_2 are in series. Since the capacitors are the same size, V_x is $\frac{1}{2}$ of V_in.
In phase 2, the discharging phase, ϕ_2 switches are closed and ϕ_1 switches are open. Now Cf_1 and Cf_2 are in parallel. Since they are matched in size, V_x remains at $\frac{1}{2}$ and is seen at terminal L across both capacitors.

2.2 Inductor-capacitor stepdown converter operating principle

The second popular converter is the inductor-capacitor stepdown (buck) converter. A simplified canoical topology is shown in Figure 2.

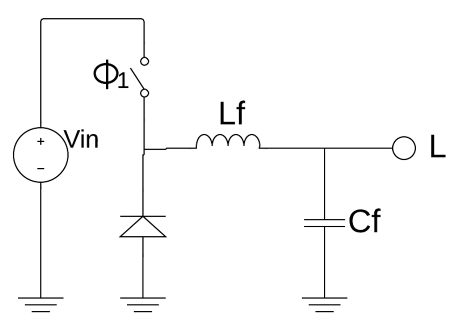

Figure 2: An inductor capacitor buck topology

The voltage conversion principle is understood by considering the inductor and capacitor as a low pass filter. ϕ_1 is a clock used to generate a square wave voltage of amplitude V_{in}. If this square wave is at a frequency sufficiently higher than the 3db cutoff frequency of the filter, only the DC component of the square wave is observed at L. Because of this, buck converters may change their voltage stepdown ratio during operation, by modulating ϕ_1. For a converter when current always flows in L (CCM mode), V_L is defined by the duty cycle "D" [22] of ϕ_1 where: $V_{out} = V_{in} \times D$. In other words, if the square wave entering L_f is high for $\frac{2}{3}$ of its period, $V_{out} = \frac{2}{3} \times V_{in}$ and $D = \frac{2}{3}$.

2.3 SC stepdown converter critical parameters

The energy that a SC converter can transfer per charge cycle is $E_{Isc} = CV^2$. We could therefore express $W = E_{Isc} \times F_{\phi}$.
V For a design with a given V_in and ideal components, the designer has two degrees of freedom to power a load, C and F_{ϕ}.
We re-draw Figure 1 with non-ideal components in Figure 3.

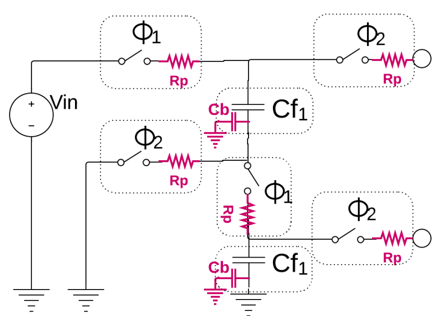

Figure 3: An SC topology with major parasitic components

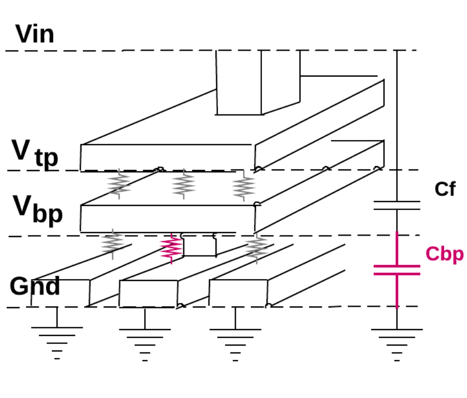

Figure 4: Bottom Plate parasitic capacitance

By observation of Figure 3 and Figure 4 we see that F_{ϕ} and C are critical parameters that must be optimised for minimum losses
Switching losses Losses associated with switches are switching loss during the non-overlapping period of ϕ, and conduction loss due to the equivilent series resistance (ESR) of switches.
Conduction loss reduces the supply voltage seen at the capacitors by a factor δV_a. Conduction loss is therefore sensitive to the stepdown ratio. Increasing the stepdown ratio increases the number of series switches between all capacitors during the charging phase. For example a ratio of $\frac{1}{3}$ has 2 series switches, one of $\frac{1}{4}$ has 3 series switches and so on.
Capacitor losses Losses associated with capacitors are parasitic capacitance losses. A parasitic capacitance known as bottom plate capacitance exists between one plate of each capacitor and ground. The voltage of these parasitic capacitor is a virtual ground and reduces the supply voltage seen at the capacitors by δV_b. Their charge can leak to true ground but cannot reach a load. As they are smaller than useful capacitance, they are significantly charged and discharged on each cycle of the converter. Loss is therefore expressed as $W = E_{Pc} \times F_{\phi}$ where $E_{Pc} = 1.5\alpha CV^2$. Literature reports bottom plate capacitance to be up to 5% of C_{tot} [33]. We also note that F_{ϕ} is adjustable at runtime yet C is not and that $I_{out} \propto C$ [9] as well as F_{ϕ}.
Circuit noise SC converters are relatively noisy compared with buck converters because they do not have the built in output filter of the buck. Output noise is therefore strongly related to bounce of the power switches and high inrush current to the power capacitors [46]. As such characterisation of the noise depends on switch and capacitor device parameters, with mitigation achieved through careful switch design and timing control to reduce high frequency noise.

In SC converters then, careful design considering voltage specification and technology parameters optimises converters to their load, with noise being addressed via control circuitry.

2.4 Inductor-capacitor converter critical parameters

Owing to the similar basic components employed in the buck converter, critical parameters are first identified by differentiating the circuits at the component level. Next, inductor losses are breifly reviewed. Finally, buck transient behaviour is more complex than SC. A brief overview of power and noise in the circuit is therefore provided as an aid to understanding trade-offs for the critical circuit parameters. We re-draw Figure 2 with non ideal components in Figure 5.

The extra MOSFET is common in the literature and

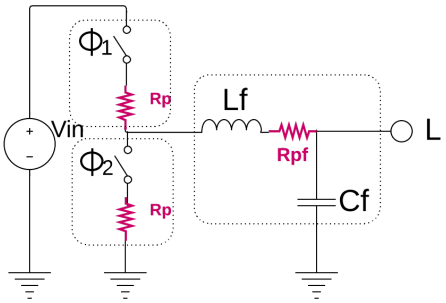

Figure 5: An SC topology with major parasitic components

replaces the diode of Figure 2. Introducing this device gives buck and SC converters a common power switch loss mechanism at each phase of operation, but the buck features fewer switches contributing to losses.

Inductor Losses: We now consider the inductor parasitics, given all other power train components are common with SC converters.
Losses associated with the inductor are dominated by equivilent series resistance (ESR). Standard CMOS only permits for planar inductors. Increasing inductance is acomplished with a spiral coil to increase flux linkeage. High inductance requires high numbers of coils per unit area, which translates to increased resistance through the coil.
Besides the ESR, the series connection with capacitor C introduces extra impedance Z_{LC} determined by the F_{Sw} of the buck. It is critical to match L to F_{Sw} and C to minimise this impedance, but the ESR may never be removed.

Circuit noise: With the voltage step-down principle understood we consider the circuit in Figure 2 from a current perspective. We cannot directly apply Kirchoffs law due the AC variation of I with T. However $P_{In} = P_{Out}$ for conservation of energy. Power can only enter the system when current flows through the closed switch from V_{In}. Due to the Diode, its path to the load must be through the inductor. Inductors impede current less as they are charged, therefore for a some T_{On} High P can be transferred into the system if either;
A: L is small relative to T_{On}
B: T_{On} is large relative to L
We consider that during T_{Off}, the inductors charge dissipates through the rest of the circuit as current driving the load and parasitic components. Let $T = T_{On} + T_{Off}$ and $F_{Sw} = \frac{1}{T}$ so now A and B correspond to designing a buck with either;
C: A high F_{Sw} and small L
D: A low F_{Sw} and high L
Since the voltage step-down principle is understood, it follows that the choice of L determines the choice of C to minimise Z_{Out} at the desired operating curve of V_{Out} for a given F_{Sw}.
Another intuitive observation is that lower P requirements result in L and F_{Sw} values that are easier to realise for given technology limitations, since $P \propto L \times F_{Sw}$. More precisely $P = V_{Out} \times \frac{V_{In}(1-D)}{2L} DT$ for the maximum load condition.

As with any analogue AC circuit, transient operating point complicate the choice of components. A breif overview of solutions provides context for evaluating component loss and trade-off. A given load has operating corners that must be satisfied. The following parameters are used to design operating point behaviour for a buck:

- **Current ripple, Δi_{Out}:** Tollerable current variation through the load
- **Voltage ripple, Δv_{Out}:** Tollerable supply voltage noise at the load
- **Switching frequency F_{Sw}:** Nominal switching frequency of the power switches, lower reduces loss but increases Δv and Δi
- **Operating voltages V_{In},V_{Out}:** Nominal input and output voltage of the converter
- **Maximum drive power P:** Converter Power at the highest DC load. $P = V_{Out} \times I_{Max}$

Δi,Δv,V_{Out} and P are constraints specified by the load. V_{In},F_{Sw} along with the passive components C and L must be chosen to satisfy the load constraints as well as technology constraints.

Current ripple: Digital circuits require low supply ripple for deterministic operation. Supply current ripple is defined as
$\Delta i_{Out} = \frac{(V_{In}-V_{Out})D}{2LF_{Sw}}$ [22]
The current flow principle of the buck is understood, so it is unsurprising that this formulae does not involve C **Voltage ripple:** Digital circuits require low voltage ripple for reliable operation. Typically $\frac{V_{In}}{10}$ is specified. Supply voltage ripple is defined as
$\Delta v_{Out} = \frac{(V_{In}-V_{Out})D}{16LCF_{Sw}^2}$ [22]
The voltage filtering behaviour of the buck is understood, so it is unsurprising that this formula involve F_{Sw}, L and C

In summary the loss mechanisms in the buck converters offer more degrees of freedom for optimisation than SC designs because of the additional component type of the inductor. The ripple formulae are useful in limiting aggresiveness applied to any particular parameter and can be used to balance the losses of power train components.

2.5 Converter load regulation concept

Load regulation is matching output impedance ”Z_O” of a power converter to a current load. Because $I = \frac{V}{Z_O}$ and maintaining V for a processor is critical, converter output impedance must track quickly with the load condition to keep V constant. The responsibility of tracking load and adjusting Z_O belongs to control circuits. Block Diagrams are shown in figure **??**

Inductor-capacitor converters can reduce Z_O by increasing conductance. This is done by increasing ”D” in eqn**REF EQN**. Because the asymtote is impedance of the filter at F_S, Z_O may also be increased by reducing F_S. [2].

SC converters power loads capacitively. Because the capacitors supply a DC load in parallel, Z_O cannot be lowered below $Z_C + Z_{Sw}$ at the nominal F_{Sw}. Modulating F_{Sw} can increase impedance in practice, because the capacitors can be purposely under-charged [35].

3 Design of Integrated DC DC Converters

Practical integrated converters are emerging and designed with different goals. A taxonomy of reviewed literature identifies two groupings:

1: Power system replacement converters. The goal is to remove external VRMs with an equaly performing integrated subsystem

2: LDO replacement converters. The goal is an incremental improvement of the Low-dropout (LDO) regulators that have long been integrated on chip **??**.

These differing goals result in different design tradeoffs. We focus on group 1 because of an efficiency reason. To explain, consider the operating principle of an LDO. A transistor gate is biased in its linear conduction region and a fixed voltage is dropped from source to drain to give desired V_{Out}. Recall power transfer efficiency, $\eta = \frac{R_{Load}}{R_{Load}+R_{Source}}$. For an LDO, (**MAX**)[$\eta$] = 0.5. Using a comparable integrated converter to optimize power pins is intractable because around half the power budget is wasted as heat, clearly a sub-optimal design. As such, literature aiming at group 1 best aligns with our interest in pin count optimisation.

3.1 Motivation

Switching converters such as the SC and buck can offer far higher efficient energy transfer than linear types. Theoretical efficiencies have been modeled at 96% [**?**] using state of the art devices. Integrated buck and SC implementations have been reported with 84% [15] and 93% [9] efficiency respectively. Provided these power converters can drive the desired load of a processor, they could be used to obtain an optimum IO to power pin ratio for a processor. This would be done by increasing the input voltage to on die converters to reduce the number of supply pins until a desired number is reached.

3.2 Design challenges

An Integrated DC DC converter is optimized through design tradeoffs that consider component non-idealities. Given that CPU designs have differing power envelopes and CMOS processes have unique electrical properties, researchers have explored the design space at multiple entry vectors.

SC converters The entry vector is an argument that A: Capacitance is easy to implement because MOSFET gate capacitance is a basic building block of CMOS. No corresponding basic block exists for inductance. B: Inductors have a necessarily large parasitic impedance because they are made from coiled resistive wire. Capacitors have a lower minimum impedance which shrinks as the plate size or capacitance grows.

However, as we have seen this type of converter has less flexible output impedance as compared with buck converters. Also SC converters do not have a voltage regulating filter which is built-in to bucks. This makes their output voltage vunerable to switching noise.

Therefore the design challenges emphasised in SC converters are: maximising effective capacitance, controlling output impedance and regulating output voltage.

buck converters The entry vector is an argument that C: Inductors can be implemented in standard CMOS. D: Inductor based buck has been a preferred design for (¿100mW) applications over the past several decades [36], why change now?

3.3 Performance drawbacks of Baseline monolithic DC DC Converters

An example of a CMOS integrated SC converter [43] and CMOS integrated buck converter [3] are taken as examples. These designs highlight the performance drawbacks of baseline CMOS for integrated converters and explain the present concentration of research interest in this field. These setbacks from the initial entry vectors of the SC and buck camps also explain the research and design approaches taken in more recent work. Although one process generation separates the designs, they are reasonably compared since the power components (capacitors, inductors and switches) consume almost all of the die in both designs.

SC drawbacks Naive Integrated SC converters have a low power density. [43] realize an on die capacitance of 1600pF with a converter power density of $1.7mW/mm^2$. In comparison the baseline buck [3] realize on die capacitance of 1.1nF with a power density of $20mW/mm^2$. The baseline SC converter also realizes much lower efficiency than expected in[43]. 80% is predicted in the literature, but only 62% is achieved due to unmoddled losses.

Only a single step-down voltage ratio is implemented, since the fixed SC circuit topology described earlier is used.

The performance of this design focussed researchers in areas to make SC integrated converters attractive in replacing off chip IC power converters. Broad categories and related research are listed below.

- **Energy density:** Device technology research to improve capacitor energy density
- **Efficiency:** Technology, circuit topology and converter control research to reduce power leakage
- **Flexibility:** Improve load regulation with SC power circuit topology and SC converter control research. In other words, provide flexible step-down ratio's.

buck drawbacks Although power density is higher than the baseline SC, it is still too low for contemporary processors. The combined area of the converter and load must feature an power density higher than that dissipated in the load **GET A GOOD REF OF POWER FOR MOBILE CPU'S**

Naive Integrated buck converters have a low efficiency. [3] achieve a peak efficiency of 46%. Not only is this lower than the baseline SC [43], its lower than an LDO (50%).

Unlike the SC design, the baseline buck can implement a range of stepdown voltages in a basic topology. However the baseline has poor load regulation. At its lowest output voltage it has a 25% efficiency in its most sophisticated operating mode. This drops to 13% in its baseline mode.

As with the SC design, the issues in this and other early monolithic converters led researchers to focus on areas for improvement to make integrated buck converters suitable to replace discrete IC's. Again we summarise broad categories and related research below.

- **Energy density:** Device technology research to improve inductor energy density
- **Efficiency:** Technology, buck circuit topology and buck converter control research to reduce power leakage
- **Flexibility:** Improve load regulation with buck converter control research. Buck converter voltage stepdown was better understood than SC, but poorly controlled

The broad categories of buck overlap those of the SC researchers. Therefore some research effort may transfer between the two designs and we also observe a merge between the seperate research entry vectors identified earlier.

This manifests at the device level, where both converters share the same need to reduce losses. We can list these basic blocks and consider their problems when applied to integrated power converters abstractly from the two converter topologies.

CMOS Switches: Besides conduction losses, CMOS switches also suffer static and dynamic parasitic losses due to non-idealities. All must be balanced for an optimised power switch.

TRANSISTOR DIAGRAM SHOWING CRITICAL PARAMS

Static losses are constant no matter if the MOSFET switch is on or off. They occur because the MOSFET does not have an infinite open circuit resistance. Static loss is therefore technology node dependent and impossible to remove completely. Static losses are contributed to by components from sub-threshold leakage and gate oxide leakage currents.

These losses are intrinsic to all transistor based switches, however tradeoffs possible in modern technology nodes for full integration are less optimal than older technologies. Aggressive technology scaling continuously increases transistor leakage[16], so that realising the highest compute performance results in switches with the lowering efficiency in fully integrated designs.

Dynamic losses occur due to toggling the MOSFET switches. Power is consumed by changing the switch condition. As such, losses can be reduced by controlling switch toggling frequency, since for a given technology loss of the power switches and drivers increases by approximately $\sqrt{F_s}$[4]. However given fixed size energy transfer components, reducing F_s reduces the converters power rating since $P = F_s \times E$.

Conduction loss occurs because the MOSFET switch does not have a zero on resistance. At a DC operating point, the conduction loss is simply the resistance of the MOSFET. Resistance of a MOSFET may be reduced by decreasing its channel length, L_{ch} or increasing its channel width, W_{ch}. The minimum channel length is determined by process node e.g. 22_{nm} long in a 22_{nm} process, but channel width can be extended arbitrarily. However gate capacitance, $G_c \propto W_{ch} \times L_{ch}$. Reducing conduction loss therefore increases dynamic loss by increasing the power needed to charge G_c and toggle the switch.

As a final note, CMOS switches cannot operate reliably beyond the technology node voltage. This imposes limitations on the stepdown voltage ratio that can be achieved if a switch is connected between power rails. This does not impact loss but it does mean that the power a converter can supply is maximum when the stepdown ratio is $1:1$ **TRUE KINDA BUT JUSTIfy WITH EQN**

By considering a fully optimised switch, we see the pressing research problems are reversing the leakage trend[16] and operating with rail voltages above the target technology rating.

Capacitors: Capacitors suffer from time or frequency related losses due to non-ideality. The loss problem is complicated by the frequency dependence of capacitor impedance/reactance. This is encapsulated with $Q_c = \frac{1}{\omega C R_c}$, or the capacitors "Q" quality factor. If $Q_c = 1$, the capacitor is ideal and does not impede a voltage signal. The "Q" factor has a different level of criticality in SC and buck designs. buck designs can offset a low capacitor "Q_c" value with their inductor if properly designed.

DIAGRAM SHOWING CRITICAL PARASITICS

Because converters normally operate at a high frequency, Loss in the capacitor is typically due to its equivilant series resistance, R_c and its parasitic capacitance. The major parasitic capacitance component is formed between the ground node and bottom plate of the capacitor[9]. as noted previously CMOS may have up to 5% parasitic capacitance. This is more critical for SC designs since they must transfer all of their energy via capacitors.

Considering the loss mechanisms in a capacitor, improvements to integrated converters are not easily made at the architectural or circuit level. Important research questions involve critical technology parameters. We also observe buck converters are less sensitive to low quality capacitors.

Inductors: Inductors, similar to capacitors suffer from frequency related non-ideality as well as static DC loss. As such, they have a quality factor $Q_l = \frac{\omega L}{R_l}$. A $Q_l = 1$ represents a perfect inductor. In a standard CMOS process, $R_l \gg R_c$. This is because $L \propto \phi_{ind}$ where ϕ_{ind} is magnetic flux. In standard CMOS, ϕ_{ind} is increased by increasing the inductor length and hence increasing R_l. Contemporary CMOS has metal layers optimised for deep sub-micrometer components and design rules Conversely for a capacitor, increasing C requires increasing plate area and hence reducing R_c. For this reason SC designs cite low Q_l as their research motivation **CITE A BUNCH OF PAPERS THAT SAY THIS**.

Because the impedance of inductors is phase shifted from capacitors, buck converters can be optimized at the circuit level through component sizes. However, given their low Q_l due to high resistive loss, important research questions concern technology parameters critical to improving ϕ_l and reducing R_l.

4 Summary of recent literature

An evaluation of recent literature finds a volume of work addressing the previously outlined issues of integrated converters.

We review the literature beginning with work on the common building blocks of passive components and power transistors, then move on to review system level advances.

4.1 CMOS Switches:

Alimadadi et al.[3] propose an energy recycling mechanism to use the charge at the power switch gates as useful energy by pumping it to the load. The power PMOS and power NMOS gates are driven by stacked supply buffers to toggle the power switches. vss of the power PMOS gate buffer is vdd of the power NMOS gate buffer via an electrical connection at node x. by connecting node x to the load via a forward-biased diode, energy used to charge power MOS gate capacitance can also charge the load node, rather than sink to ground. The drawback of this technique is that the $\frac{1}{2}$ VSS swing of the power MOS gate nodes limits the amount of stepdown possible. It would therefore not translate to a high voltage stepdown.

Bathily et al.[6] also focus on energy loss in switch toggling. They propose an LC tank that resonates at F_s such that the power MOSFET switch gate voltages oscillate at this resonant frequency. If the power switch gate voltage is low the switching energy is stored in the tank. If the power switch gate voltage is high, switching energy is stored at the switch nodes. The authors find improvements in switch efficiency ranging from around $12-25\%$ accross the complete operating range. However the requirement is 16nH of inductance occupying 40% extra silicon area in a standard CMOS process. The technique is applicable in high voltage converters, but the 40% reduction of energy density makes it unattractive in medium to high power applications. Hyunseok et all.[29] address the higher than operating voltage step-down issue with circuit design and CMOS layout techniques. The circuit design handles higher than operating voltage by stacking power MOSFET devices in series such that each device does not drop more than the CMOS operating voltage. The sum of series voltage exceeds the operating voltage however. This technique is made novel with the circuit design of the power MOSFET switching inputs, which are toggled by operating voltage, despite the switch stacking. Although an arbitrary voltage stepdown could be achieved with power MOSFET stacking, this technique has diminishing returns for two reasons. Firstly, the conduction loss of the stacked power switches is summed, reducing efficiency. Secondly the switch toggling energy of the stacked power switches is summed since it is capacitive. This reduces the maximum F_s and therefore increases the required C or L for a fixed power envelope. As such this technique is less attractive as input voltage increases.

In the same high voltage vein, Bandyopadhyay et al[**?**] propose a buck converter with stacked power MOSFET switches. However, they use a single drain extended NMOS (DEnMOS) for high voltage and stacked PMOS devices. DEnMOS increases the reverse breakdown voltage of a MOSFET so that it will not short circuit at voltage above the technology operating vdd. An advantage of DEMOS is that no special process steps are needed. The main disadvantage of DEMOS in high voltage converters is high on-resistance and sensitivity to process variation. The limit of voltage step-down and current flow is around 30V at 2A [13] at which point non-standard CMOS process is required for reliable operation.

With the limit of DEMOS understood we consider the literature regarding switches suitable for high voltage and or high current.
For voltages above 20V at current above 1A, LDMOS switches outperform DEMOS. Hower et al[13] are paraphrased as follows: LDMOS devices have lower on-resistance than DEMOS but have a fixed device length, so transistors cannot be folded geometrically. LDMOS can be integrated into a low voltage technology node monolitically because they are compatible with bulk CMOS. The cost is an additional mask layer and therefore a non-standard process. A final drawback is LDMOS has a higher V_t, so they require more switching energy.

Finally in the high F_s high power design corner we consider AlGaN/GaN switches. Although much research effort has been made to improve power density and breakdown voltage, AlGaN/GaN switches outperform LDMOS in high-power high frequency switching applications [12]. This is because these switches have unique semiconductor properties beneficial to high voltage power conversion, such as; high operating frequency, high current density and high breakdown voltage[7],[10]. Krausse[20] summarises recent literature on power transistors graphically:

To conclude discussion on power switches, the

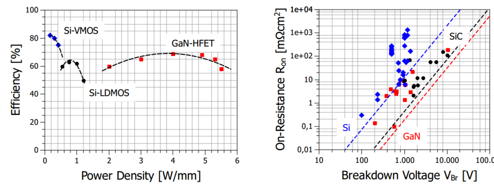

Figure 6: Comparative performance of power switch types, Reproduced from[20]

literature proposed novel circuit designs to improve switching efficiency. The limitations of these designs focus attention on the switch devices. The literature indicates as voltage and power density demands of a design increase, non-standard CMOS process and CMOS alternatives become increasingly attractive.

4.2 Capacitors:

After Viraj et al.[43], much research effort was expended regarding converter capacitor energy density and impedance modulation. Kwong et al.[24] address both issues uniquely. The load is a sub-threshold processor, which allows low-energy density capacitors to provide adequate drive. Converter impedence is reduced with technology options and circuit topology. Metal insulator metal (MIM) capacitors are used as power passives. MIM capacitors have the desirable qualities of being compatible with bulk CMOS and having a high Q_c. Their disadvantage is low energy density. Viraj et al.[43] observed an exponential deterioration of efficiency with mismatched load impedance. This work implements a re-configurable step-down voltage circuit, where output capacitors can be stacked for 4 step-down voltages or 4 converter impedances.
Kwong et al. stands alone in the literature because it uses a sub-vt processor load to mitigate low energy density where most literature attempts to improve it.

Regarding energy density, non-standard CMOS capacitors dominate contemporary integrated converter literature.
Since energy density is improved by reducing loss, early work explored the limit of CMOS with circuit techniques. Besides their other innovations, Kwong et al.[24] feature a charge recycling circuit. The operating principle is similar to [3], but the energy source is parasitic capacitance and bondwire inductance. The

Capacitor	Material	Permittivity (ε_r)
Bulk CMOS [34]	SiO2	3.9
High K CMOS [34]	HfSiO4	11
*Deep trench (structure) [18]	PZT	1000
*Ferroelectric [27]	BaTiO3	≈4600

technique was not implemented in later designs by the authors or others. Later work focuses on technology options for improving energy density. In CMOS compatible technologies, MIM [24] and Thin-gateMOS/fringe metal [**?**] capacitors are succeded by the exotic Deep trench [**?**] and Ferroelectric [9] capacitors.

Exotic capacitor types either greatly increase C per unit area because they realise an extremely high permittivity (ε_r). Capacitance may be calculated $C = \varepsilon_r \times \frac{A_p}{l_p}$ where A_p is the area of capacitive plates and l_p is the separation distance. * *example technologies, not used in reviewed designs* High ε_r can effectively negate bottom and top plate parasitic capacitance, since these capacitors could have an ε_r several orders of magnitude lower than the power capacitors.

To close on the topic of high ε_r, Deep trench and Ferroelectric capacitors designs do not exhibit multiple order of magnitude power density improvements over others. In these technologies, ε_r varies with greatly with temperature [27] and frequency **Get paper ref**. Further research is needed to understand their limits in power converters.

Another class of converters has gained prominence due to the difficulties of energy density in capacitors. Semi-integrated converters **Cite a bunch** use off-die capacitors as a charge source. Provided such capacitors can be connected to the rest of a converter with a very low inductive path, these designs offer higher drive capability at the cost of an extra component.

In summary of capacitors, early circuit level approaches to energy density have been superceded by non-standard CMOS. Architectural level approaches in SC designs have been successful in improving impedance modulation.

4.3 Inductors:

Since total inductance is improved by increasing mutual inductance within a conductor structure, researchers have made several attempts to improve Q_l with custom inductor layout. Angular spiral inductors were shown to have inadequate Q_l for efficient fully integrated power converters[3],[5], motivating exploration of alternate structures and materials. Meere et al. [28] characterized fully integrated racetrack style inductors for buck power converters. They find the *Cu* resistivity to dominate loss and to increase exponentially with F_s. They conclude 7mA as the supply limit of a converter with such inductors.

As with capacitors, the Q_l problem was also explored using semi-integrated converters. Researchers realised the parasitic inductance of bond wires could be re-purposed to become active power delivering inductance [44], [1]. This work received much attention owing to the high L of bondwire relative to integrated *Cu* spiral and racetrack inductors. In addition, since package inductance is a large contributer to power loss, end to end efficiencies have been realised up to 84.7% [15]. Owing to the relatively low resistivity of bondwire, energy density is also greatly improved with an I_{Out} of 1.2A reported [15].

Researchers have also combined innovations. L is enhanced when the core of an inductor is a high permiability material. $L \approx \frac{N^2 \mu A_L}{l_L}$ where μ is the permeability of the core. To this end Hongwei et al. [17] propose applying a ferrite epoxy to bondwire inductors with Wang et all. proposing ceramic tape for 2.5D semi-integrated passives. Although neither author was able to match the energy density of Chengs work, a more fundamental issue omits bondwire inductor converters as a candidate technology for pin optimisation.

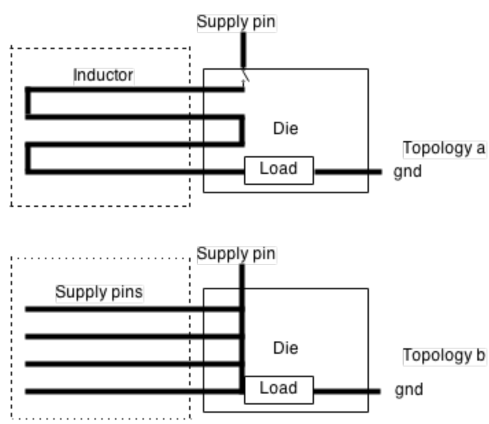

Figure 7: The power limitation of bondwire inductors

Topology b, with no switching converter in Figure 7 is able to deliver more power per pin than topology a, which features bondwire inductors.

With the above mentioned limitations, research integrating high permiability materials into custom layout inductors is considered. Recent advances in device physics have yeilded thin film inductors [30] with orders of magnitude energy density improvement over those in prior art [28]. Sturcken et al. [39] propose a converter with such devices able to drive 6.3A and Intel report 400A [42] using the same inductor technology. This is the highest reported drive of all integrated converters to the authors knowledge. Thin film inductors appear to be subject to a caveat. Due to their geometric structure and unique ferroelectric core they are not integrated into bulk CMOS in the literature, instead being built on a separate interposer.

Inductor research is summarised as being a focussed effort to improve Q_l The state of the art is represented by thin film inductors, which enable much higher energy density converters than capacitors alone.

Component literature as a whole is distilled as follows; power switches offer many options for design trade-off. The upper limits of voltage and energy density are reached with CMOS alternative transistors. Passive components were limited in energy density with standard CMOS. Recent advances in device physics have succeeded in miniturising energy dense inductors and capacitors, but these require additional doping material and process steps to create on bulk Si. As with power switches, the upper limit of energy density is not demonstrated in bulk CMOS

4.4 SC Architecture

Integrated SC architecture research focusses on addressing the poor load regulation and line noise of the basic circuit topology described earlier.
Improving load regulation: Basic SC converters have no load regulation. Load regulation is desirable as it improves the exponential decay in efficiency outside of the basic topology operating point(s). This is because increasing Z_O for light loads means less power is burned in the converter, since for a fixed operating voltage, the end to end DC impedance is higher and therefore end to end DC current is lower.

As seen in Viraj et al. [43] Integrating SC converters to digital processors allows for complex capacitor and switch topologies, since bulk capacitance can be sub-divided.
Le et al. [26] propose a novel converter circuit topology with more granular impedance modulation control than that of Viraj. By splitting C into 4 parallel SC converter modules, Z_O is adjusted by modulating the phase difference between the F_s of these modules. The converter also features the re-configurable step-down voltage circuit for coarse grain voltage control. Peak efficiency is far higher than [43] at 82%, and the efficiency curve has linear regions as opposed to the purely exponential worsening of [43].
Although other work ([32] etc.) implement capacitance modulation, Le et al. is notable for additionally implementing conductance modulation.
Conductance modulation of the power switches allows finer control of converter impedance, since the MOSFETs are analogue devices. However since the operating principle is equivilant to an LDO, it is unattractive in terms of efficiency. **Improving line noise:** Basic SC converters have high voltage ripple because of exponential discharge of the power capacitors to the load. Improving the voltage line stability is important as processors have low line noise tolerances.
Line noise is addressed in the literature by sub-dividing the load driving capacitance as was seen in load regulation improvement techniques. However the capacitance visible at the load is not modulated. Instead, the converter modules operate out of phase, superposing their exponential voltage discharges to smooth V_{Out}. Success of this technique motivated aggressive exploration of capacitance phase slicing in the literature. Pique [**?**] reports a load driving capacitance sliced into 41 phase shifted parallel converters and find line noise to improve around 16× compared with 10 phase prior art.

4.5 Inductor buck architecture

The basic buck topology offers far better impedance modulation relative to SC designs with the well established technique of pulse width modulation (PWM). Earlier discussion focussed on Continuous current mode (CCM), where conductance is increased varying the D ducty cycle. Increased conductance improves buck efficiency for heavy loads since the converters impedance can be made lower than the load, with less wasted power burnt in the converter.
However for light loads efficiency is improved with increased Impedance. Impedance is increased by shortening the inductor charge pulse. In DCM PWM, inductor current is ”discontinuous” because the charge pulse is so short the inductor fully discharges into the filter capacitor F_c and load. In DCM mode, DC V_{Out} is no longer simplified to $D \times V_{in}$ because C supplies both current and voltage after the inductor is discharged. Resolving V_{Out} is therefore non trivial for buck control circuitry.

Integrated buck converters can feature complex digital control loops and the literature explores this space. The two challanges are precisely controlling the operating point in DCM and switching between DCM and CCM at optimum intervals for a load in flux.
Wens et al. [45] report a novel SCOOT control system for alternating between CCM and DCM. SCOOT differs from the bulk of literature on this topic by splitting the passive components into a grid of sub modules, a technique applied in integraged SC architectures. However unlike capacitance, inductance reduces for electrically parallel modules, such that the 4 constituent

converters quiesce in DCM mode. The superposition principle allows Wens to simulate CCM in this quiescent mode by adding a phase shift of $\frac{\pi}{2}$ for each module relative to its two adjacent neighbours. DCM can be forced by reducing the duty cycle D. The benefit of this approach is reduced ripple voltage at V_{Out} compared with monolithic passives. SCOOT varies module phase along with D in attempts to optimize the operating point to load, however the latency of the passives and control circuitry appears to oscillate efficiency around the load operating point.
The imprecise operating point of DCM is also addressed with control techniques on monolithic passive designs.
DCM control operates on a hysteresis principle since D does not govern V_{Out}. Non-integrated buck converters can adjust T_{On} of the power train switch(es) after sensing V_{Out} in a timely fashion since these converters feature large passive devices. Switching speeds typically occur in the KHz regimen. The small passive size of integrated converters requires switching speeds of hundreds of MHz **Cite a bunch**. With control circuit blocks operating in the nS range, simple hysteresis control of integrated bucks has received attention in the literature.
Feng et al. [41] propose a delay compensation hysteresis controller for integrated DC DC converters, however their approach requires overcharging the load for faster operation of the control comparator circuitry. This is unattractive from an efficiency perspective, since the goal is to increase converter impedance in DCM. Cheng et al. [15]address this by using a short discharge pulse of the load. They calibrate the control loop timing for different light load conditions using difference in the sensed V_{Out} before and after discharge to determine an optimum T_{On} to restore V_{Out}. As Cheng's method increases output impedance, it is more attractive in DCM mode than Feng's. The 84.7% efficiency is the highest reported for a chip integrated converter, however the architecture cannot be applied to moderate and heavy loading conditions.

Researchers have applied circuit design to improving performance characteristics besides efficiencies. An additional flying capacitor added to the basic circuit can reduce the total capacitance by 50% according to Cheng [14].Flying capacitor buck converters vary in topology depending if the target passive for reduction is capacitive [14] or inductive [19], but all create a more complicated filter and energy storage network. The Additional complex poles in the circuit frequency domain enable researchers to operate at a target load range with smaller passives.

To summarize converter architecture research, integrated buck and SC topologies improve performance with common techniques such as passive slicing and control phase shift techniques applied to modular converter designs. Both types of converter are able to improve control of impedance, Z_O however the SC design is still fundamentally limited to higher impedance than the buck.
In addition, circuit techniques in the literature are shown to reduce the passive sizes beyond those required for a basic topology.

5 The IO limit with integrated DC DC converters

For a given SOC design if power were supplied with independently from the PCB substrate, the IO bandwidth limit of a package is defined by signal integrity limits. The theoretical limit proposed by Shannon [37] defines an SNR that must be met for information transfer. For some given noise, chips toggle their pins with an SNR headroom beyond Shannon's limit for practical IO. As frequencies increase it becomes more difficult to maintain this headroom. The reason is characterised by

- Reducing signal drive relative to noise
- Increasing signal attenuation relative to noise

For signal attenuation consider the transmission line diagram, Figure8
We see that the parasitics create a low pass filter on the

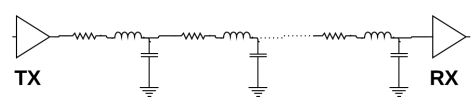

Figure 8: Transmission line model with parasitic Z

transmission line. A high transmission frequency offers high bandwidth but also suffers higher attenuation. Because noise has constant power for all frequencies the result is lower SNR. Since the parasitics increase with line length, transmission lines may be shortened to reduce filtering and improve SNR. The parasitics are also affected by transmission line quality so filtering is also reduced with routing techniques and improved materials.

For reducing signal drive consider the IO buffer diagrams, Figure**??**
The supply voltage of buffers must be maintained for the maximum swing and hence SNR of IO. Driving. Consider the difference in topology for integrated and external DC DC Converters
DIAGRAMSHOWINGLARGEPARASITCINDUCTANCE FOR EXTERNAL MAYBE SHOW ON CHIP DECAP FOR BUFFER TOO! The high switching speed and bursty nature of high speed IO, such as processor

to processor interfaces creates a performance corner requirement for DC DC converters. For reliable chip operation, the converter must be able to respond to transient I×R drop at the IO buffers V_{CC}. Because of the long power transmission lines from off chip converters an IO buffer, large parasitic inductance Increases the converters response time to transient I×R drop. This attenuates IO signals and reduces SNR.

A review of Intel processors from the past three decades evidences the two SNR characteristics in IO. Increasing SNR at high frequency **NEED TO MASSAGE THESE NUMBERS!**

Integrated DC DC converter can improve SNR to and the IO limit

IO drive strength is compromised because of localized transient voltage droops at IO driver transistor supply terminals. This reduces the SNR since the IO buffers have a weaker drive capability. Not only can integrated converters respond faster to voltage droop than external converters, they can do so on localised regions of a power grid. Designs such as **Cite** split the power components into modules distributed geographically in a chip, with similarly distributed V_{Out} terminals.

Signal attenuation: An integrated DC DC converter addresses the problem of transient IO loading. The inductance path from power supply to IO buffer V_{CC} is reduced. This makes reliable chip operation easier to achieve, since the on chip converter can respond to transient I×R drop faster. The granularity of transient I×R drop is also improved since the on chip converter can be split into multiple power supply modules driving regions of the power distribution network. The literature exemplifies several such topologies **CITE**.

The literature demonstrates integrated power converters capable of replacing external VRMs with a low volume considering input voltage above those common to Li-Ion batteries. Although the set of component capabilities and converter characteristics identified earlier show promise for application to this problem, the high voltage integrated converters identified do not make aggressive use of them. Therefore the performance of integrated converters in high voltage is an open research question

5.1 Saving pins with DC DC converters

Practical high power, high voltage integrated converters are the enabler for pin optimisation as they define the lower bound of pins required for a given power envelope. Previously reviewed literature finds active and passive components capable of driving a spectrum of processor power loads. reviewed literature has also reported integrated converters capable replacing external VRMs. However up to this point the report has focussed on systems operating at input voltages of $4.5V$ and lower. With high voltage switches reviewed, state of the art in high voltage integrated converters are reviewed in this section.

As high power density passives are nacent, there is a dearth of literature on high voltage integrated converters owing to their impracticality as LDO replacements. Two representitive designs are reviewed below that attempt to circumvent the limitations of commonly available low power integrated passives.

High voltage SC-buck: Pilawa et al. [31] Implement a twin stage stepdown converter that is a hybrid SC and buck design. high voltage input is stepped down by an SC phase as pre-regulation. The output of the pre-regulator is input to a secondary buck phase, which cleans the noisy SC voltage with its filter and provides an analogue range of low voltages.

Pilawa et al. implement a semi-integrated design. They achieve relatively high power density of 0.8W with off die passive components. High input voltage is handled with LDMOS (triple well) switches, which increases the operating voltage at the cost of switching speed. Since the buck stage operates within nominal bulk supply voltage, its power switches operate much faster. This improves the realisable Z_O regulation speed.

The LDMOS switches are a technology option of the CMOS process chosen in the work. They limit the design input voltage to 5V and are a significant source of loss.

With more closely integrated passives and improved switches, the ideas of this work could mature into a practical candidate for high voltage integrated power converters.

High voltage substrate transformer-buck: High voltage DC DC converters (5v+) miniture power converters exist as substrate integrated devices. With semi-integrated converters emerging as viable replacements for off chip VRM's, we consider the limit of semi-integration. Much of the reviewed literature integrates passive components to die substrate **Cite a bunch, inc pilawa**. Gong et al. [11] is an example of substrate integration for high voltage, high energy density power converters. The design embeds a miniture transformer coil and inductor coil in a 6 layer PCB substrate. The control IC, power switches and capacitor are mounted on this substrate. This design operates in the high voltage high power, high efficiency corner. Metrics are respectively 48V, 300W and 96% peak.

This level of substrate integration and power output has several drawbacks. The primary issue for pin count optimisation is substrate area consumed by planar power components blocks vias and constrains pin routing.

Designs such as that of Gong offer a potential means for high voltage efficient converters but have a high component cost and area penalty in the substrate. This limits their appeal despite their demonstrated utility.

To conclude on the state of the art, a lack of exploration in high voltage integrated converters was identified. Practical semi-integrated approaches were found but have limited power capabilities or limited appeal for pin optimisation.

5.2 Directions for future work

We define a research goal of high voltage, efficient and energy dense integrated power converters.
Several enabling works were identified in the literature to explore this space. Therefore the goal is refined as investigating the lower bound power to IO pin ratio of realisable converters.
Several reviewed converter implementations can be eliminated given the refined goal:

- **Standard CMOS SC/Buck converters:** Standard CMOS converters do not operate efficiently enough to reduce the power to IO pin ratio
- **Mini-transformer:** Planar substrate transformer and inductors block both IO and power pins
- **Bondwire inductors:** Consuming substrate pin pads for power inductors can never reduce the power to IO pin ratio

Some augmentation to the reviewed literature is now postulated.
LDMOS High voltage SC-Buck Pilawa's work [**?**] Is a potential application for relatively slow switching high voltage LDMOS.
LDMOS transistors cannot operate fast enough to provide the tightly controlled converter required for high bandwidth IO, neither is an SC converter suited to an efficient transient load regulation. However the pre-regulated capacitors are excellent charge wells for decoupling. This allows a faster switching buck regulator to provide a clean voltage with fast transient response, since there is negligable inductance between the charge well and filter. This is the main advantage of such a design.
Realizing the pontential benefits require several research questions be addressed.
Power Density: Pilawa's semi-integrated solution to the power density issue of integrated capacitors may be questioned and alternate avenues explored. Although power density of Pilawa's work is relatively high it is below that of Cheng [15], Strucken [40], [39] and other semi-integrated converters. As such Pilawa's power density is unattractive. The semi-integrated approach of passives may also be further explored as Pliawa's design mounts the power capacitors to the die substrate, introducing a far larger parasitic impendence than Strucken and Intel's *Si* interposer mounted inductors. The trade-off in energy density and charge cycle periods of deep trench [**?**] and ferroelectric capacitors [9] employed by could be weighed against those of substrate and interposer mounted power capacitors.
Efficiency: The design has a double power train and therefore double parasitic losses. The design is also complex for component value optimization since the SC and buck create a complex filter.
Interposer buck: Silicon interposer bucks represent the state of the art in performance [42], [39]. In additon the interposer enables IO optimisation to be explored via the directions of 3D and 2.5D integration.
The limit of IO density: A tangental exploration of processor IO density leveraging interposers is presented by Gokul et al. [21]. Interposers are used to reduce memory IO pins on the die substrate by sandwiching a Si interposer between memory and digital logic. The interposer mounted inductors used by Strucken and Intel could be integrated into such an interposer, with the buck converter used to optimise the IO and memory bandwidth to digital logic.
Power Density: In the 2.5D space, the energy dense non standard passives and high voltage power switches reviewed earlier could be used to explore an optimum pin ratio whilst retaining a standard CMOS digital die. The performance of GaN switches and Ferroelectric deep-trench capacitors alongside thin film inductors is as yet unknown.

5.3 Conclusions

Integrated DC DC converters show promise as a means to optimise IO pins in CPU and SOC chips. Integrated converters may improve power efficiency and power integrity for digital circuits and IO buffers as well as reducing the required number of core logic supply pins. The state of the art demonstrates some of this utility, but research is required to explore the full potential of integrated converters.
The limits of converter circuits and their components along with related research were reviewed.
Novel solutions and techniques show potential in addressing the efficiency and energy density issues of integrated circuits. However the question of optimally integrating the reviewed work remains open owing to the dearth of collaboration between specialists in each problem area.

With a goal of IO pin optimisation, conjecture is offered on advancing understanding of the area based on the SNR problems of high speed IO and the reviewed work. The low latency $I \times R$ droop response and high

quality output regulation required may be possible by furthering the twin stage converter work of Pilawa [?] as this architecture features a coarse grain low latency charge well in the SC phase in support of a low drive strength high quality output line in the buck phase.
Other reviewed literature offers insight required to address this works caveats and augment it for differing power and bandwidth requirements.

Pilawa's work is only one of several possible directions for integrated converter research targeting the IO problem. At it's heart, miniturizing DC DC converters is governed by advances in device physics and a discovery in this field could rapidly change the focus of architecture researchers in the future.

References

[1] AHN, YOUNGKOOK, H. N., AND ROH, J. A 50-mhz fully integrated low-swing buck converter using packaging inductors. *Power Electronics, IEEE Transactions on 27.10* (2012), 4347–4356.

[2] ALGHAMDI, M. K., AND HAMOUI., A. A. A spurious-free switching buck converter achieving enhanced light-load efficiency by using a-modulator controller with a scalable sampling frequency. *Solid-State Circuits, IEEE Journal of 47.4* (2012), 841–851.

[3] ALIMADADI, MEHDI, S. S. G. L. P. P. S. M., AND DUNFORD., W. A 660mhz zvs dc-dc converter using gate-driver charge-recycling in 0.18m cmos with an integrated output filter. *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* (2008), 140–146.

[4] ANDREOU, A. G., AND SNCHEZ-SINENCIO., E. Low-voltage/low-power integrated circuits and systems. *IEE* (1999).

[5] ARTILLAN, PHILIPPE, M. B. D. B. J.-P. L. N. M. L. B. M. D. B. E. C. A., AND SANCHEZ, J. L. Integrated lc filter on silicon for dcdc converter applications. *Power Electronics, IEEE Transactions on 26.8* (2011), 2319–2325.

[6] BATHILY, MALAL, B. A., AND HASBANI, F. A 200-mhz integrated buck converter with resonant gate drivers for an rf power amplifier. *Power Electronics, IEEE Transactions on 27.2* (2012), 610–613.

[7] DEL ALAMO, J. A., AND JOH, J. Gan hemt reliability. *Microelectronics reliability 49.9* (2009), 1200–1206.

[8] DENNARD, ROBERT H., F. H. G. V. L. R. E. B., AND LEBLANC., A. R. Design of ion-implanted mosfet's with very small physical dimensions. *Solid-State Circuits, IEEE Journal of 9.5* (1974), 256–268.

[9] EL-DAMAK, DINA, S. B., AND CHANDRAKASAN., A. P. A 93using on-chip ferroelectric capacitors. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), 374–375.

[10] FAQIR, MUSTAPHA, G. V. A. C. F. F. F. D. G. M. E. Z., AND DUA, C. Mechanisms of rf current collapse in algangan high electron mobility transistors. *Device and Materials Reliability, IEEE Transactions on 8.2* (2008), 240–247.

[11] GONG, ZHANKUN, Q. C. X. Y. B. Y. W. F., AND WANG, Z. Design of high power density dc-dc converter based on embedded passive substrate. *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* (2008), 273–277.

[12] GOYAL, N. Design and modeling of high-power semiconductor devices with emphasis on algan/gan hemts.

[13] HOWER, P. L., AND PENDHARKAR, S. Short and long-term safe operating area considerations in ldmos transistors. *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International* (2005), 545–550.

[14] HUANG, C., AND MOK, P. K. A 100 mhz 82.4fully-integrated buck converter with flying capacitor for area reduction. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International. IEEE* (2013), 1–12.

[15] HUANG, C., AND MOK., P. K. An 84.7buck converter with precise dcm operation and enhanced light-load efficiency. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), 1–13.

[16] IWAI, H. Roadmap for 22nm and beyond. *Microelectronic Engineering 86.7* (2009), 1520–1528.

[17] JIA, HONGWEI, J. L. X. W. K. P., AND SHEN, Z. J. Integration of a monolithic buck converter power ic and bondwire inductors with ferrite epoxy glob cores. *Power Electronics, IEEE Transactions on 26.6* (2011), 1627–1630.

[18] JOHARI, H., AND AYAZI, F. High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage. *Components and Packaging Technologies, IEEE Transactions on 32.4* (2009), 808–815.

[19] KIM, WONYOUNG, D. M. B., AND WEI, G.-Y. A fully-integrated 3-level dc/dc converter for nanosecond-scale dvs with fast shunt regulation. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011, IEEE International* (2011), 268–270.

[20] KRAUE, D. High power algan, gan hfets for industrial, scientific and medical applications. *Diss. Universittsbibliothek Freiburg* (2013).

[21] KUMAR, GOKUL, T. B. V. S. V. S. S. K. L., AND TUMMALA, R. Ultra-high i/o density glass/silicon interposers for high bandwidth smart mobile applications. *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st. IEEE* (2011), 217–223.

[22] KURSON, V., F. E. *Multi-voltage CMOS circuit design.* John Wiley and Sons, Chichester, 2006.

[23] KURSUN, VOLKAN, S. G. N. V. K. D., AND FRIEDMAN., E. G. Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 11.3* (2003), 514–522.

[24] KWONG, JOYCE, Y. K. R. N. V., AND CHANDRAKASAN, A. P. A 65 nm sub-microcontroller with integrated sram and switched capacitor dc-dc converter. *Solid-State Circuits, IEEE Journal of 44.1* (2009), 115–126.

[25] L CHANG, D FRANK, R. M. S. K. B. J. P. C. R. D., AND HAENSCH., W. Practical strategies for power-efficient computing technologies. *Proceedings of the IEEE 98.2.* (2010), 215–236.

[26] LE, H.-P. SEEMAN, M. . S. S. . S. V. . N. S. . A. E. A 32nm fully integrated reconfigurable switched-capacitor dc-dc converter delivering 0.55w/mm2 at 81 *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* (2010), 210–211.

[27] LEE, SANGKYU, U. P. V. A. H. Y.-G. J., AND YOON, K.-J. Microstructure and permittivity of sintered batio 3 : influence of particle surface chemistry in an aqueous medium. *Materials research bulletin 39.1* (2004), 93–102.

[28] MEERE, RONAN, T. O. H. J. B. N. W., AND O'MATHUNA, S. C. Analysis of microinductor performance in a 20-100 mhz dc/dc converter. *Power Electronics, IEEE Transactions on 24.9* (2009), 2212–2218.

[29] NAM, HYUNSEOK, Y. A., AND ROH, J. 5-v buck converter using 3.3-v standard cmos process with adaptive power transistor driver increasing efficiency and maximum load capacity. *Power Electronics, IEEE Transactions on 27.1* (2012), 463–471.

[30] O'SULLIVAN, EUGENE J., E. A. (invited) developments in integrated on-chip inductors with magnetic yokes. *ECS Transactions 50.10* (2013), 93–105.

[31] PILAWA-PODGURSKI, R. C., AND PERREAULT, D. J. Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos. *Solid-State Circuits, IEEE Journal of 47.7* (2012), 1557–1567.

[32] RAMADASS, YOGESH, A. F. B. H., AND CHANDRAKASAN, A. A 0.16mm2 completely on-chip switched-capacitor dc-dc converter using digital capacitance modulation for ldo replacement in 45nm cmos. *ISSCC 2010/SESSION 10/DC-DC POWER CONVERSION/10.7* (2010).

[33] RAMADASS, Y. K., AND CHANDRAKASAN, A. P. Voltage scalable switched capacitor dc-dc converter for ultra-low-power on-chip applications. *Power Electronics Specialists Conference* (2007).

[34] ROBERTSON, J. High dielectric constant oxides. *The European physical journal applied physics 28.03* (2004), 265–291.

[35] SEEMAN, M. D., AND SANDERS., S. R. Analysis and optimization of switched-capacitor dcdc converters. *Power Electronics, IEEE Transactions on 23.2* (2008), 841–851.

[36] SEEMAN, MICHAEL D., V. W. N. H.-P. L. M. J. E. A., AND SANDERS., S. R. A comparative analysis of switched-capacitor and inductor-based dc-dc conversion technologies. *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on* (2010), 1–7.

[37] SHANNON, C. E. A mathematical theory of communication. *ACM SIGMOBILE Mobile Computing and Communications Review 5.1* (2001), 3–51.

[38] STANLEY-MARBELL, PHILLIP, V. C. C., AND LUIJTEN., R. Pinned to the walls: impact of packaging and application properties on the memory and power walls. *Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design. 50* (2011), 51–56.

[39] STURCKEN, NOAH, E. J. O. N. W.-P. H. B. C. W. L. T. R. M. P. E. A. A 2.5 d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer. *Solid-State Circuits, IEEE Journal of 48.1* (2013), 244–254.

[40] STURCKEN, NOAH, E. O. N. W. P. H. B. W. L. R. M. P., AND SHEPARD, K. A 2.5 d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer delivering 10.8 a/mm 2. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International* (2012), 400–402.

[41] SU, FENG, W.-H. K., AND TSUI, C.-Y. Ultra fast fixed-frequency hysteretic buck converter with maximum charging current control and adaptive delay compensation for dvs applications. *Solid-State Circuits, IEEE Journal of 43.4* (2008), 815–822.

[42] TED-DIBENNE II, J, M. P. R. P. M. C. K. W. P. Z. T. F. L. X. M. S. W. S. E. F. R., AND PAUL., F. A 400 amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors. *APECSpecial Presentation* (2010).

[43] VIRAJ, A. K. P., AND AMARATUNGA., G. A. J. A monolithic cmos 5v/1v switched capacitor dc-dc step-down converter. *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE* (2007), 2510–2514.

[44] WENS, MIKE, K. C., AND STEYAERT, M. A fully-integrated 0.18m cmos dc-dc step-up converter, using a bondwire spiral inductor. *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European. IEEE* (2007), 268–271.

[45] WENS, M., AND STEYAERT, M. A fully integrated cmos 800-mw four-phase semiconstant on/off-time step-down converter. *Power Electronics, IEEE Transactions on 26.2* (2011), 326–333.

[46] ZHENG, CHEN, I. C., AND MA, D. Low-noise switched-capacitor power converter with adaptive on-chip surge suppression and preemptive timing control. *IEEE transactions on power electronics 28.11* (2013), 5174–5182.

Notes

[1]Remember to use endnotes, not footnotes!