

Saving pins and power with integrated voltage converters

Michael Barrow

mbarrow@eng.ucsd.edu

University of California, San Diego

Abstract

Recently, demand for increased processor performance coupled with reducing power budget has been addressed using emerging parallel processors. Parallel computation is an energy efficient (**cite chandrakasan**) way of increasing performance but requires wider interconnect busses. At the die boundary, the consequence is that systems face an IO bottleneck. The connection between silicon and substrate ends the scope of Moores law in a system, with IO density of packages increasing at a slower rate than on chip.

Compounding this problem, addressing performance by increasing parallel units result in increasing energy density due to the end of Dennard scaling (**cite**). Devices therefore require an increasing number of power pins, further limiting IO pin availability. **HOW ABOUT COMPELLING EXAMPLE?** We examine integrated power converters in this context. A review of the literature suggests with further research this technique could address the IO bottleneck of future processors.

1 Introduction

Against a backdrop of declining PC and growing smartphone sales, mobile devices drive demand for low power, high performance architectures. Emerging applications such as augmented reality, location aware services, high performance games and novel machine interfaces place an increasing demand for expanded IO capabilities and memory bandwidth from generation to generation of these devices. With the number of popular software stacks being lower than the number of major hardware vendors, device battery life is an important product differentiator. Research interest has therefore increased in power efficient architectures that can meet the IO and memory bandwidth requirements of the mobile segment.

package IO density is a well known problem to

architects. Marbell et al [26] review 130 hardware designs over 30 years and conclude the historical trend of package pin count and power pin count increase at an unsustainable rate. Promising solutions have been proposed, with Chang et al [18] identifying a subset of practical approaches in 2010. They conclude that voltage scaling as proposed by Dennard et al [7] is feasible, but enabled by a sum of techniques in different disciplines.

At the architectural level, power converter integration is advised in the worst case, where challenges of sub-threshold leakage prevent further reduction of CMOS voltage and power density prevents further integration of IO intensive system blocks such as memory. The observation in [18] is that reducing CMOS voltage has an exponential impact on loss through the power delivery pins. By maintaining pin voltage to devices and reducing operating voltage of CMOS using an efficient on die DC DC voltage converter bridge, an IC has a higher effective power density without increasing the number of power pins.

Research into integrated DC DC converters has been an active topic pre-empting [18] for other architectural benefits. As will be seen in detail in section **SECTION No**, DC DC converters typically feature bulky passive components. These increase the cost and footprint of mobile systems. Additionally, battery technology does not enjoy the improvement rate of CMOS, so operating voltage drops have opened a gulf between Battery supply voltage and IC input voltages. Techniques for extending battery life such as multiple voltage domains mean CPU's require multiple supply voltages. The symptoms of this are seen in the **Qualcomm snapdragon 800 which features 9 off chip DC DC converters CITE**. Against this backdrop, the feasibility of integrated DC DC converters shown by Kurson et al [16] invigorated research interest of integrated DC DC converters. A major motivation is removing the space and component costs of off chip converters **CITE A bunch of papers**

that feature this in abstracts.

State of the art in integrated DC DC converters is exemplified in Intel Haswell CPU's FIVR. Although a comparable DC DC converter exists in the literature [27], to the authors knowledge this is the only example of an integrated DC DC converter supplying a general purpose CPU in such a power envelope.

Intel's literature [28] suggests the FIVR is employed primarily to remove external DC DC converters and improve power efficiency. However a comparison of the pinout between Haswell **Cite** and the non FIVR predecessor **Ivybridge Cite** suggests that some power pins were saved too. This is unsurprising as Kurson notes in [16] that power pins could be saved by integrated DC DC converters. As we note DC DC converters improve the IO density problem, we review the literature to asses the feasibility of optimizing power pins to IO pins by increasing supply voltage of an integrated DC DC converter greatly beyond typical CPU operating voltage.

The rest of the document is ordered as follows:

- The operation of the DC DC converter and its critical design parameters
- Challenges associated with integrating DC DC Converters on die
- Performance limitations of monolithic CMOS DC DC converters
- Summary of recent research in integrated DC DC converters
- Methods of optimizing IC pin out with integrated DC DC converters
- Conclusions

2 Operation of the DC DC converter

Definition of the problem

Two popular stepdown converters in the literature are presented. A review of the literature highlights critical properties the topologies must feature in order to integrate either on chip.

2.1 Switched Capacitor stepdown converter operating principle

Two types of DC DC step down converter are popular in the literature. Type 1 is the switched capacitor (SC) converter. a simplified canoical $\frac{1}{2}$ series-parallel step-down topology is shown in Figure 1.

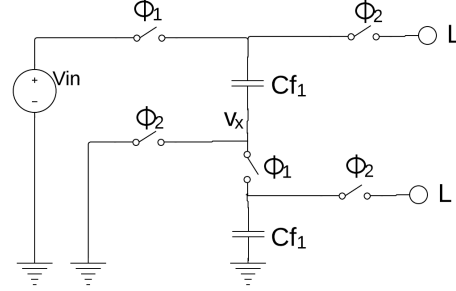


Figure 1: A $\frac{1}{2}$ stepdown SC topology

Let us consider the circuit with ideal components. Cf denotes some capacitance such that $Cf_1 = Cf_2$. switches are controlled by mutually exclusive clocks, ϕ_1 and ϕ_2 . These clocks are non-overlapping.

The circuit has two phases of operation. In phase 1, the charging phase, ϕ_1 switches are closed and ϕ_2 switches are open. Cf_1 and Cf_2 are in series. Since the capacitors are the same size, V_x is $\frac{1}{2}$ of V_{in} .

In phase 2, the discharging phase, ϕ_2 switches are closed and ϕ_1 switches are open. Now Cf_1 and Cf_2 are in parallel. Since they are matched in size, V_x remains at $\frac{1}{2}$ and is seen at terminal L across both capacitors.

2.2 Inductor-capacitor stepdown converter operating principle

The second popular converter is the inductor-capacitor stepdown (buck) converter. A simplified canoical topology is shown in Figure 2.

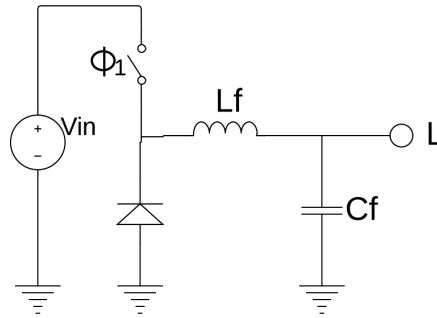


Figure 2: An inductor capacitor buck topology

The voltage conversion principle is understood by considering the inductor and capacitor as a high pass filter. ϕ_1 is a clock used to generate a square wave voltage of amplitude V_{in} . If this square wave is at a frequency

sufficiently higher than the 3db cutoff frequency of the filter, only the DC component of the square wave is observed at L . Because of this, buck converters may change their voltage stepdown ratio during operation, by modulating ϕ_1 . For a properly designed converter, V_L is defined by the duty cycle "D" [15] of ϕ_1 where: $V_{out} = V_{in} \times D$. In other words, if the square wave entering L_f is high for $\frac{2}{3}$ of its period, $V_{out} = \frac{2}{3} \times V_{in}$ and $D = \frac{2}{3}$.

2.3 SC stepdown converter critical parameters

The energy that a SC converter can transfer per charge cycle is $E_{Isc} = CV^2$. We could therefore express $W = E_{Isc} \times F_\phi$.

For a design with a given V_{in} and ideal components, the designer has two degrees of freedom to power a load, C and F_ϕ .

We re-draw Figure 1 with non-ideal components in Figure ??.

By observation of Figure ?? we see that F_ϕ and C are critical parameters that must be optimised for minimum losses

Losses associated with switches are switching loss during the non-overlapping period of ϕ , and conduction loss due to the equivalent series resistance (ESR) of switches. Conduction loss reduces the supply voltage seen at the capacitors by a factor δV_a . Conduction loss is therefore sensitive to the stepdown ratio. Increasing the stepdown ratio increases the number of series switches between all capacitors during the charging phase. For example a ratio of $\frac{1}{3}$ has 2 series switches, one of $\frac{1}{4}$ has 3 series switches and so on.

Losses associated with capacitors are parasitic capacitance losses. A parasitic capacitance known as bottom plate capacitance exists between one plate of each capacitor and ground. The voltage of these parasitic capacitor is a virtual ground and reduces the supply voltage seen at the capacitors by δV_b . Their charge can leak to true ground but cannot reach a load. As they are smaller than useful capacitance, they are significantly charged and discharged on each cycle of the converter. Loss is therefore expressed as $W = E_{Pc} \times F_\phi$ where $E_{Pc} = 1.5\alpha CV^2$. Literature reports bottom plate capacitance to be up to 5% of C_{tot} [22]. We also note that F_ϕ is adjustable at run-time and C is not and that $I_{out} \propto C$ [8] as well as F_ϕ .

In SC converters then, careful design considering voltage specification and technology parameters optimises converters to their load.

2.4 Inductor-capacitor converter critical parameters

How it works, critical parameters

2.5 Converter load regulation concept

Load regulation is matching output impedance "Z_O" of a power converter to a current load. Because $I = \frac{V}{Z_O}$ and maintaining V for a processor is critical, converter output impedance must track quickly with the load condition to keep V constant. The responsibility of tracking load and adjusting Z_O belongs to control circuits. Block Diagrams are shown in figure ??

Inductor-capacitor converters can reduce Z_O by increasing conductance. This is done by increasing "D" in eqnREF EQN. Because the asymptote is impedance of the filter at F_S , Z_O may also be increased by reducing F_S . [2].

SC converters power loads capacitively. Because the capacitors supply a DC load in parallel, Z_O cannot be lowered below $Z_C + Z_{Sw}$ at the nominal F_{Sw} . Modulating F_{Sw} can increase impedance in practice, because the capacitors can be purposely under-charged [24].

3 Design of Integrated DC DC Converters

Practical integrated converters are emerging and designed with different goals. A taxonomy of reviewed literature identifies two groupings:

1: Power system replacement converters. The goal is to remove external VRMs with an equally performing integrated subsystem

2: LDO replacement converters. The goal is an incremental improvement of the Low-dropout (LDO) regulators that have long been integrated on chip ??.

These differing goals result in different design tradeoffs. We focus on group 1 because of an efficiency reason. To explain, consider the operating principle of an LDO. A transistor gate is biased in its linear conduction region and a fixed voltage is dropped from source to drain to give desired V_{Out} . Recall power transfer efficiency, $\eta = \frac{R_{Load}}{R_{Load} + R_{Source}}$. For an LDO, (MAX)[η] = 0.5. Using a comparable integrated converter to optimize power pins is intractable because around half the power budget is wasted as heat, clearly a sub-optimal design. As such, literature aiming at group 1 best aligns with our interest in pin count optimisation.

3.1 Motivation

Switching converters such as the SC and buck can offer far higher efficient energy transfer than linear types. Theoretical efficiencies have been modeled at 96% [?] using state of the art devices. Integrated buck and SC implementations have been reported with 84% [12] and 93% [8] efficiency respectively. Provided these power converters can drive the desired load of a processor, they could be used to obtain an optimum IO to power pin ratio for a processor. This would be done by increasing the input voltage to on die converters to reduce the number of supply pins until a desired number is reached.

3.2 Design challenges

An Integrated DC DC converter is optimized through design tradeoffs that consider component non-idealities. Given that CPU designs have differing power envelopes and CMOS processes have unique electrical properties, researchers have explored the design space at multiple entry vectors.

SC converters The entry vector is an argument that A: Capacitance is easy to implement because MOSFET gate capacitance is a basic building block of CMOS. No corresponding basic block exists for inductance. B: Inductors have a necessarily large parasitic impedance because they are made from coiled resistive wire. Capacitors have a lower minimum impedance which shrinks as the plate size or capacitance grows.

However, as we have seen this type of converter has less flexible output impedance as compared with buck converters. Also SC converters do not have a voltage regulating filter which is built-in to bucks. This makes their output voltage vulnerable to switching noise. Therefore the design challenges emphasised in SC converters are: maximising effective capacitance, controlling output impedance and regulating output voltage.

buck converters The entry vector is an argument that C: Inductors can be implemented in standard CMOS. D: Inductor based buck has been a preferred design for (>100mW) applications over the past several decades [25], why change now?

3.3 Performance drawbacks of Baseline monolithic DC DC Converters

An example of a CMOS integrated SC converter [29] and CMOS integrated buck converter [3] are taken as examples. These designs highlight the performance drawbacks of baseline CMOS for integrated converters and explain the present concentration of research interest in this field. These setbacks from the initial entry vectors

of the SC and buck camps also explain the research and design approaches taken in more recent work. Although one process generation separates the designs, they are reasonably compared since the power components (capacitors, inductors and switches) consume almost all of the die in both designs.

SC drawbacks Naive Integrated SC converters have a low power density. [29] realize an on die capacitance of 1600pF with a converter power density of $1.7mW/mm^2$. In comparison the baseline buck [3] realize on die capacitance of 1.1nF with a power density of $20mW/mm^2$. The baseline SC converter also realizes much lower efficiency than expected in[29]. 80% is predicted in the literature, but only 62% is achieved due to unmoddled losses.

Only a single step-down voltage ratio is implemented, since the fixed SC circuit topology described earlier is used.

The performance of this design focussed researchers in areas to make SC integrated converters attractive in replacing off chip IC power converters. Broad categories and related research are listed below.

- **Energy density:** Device technology research to improve capacitor energy density
- **Efficiency:** Technology, circuit topology and converter control research to reduce power leakage
- **Flexibility:** Improve load regulation with SC power circuit topology and SC converter control research. In other words, provide flexible step-down ratio's.

buck drawbacks Although power density is higher than the baseline SC, it is still too low for contemporary processors. The combined area of the converter and load must feature a power density higher than that dissipated in the load **GET A GOOD REF OF POWER FOR MOBILE CPU'S**

Naive Integrated buck converters have a low efficiency. [3] achieve a peak efficiency of 46%. Not only is this lower than the baseline SC [29], its lower than an LDO (50%).

Unlike the SC design, the baseline buck can implement a range of stepdown voltages in a basic topology. However the baseline has poor load regulation. At its lowest output voltage it has a 25% efficiency in its most sophisticated operating mode. This drops to 13% in its baseline mode.

As with the SC design, the issues in this and other early monolithic converters led researchers to focus on areas for improvement to make integrated buck converters suitable to replace discrete IC's. Again we summarise broad categories and related research below.

- **Energy density:** Device technology research to improve inductor energy density
- **Efficiency:** Technology, buck circuit topology and buck converter control research to reduce power leakage
- **Flexibility:** Improve load regulation with buck converter control research. Buck converter voltage stepdown was better understood than SC, but poorly controlled

The broad categories of buck overlap those of the SC researchers. Therefore some research effort may transfer between the two designs and we also observe a merge between the separate research entry vectors identified earlier.

This manifests at the device level, where both converters share the same need to reduce losses. We can list these basic blocks and consider their problems when applied to integrated power converters abstractly from the two converter topologies.

CMOS Switches: Besides conduction losses, CMOS switches also suffer static and dynamic parasitic losses due to non-idealities. All must be balanced for an optimised power switch.

TRANSISTOR DIAGRAM SHOWING CRITICAL PARAMS

Static losses are constant no matter if the MOSFET switch is on or off. They occur because the MOSFET does not have an infinite open circuit resistance. Static loss is therefore technology node dependent and impossible to remove completely. Static losses are contributed to by components from sub-threshold leakage and gate oxide leakage currents.

These losses are intrinsic to all transistor based switches, however tradeoffs possible in modern technology nodes for full integration are less optimal than older technologies. Aggressive technology scaling continuously increases transistor leakage[1], so that realising the highest compute performance results in switches with the lowering efficiency in fully integrated designs.

Dynamic losses occur due to toggling the MOSFET switches. Power is consumed by changing the switch condition. As such, losses can be reduced by controlling switch toggling frequency, since for a given technology loss of the power switches and drivers increases by approximately $\sqrt{F_s}$ [4]. However given fixed size energy transfer components, reducing F_s reduces the converters power rating since $P = F_s \times E$.

Conduction loss occurs because the MOSFET switch does not have a zero on resistance. At a DC operating point, the conduction loss is simply the resistance of the MOSFET. Resistance of a MOSFET may be reduced

by decreasing its channel length, L_{ch} or increasing its channel width, W_{ch} . The minimum channel length is determined by process node e.g. 22_{nm} long in a 22_{nm} process, but channel width can be extended arbitrarily. However gate capacitance, $G_c \propto W_{ch} \times L_{ch}$. Reducing conduction loss therefore increases dynamic loss by increasing the power needed to charge G_c and toggle the switch.

As a final note, CMOS switches cannot operate reliably beyond the technology node voltage. This imposes limitations on the stepdown voltage ratio that can be achieved if a switch is connected between power rails. This does not impact loss but it does mean that the power a converter can supply is maximum when the stepdown ratio is 1 : 1 **TRUE KINDA BUT JUSTIFY WITH EQN**

By considering a fully optimised switch, we see the pressing research problems are reversing the leakage trend[1] and operating with rail voltages above the target technology rating.

Capacitors: Capacitors suffer from time or frequency related losses due to non-ideality. The loss problem is complicated by the frequency dependence of capacitor impedance/reactance. This is encapsulated with $Q_c = \frac{1}{\omega C R_c}$, or the capacitors "Q" quality factor. If $Q_c = 1$, the capacitor is ideal and does not impede a voltage signal. The "Q" factor has a different level of criticality in SC and buck designs. buck designs can offset a low capacitor " Q_c " value with their inductor if properly designed.

DIAGRAM SHOWING CRITICAL PARASITICS

Because converters normally operate at a high frequency, Loss in the capacitor is typically due to its equivalent series resistance, R_c and its parasitic capacitance. The major parasitic capacitance component is formed between the ground node and bottom plate of the capacitor[8]. as noted previously CMOS may have up to 5% parasitic capacitance. This is more critical for SC designs since they must transfer all of their energy via capacitors.

Considering the loss mechanisms in a capacitor, improvements to integrated converters are not easily made at the architectural or circuit level. Important research questions involve critical technology parameters. We also observe buck converters are less sensitive to low quality capacitors.

Inductors: Inductors, similar to capacitors suffer from frequency related non-ideality as well as static DC loss. As such, they have a quality factor $Q_l = \frac{\omega L}{R_l}$. A $Q_l = 1$ represents a perfect inductor. In a standard CMOS process, $R_l \gg R_c$. This is because $L \propto \phi_{ind}$ where ϕ_{ind} is magnetic flux. In standard CMOS, ϕ_{ind} is increased by increasing the inductor length and hence increasing R_l . Contemporary CMOS has metal layers optimised for

deep sub-micrometer components and design rules Conversely for a capacitor, increasing C requires increasing plate area and hence reducing R_c . For this reason SC designs cite low Q_l as their research motivation **CITE A BUNCH OF PAPERS THAT SAY THIS.**

Because the impedance of inductors is phase shifted from capacitors, buck converters can be optimized at the circuit level through component sizes. However, given their low Q_l due to high resistive loss, important research questions concern technology parameters critical to improving ϕ_l and reducing R_l .

3.4 Summary of recent literature

An evaluation of recent literature finds a volume of work addressing the previously outlined issues of integrated converters.

We review the literature beginning with work on the common building blocks of passive components and power transistors, then move on to review system level advances.

CMOS Switches: Alimadadi et al.[3] propose an energy recycling mechanism to use the charge at the power switch gates as useful energy by pumping it to the load. The power PMOS and power NMOS gates are driven by stacked supply buffers to toggle the power switches. vss of the power PMOS gate buffer is vdd of the power NMOS gate buffer via an electrical connection at node x . by connecting node x to the load via a forward-biased diode, energy used to charge power MOS gate capacitance can also charge the load node, rather than sink to ground. The drawback of this technique is that the $\frac{1}{2}$ VSS swing of the power MOS gate nodes limits the amount of stepdown possible. It would therefore not translate to a high voltage stepdown.

Bathily et al.[5] also focus on energy loss in switch toggling. They propose an LC tank that resonates at F_s such that the power MOSFET switch gate voltages oscillate at this resonant frequency. If the power switch gate voltage is low the switching energy is stored in the tank. If the power switch gate voltage is high, switching energy is stored at the switch nodes. The authors find improvements in switch efficiency ranging from around 12 – 25% accross the complete operating range. However the requirement is 16nH of inductance occupying 40% extra silicon area in a standard CMOS process. The technique is applicable in high voltage converters, but the 40% reduction of energy density makes it unattractive in medium to high power applications. Hyunseok et al.[21] address the higher than operating voltage step-down issue with circuit design and CMOS layout techniques. The circuit design handles higher than operating voltage by stacking power MOSFET devices in series

such that each device does not drop more than the CMOS operating voltage. The sum of series voltage exceeds the operating voltage however. This technique is made novel with the circuit design of the power MOSFET switching inputs, which are toggled by operating voltage, despite the switch stacking. Although an arbitrary voltage step-down could be achieved with power MOSFET stacking, this technique has diminishing returns for two reasons. Firstly, the conduction loss of the stacked power switches is summed, reducing efficiency. Secondly the switch toggling energy of the stacked power switches is summed since it is capacitive. This reduces the maximum F_s and therefore increases the required C or L for a fixed power envelope. As such this technique is less attractive as input voltage increases.

In the same high voltage vein, Bandyopadhyay et al[?] propose a buck converter with stacked power MOSFET switches. However, they use a single drain extended NMOS (DnMOS) for high voltage and stacked PMOS devices. DnMOS increases the reverse breakdown voltage of a MOSFET so that it will not short circuit at voltage above the technology operating vdd. An advantage of DEMOS is that no special process steps are needed. The main disadvantage of DEMOS in high voltage converters is high on-resistance and sensitivity to process variation. The limit of voltage step-down and current flow is around 30V at 2A [11] at which point non-standard CMOS process is required for reliable operation.

With the limit of DEMOS understood we consider the literature regarding switches suitable for high voltage and or high current.

For voltages above 20V at current above 1A, LDMOS switches outperform DEMOS. Hower et al[11] are paraphrased as follows: LDMOS devices have lower on-resistance than DEMOS but have a fixed device length, so transistors cannot be folded geometrically. LDMOS can be integrated into a low voltage technology node monolithically because they are compatible with bulk CMOS. The cost is an additional mask layer and therefore a non-standard process. A final drawback is LD-MOS has a higher V_t , so they require more switching energy.

Finally in the high F_s high power design corner we consider AlGaIn/GaN switches. Although much research effort has been made to improve power density and breakdown voltage, AlGaIn/GaN switches outperform LDMOS in high-power high frequency switching applications [10]. This is because these switches have unique semiconductor properties beneficial to high voltage power conversion, such as; high operating frequency, high current density and high breakdown voltage[6],[9]. Krausse[14] summarises recent literature on power transistors graphically:

To conclude discussion on power switches, the litera-

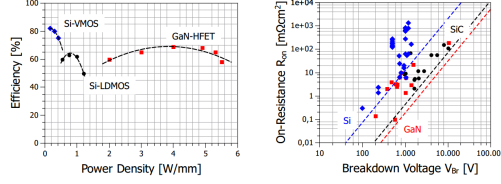


Figure 3: Comparative performance of power switch types, Reproduced from[14]

ture proposed novel circuit designs to improve switching efficiency. The limitations of these designs focus attention on the switch devices. The literature indicates as voltage and power density demands of a design increase, non-standard CMOS process and CMOS alternatives become increasingly attractive.

Capacitors: After Viraj et al.[29], much research effort was expended regarding converter capacitor energy density and impedance modulation. Kwong et al.[17] address both issues uniquely. The load is a sub-threshold processor, which allows low-energy density capacitors to provide adequate drive. Converter impedance is reduced with technology options and circuit topology. Metal insulator metal (MIM) capacitors are used as power passives. MIM capacitors have the desirable qualities of being compatible with bulk CMOS and having a high Q_c . Their disadvantage is low energy density. Viraj et al.[29] observed an exponential deterioration of efficiency with mismatched load impedance. This work implements a re-configurable step-down voltage circuit, where output capacitors can be stacked for 4 step-down voltages or 4 converter impedances.

Kwong et al. stands alone in the literature because it uses a sub-vt processor load to mitigate low energy density where most literature attempts to improve it.

Le et al. [19] propose a novel converter circuit topology with more granular impedance modulation control. By splitting C into 4 parallel SC converter modules, Z_O is adjusted by modulating the phase difference between the F_s of these modules. The converter also features the re-configurable step-down voltage circuit for coarse grain voltage control. Peak efficiency is far higher than [29] at 82%, and the efficiency curve has linear regions as opposed to the purely exponential worsening of [29].

Regarding energy density, non-standard CMOS capacitors dominate contemporary integrated converter literature.

Since energy density is improved by reducing loss, early work explored the limit of CMOS with circuit techniques. Besides their other innovations, Kwong et al.[17] feature a charge recycling circuit. The operating principle is similar to [3], but the energy source is parasitic capacitance and bondwire inductance. The technique was

Capacitor	Material	Permittivity (ϵ_r)
Bulk CMOS [23]	SiO ₂	3.9
High K CMOS [23]	HfSiO ₄	11
*Deep trench (structure) [13]	PZT	1000
*Ferroelectric [20]	BaTiO ₃	≈ 4600

not implemented in later designs by the authors or others.

Later work focuses on technology options for improving energy density. In CMOS compatible technologies, MIM [17] and Thin-gateMOS/fringe metal [?] capacitors are succeeded by the exotic Deep trench [?] and Ferroelectric [8] capacitors.

Exotic capacitor types either greatly increase C per unit area because they realise an extremely high permittivity (ϵ_r). Capacitance may be calculated $C = \epsilon_r \times \frac{A_p}{l_p}$ where A_p is the area of capacitive plates and l_p is the separation distance. * *example technologies, not used in reviewed designs* High capacitor permittivity can effectively negate bottom and top plate parasitic capacitance, since these capacitors could have an ϵ_r several orders of magnitude lower than the power capacitors.

Another class of converters has gained prominence due to the difficulties of energy density in capacitors. Semi-integrated converters **Cite a bunch** use off-die capacitors as a charge source. Provided such capacitors can be connected to the rest of a converter with a very low inductive path, these designs offer higher drive capability at the cost of an extra component.

In summary of capacitors, early circuit level approaches to energy density have been superseded by non-standard CMOS. Architectural level approaches in SC designs have been successful in improving impedance modulation.

To summarise power component literature, power switches offer many options for design trade-off. Passive components were limited in energy density with standard CMOS. Recent advances in device physics have succeeded in miniturising energy dense inductors and capacitors, but these require additional doping material and process steps to create on bulk Si.

- Control fixes paper list and description NOTE THAT THIS PROBLEM IS WELL UNDER CONTROL, CONCLUDE FROM THIS SECTION Le note that splitting C into parallel converter modules improves the terrible ripple of SC converters, 41phase of Pique takes this to the next level. all those phases greatly smooth ripple but this is an architecture/control technique
- Inductor fixes paper list and description. NOTE THAT THIS IS "SOLVED" BUT FOR SEMI-INTEGRATED OR WHATEVER note topology

fixes, flying capacitor is used We note that the approach is not necessarily to increase the size of inductance, but the quality factor. the baseline CMOS [3] realized 4.38nH inductors which is comprable with **HKGuys** at **5.xnH**, but the later work is able to realize a far greater energy density due to the novel technique of using bondwire as inductors.

4 Saving pins with DC DC converters

Solutions & Stakeholders, why is there still work to be done?

Need to define the problem of Signal to power pin ratio. We cannot optimize this today with DC DC converters, because the CMOS voltage stepdown means we need to have a lot of CORE power pins.

Our "stakeholder" is high voltage stepdown. If we do it we could reduce **DEFINE**"CORE POWER PINS" to an amount desirable for **DEFINE** signal integrity

Now we can outline the high voltage work that was summarized in the google doc I did

4.1 The IO limit with integrated DC DC converters

Defines stakeholder specific problem

Think about this, it has to be differentiated from the section above

4.2 Solutions

Here we have to talk about:

3 the micro transformer solution to this problem (it could be made promising)

2 the MIT solution to this problem (it does not look promising)

1 the disruptive technology of Si on Insulator, and how it could be paired with interposers

In the mobile segment Silicon interposers can be used to solve the IO problem as seen in [Ultra-high I/O Density Glass/Silicon Interposer for high Band-witdh Smart Mobile Application].

This interposer allows signal integrity to be maintained at low voltage from the interposer to memory. a High voltage from the substrate and DC DC converter integrated to the interposer allows power density to be met with fewer pins on the package. In this scenario, the package can be made smaller to allow denser integration, or the io bandwidth can be bound to signal integrity requirements...

SHOULD HAVE SOME SIMULATION TO CHECK INSIGHT ON 1, 2 and 3

4.3 Conclusions

Basically conclude that given the solutions simulation we could reach a situation where IO pressure is lifted from core power perspective, but that isn't so great tbh. **Remember Q = CV A high voltage power grid will require higher board capacitors and you need to be sure that inductance is sufficiently low on pcb as not to impede this current path**

References

- [1]
- [2] ALGHAMDI, M. K., AND HAMOUI, A. A. A spurious-free switching buck converter achieving enhanced light-load efficiency by using a-modulator controller with a scalable sampling frequency. *Solid-State Circuits, IEEE Journal of* 47.4 (2012), 841–851.
- [3] ALIMADADI, MEHDI, S. S. G. L. P. P.-S. M., AND DUNFORD, W. A 660mhz zvs dc-dc converter using gate-driver charge-recycling in 0.18m cmos with an integrated output filter. *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* (2008), 140–146.
- [4] ANDREOU, A. G., AND SNCHEZ-SINENCIO, E. Low-voltage/low-power integrated circuits and systems. *IEE* (1999).
- [5] BATHILY, MALAL, B. A., AND HASBANI, F. A 200-mhz integrated buck converter with resonant gate drivers for an rf power amplifier. *Power Electronics, IEEE Transactions on* 27.2 (2012), 610–613.
- [6] DEL ALAMO, J. A., AND JOH, J. Gan hemt reliability. *Microelectronics reliability* 49.9 (2009), 1200–1206.
- [7] DENNARD, ROBERT H., F. H. G. V. L. R. E. B., AND LEBLANC, A. R. Design of ion-implanted mosfet's with very small physical dimensions. *Solid-State Circuits, IEEE Journal of* 9.5 (1974), 256–268.
- [8] EL-DAMAK, DINA, S. B., AND CHANDRAKASAN, A. P. A 93using on-chip ferroelectric capacitors. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), 374–375.
- [9] FAQIR, MUSTAPHA, G. V. A. C. F. F. D. G. M. E. Z., AND DUA, C. Mechanisms of rf current collapse in algangan high electron mobility transistors. *Device and Materials Reliability, IEEE Transactions on* 8.2 (2008), 240–247.
- [10] GOYAL, N. Design and modeling of high-power semiconductor devices with emphasis on algan/gan hemts.
- [11] HOWER, P. L., AND PENDHARKAR, S. Short and long-term safe operating area considerations in ldmos transistors. *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International* (2005), 545–550.
- [12] HUANG, C., AND MOK, P. K. An 84.7buck converter with precise dcm operation and enhanced light-load efficiency. *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), 1–13.
- [13] JOHARI, H., AND AYAZI, F. High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage. *Components and Packaging Technologies, IEEE Transactions on* 32.4 (2009), 808–815.
- [14] KRAUE, D. High power algan, gan hfets for industrial, scientific and medical applications. *Diss. Universitätsbibliothek Freiburg*.
- [15] KURSON, V., F. E. *Multi-voltage CMOS circuit design*. John Wiley and Sons, Chichester, 2006.

- [16] KURSUN, VOLKAN, S. G. N. V. K. D., AND FRIEDMAN., E. G. Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 11.3* (2003), 514–522.
- [17] KWONG, JOYCE, Y. K. R. N. V., AND CHANDRAKASAN, A. P. A 65 nm sub-microcontroller with integrated sram and switched capacitor dc-dc converter. *Solid-State Circuits, IEEE Journal of 44.1* (2009), 115–126.
- [18] L CHANG, D FRANK, R. M. S. K. B. J. P. C. R. D., AND HAENSCH., W. Practical strategies for power-efficient computing technologies. *Proceedings of the IEEE 98.2*. (2010), 215–236.
- [19] LE, H.-P. SEEMAN, M. . S. S. . S. V. . N. S. . A. E. A 32nm fully integrated reconfigurable switched-capacitor dc-dc converter delivering 0.55w/mm² at 81 *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* (2010), 210–211.
- [20] LEE, SANGKYU, U. P. V. A. H. Y.-G. J., AND YOON, K.-J. Microstructure and permittivity of sintered batio 3 : influence of particle surface chemistry in an aqueous medium. *Materials research bulletin 39.1* (2004), 93–102.
- [21] NAM, HYUNSEOK, Y. A., AND ROH, J. 5-v buck converter using 3.3-v standard cmos process with adaptive power transistor driver increasing efficiency and maximum load capacity. *Power Electronics, IEEE Transactions on 27.1* (2012), 463–471.
- [22] RAMADASS, Y. K., AND CHANDRAKASAN, A. P. Voltage scalable switched capacitor dc-dc converter for ultra-low-power on-chip applications. *Power Electronics Specialists Conference* (2007).
- [23] ROBERTSON, J. High dielectric constant oxides. *The European physical journal applied physics 28.03* (2004), 265–291.
- [24] SEEMAN, M. D., AND SANDERS., S. R. Analysis and optimization of switched-capacitor dc-dc converters. *Power Electronics, IEEE Transactions on 23.2* (2008), 841–851.
- [25] SEEMAN, MICHAEL D., V. W. N. H.-P. L. M. J. E. A., AND SANDERS., S. R. A comparative analysis of switched-capacitor and inductor-based dc-dc conversion technologies. *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on* (2010), 1–7.
- [26] STANLEY-MARBELL, PHILLIP, V. C. C., AND LUIJTEN., R. Pinned to the walls: impact of packaging and application properties on the memory and power walls. *Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design. 50* (2011), 51–56.
- [27] STURCKEN, NOAH, E. O. N. W. P. H. B. W. L. R. M. P., AND SHEPARD, K. A 2.5 d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer delivering 10.8 a/mm². *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International* (2012), 400–402.
- [28] TED-DIBENNE II, J, M. P. R. P. M. C. K. W. P. Z. T. F. L. X. M. S. W. S. E. F. R., AND PAUL., F. A 400 amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors. *APECSpecial Presentation* (2010).
- [29] VIRAJ, A. K. P., AND AMARATUNGA., G. A. J. A monolithic cmos 5v/1v switched capacitor dc-dc step-down converter. *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE* (2007), 2510–2514.

Notes

¹Remember to use endnotes, not footnotes!