

Saving pins and power with integrated voltage converters

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Abstract

Recently, demand for increased processor performance coupled with reducing power budget has been addressed using emerging parallel processors. Parallel computation is an energy efficient (**cite chandrakasan**) way of increasing performance but requires wider interconnect busses. At the die boundary, the consequence is that systems face an IO bottleneck. The connection between silicon and substrate ends the scope of Moores law in a system with IO density of packages increasing at a slower rate.

We examine integrated power converters in this context. A review of the literature suggests this technique as a means to address both the IO bottleneck and power efficiency with further research.

1 Introduction

As Moores law continues, Technology scaling gives an increasing number of building blocks to meet conflicting consumer demands of increasing performance and energy efficiency. However the turn right approach exposes architects to complications of inconsistent technology scaling rates. In particular, for IO bound applications, the amount of achievable parallelism in silicon is proportional to the number of IO pins. The

More fascinating text. Features¹ galore, plethora of promises.

2 This is Another Section

Some embedded literal typset code might look like the following :

```
#include <iostream>
using namespace std;
```

```
main()
{
    cout << "Hello world \n";
    return 0;
}
```

Now we're going to cite somebody. Watch for the cite tag. Here it comes [?].

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Notes

¹Remember to use endnotes, not footnotes!