Saving pins and power with integrated voltage converters

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Abstract

Recently, demand for increased processor performance coupled with reducing power budget has been addressed using emerging parallel processors. Parallel computation is an energy efficient **(cite chandrakasan)** way of increasing performance but requires wider interconnect busses. At the die boundary, the consequence is that systems face an IO bottleneck. The connection between silicon and substrate ends the scope of Moores law in a system, with IO density of packages increasing at a slower rate than on chip.
Compounding this problem, addressing performance by increasing paralell units result in increasing energy density due to the end of Dennard scaling **(cite)**. Devices therefore require an increasing number of power pins, further limiting IO pin availability. **HOW ABOUT COMPELLING EXAMPLE?** We examine integrated power converters in this context. A review of the literature suggests with further research this technique could address the IO bottleneck of future processors.

1 Introduction

Against a backdrop of declining PC and growing smartphone sales, mobile devices drive demand for low power, high performance architectures. Emerging applications such as augmented reality, location aware services, high performance games and novel machine interfaces place an increasing demand for expanded IO capabilities and memory bandwidth from generation to generation of these devices. With the number of popular software stacks being lower than the number of major hardware vendors, device battery life is an important product differentiator. Research interest has therefore increased in power efficient architectures that can meet the IO and memory bandwidth requirements of the mobile segment.

package IO density is a well known problem to architects. Marbell et al [5] review 130 hardware designs over 30 years and conclude the historical trend of package pin count and power pin count increase at an unsustainable rate. Promising solutions have been proposed, with Chang et al [3] identifying a subset of practical approaches in 2010. They conclude that voltage scaling as proposed by Dennard et al [1] is feasible, but enabled by a sum of techniques in different disciplines.
At the architectural level, power converter integration is advised in the worst case, where challenges of subthreshold leakage prevent further reduction of CMOS voltage and power density prevents further integration of IO intensive system blocks such as memory. The observation in [3] is that reducing CMOS voltage has an exponential impact on loss through the power delivery pins. By maintaining pin voltage to devices and reducing operating voltage of CMOS using an efficient on die DC DC voltage converter bridge, an IC has a higher effective power density without increasing the number of power pins.

Research into integrated DC DC converters has been an active topic pre-empting [3] for other architectural benefits. As will be seen in detail in section **SECTION No**, DC DC converters typically feature bulky passive components. These increase the cost and footprint of mobile systems. Additionally, battery technology does not enjoy the improvement rate of CMOS, so operating voltage drops have opened a gulf between Battery supply voltage and IC input voltages. Techniques for extending battery life such as multiple voltage domains mean CPU's require multiple supply voltages. The symptoms of this are seen in the **Quallcomm snapdraggon 800 which features 9 off chip DC DC converters CITE**. Against this backdrop, the feasibility of integrated DC DC converters shown by Kurson et al [2] invigorated research interest of integrated DC DC converters. A major motivation is removing the space and component costs of off chip converters **CITE A bunch of papers**

that feature this in abstracts.

State of the art in integrated DC DC converters is exemplified in Intel Haswell CPU's FIVR. Although a comparable DC DC converter exists in the literature [6], to the authors knowledge this is the only example of an integrated DC DC converter supplying a general purpose CPU.

Intel's literature [7] suggests the FVIR is employed primarily to remove external DC DC converters and improve power efficiency. However a comparison of the pinout between Haswell **Cite** and the non FIVR predecessor **Ivybridge Cite** suggests that some power pins were saved too. This is unsurprising as Kurson notes in [2] that power pins could be saved by integrated DC DC converters. As we note DC DC converters improve the IO density problem, we review the literature to asses the feasibility of optimizing power pins to IO pins by increasing supply voltage of an integrated DC DC converter greatly beyond typical CPU operating voltage.

The rest of the document is ordered as follows:

- The operation of the DC DC converter and its critical design parameters
- Challenges associated with integrating DC DC Converters on die
- Performance limitations of monolithic CMOS DC DC converters
- Practicaly implementing integrated DC DC converters
- Methods of optimizing IC pin out with integrated DC DC converters
- Conclusions

2 The DC DC converter

Definition of the problem

Two popular stepdown converters in the literature are presented. A review of the literature highlights critical properties the topologies must feature in order to integrate either on chip.

2.1 Switched Capacitor stepdown converter operating principle

Two types of DC DC step down converter are popular in the literature. Type 1 is the switched capacitor (SC) converter. a simplified canoical $\frac{1}{2}$ series-parallel step-down topology is shown in Figure 1.

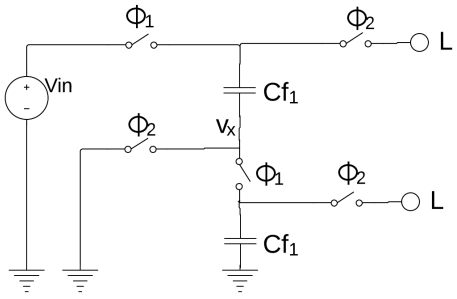

Figure 1: A $\frac{1}{2}$ stepdown SC topology

Let us consider the circuit with ideal components. Cf denotes some capacitance such that $Cf_1 = Cf_2$. switches are controlled by mutually exclusive clocks, ϕ_1 and ϕ_2. These clocks are non-overlapping.

The circuit has two phases of operation. In phase 1, the charging phase, ϕ_1 switches are closed and ϕ_2 switches are open. Cf_1 and Cf_2 are in series. Since the capacitors are the same size, V_x is $\frac{1}{2}$ of V_in.

In phase 2, the discharging phase, ϕ_2 switches are closed and ϕ_1 switches are open. Now Cf_1 and Cf_2 are in parallel. Since they are matched in size, V_x remains at $\frac{1}{2}$ and is seen at terminal L across both capacitors.

2.2 Inductor-capacitor stepdown converter operating principle

The second popular converter is the inductor-capacitor stepdown (buck) converter. A simplified canoical topology is shown in Figure 2.

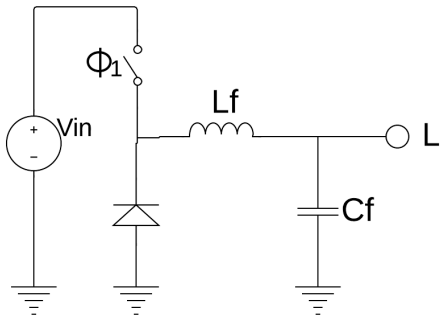

Figure 2: An inductor capacitor buck topology

The voltage conversion principle is understood by considering the inductor and capacitor as a high pass filter. ϕ_1 is a clock used to generate a square wave voltage of amplitude V_{in}. If this square wave is at a frequency

sufficiently higher than the 3db cutoff frequency of the filter, only the DC component of the square wave is observed at L. Because of this, buck converters may change their voltage stepdown ratio during operation, by modulating ϕ_1. For a properly designed converter, V_L is defined by the duty cycle "D" **??** of ϕ_1 where: $V_{out} = V_{in} \times D$. In other words, if the square wave entering L_f is high for $\frac{2}{3}$ of its period, $V_{out} = \frac{2}{3} \times V_{in}$ and $D = \frac{2}{3}$.

2.3 SC stepdown converter critical parameters

The energy that a SC converter can transfer per charge cycle is $E_{Isc} = CV^2$. We could therefore express $W = E_{Isc} \times F_\phi$.
V For a design with a given V_in and ideal components, the designer has two degrees of freedom to power a load, C and F_ϕ.
We re-draw Figure 1 with non-ideal components in Figure **??**.

By observation of Figure **??** we see that F_ϕ and C are critical parameters that must be optimised for minimum losses.
Losses associated with switches are switching loss during the non-overlapping period of ϕ, and conduction loss due to the equivilent series resistance (ESR) of switches. Conduction loss reduces the supply voltage seen at the capacitors by a factor δV_a. Conduction loss is therefore sensitive to the stepdown ratio. Increasing the stepdown ratio increases the number of series switches between all capacitors during the charging phase. For example a ratio of $\frac{1}{3}$ has 2 series switches, one of $\frac{1}{4}$ has 3 series switches and so on.
Losses associated with capacitors are parasitic capacitance losses. A parasitic capacitance known as bottom plate capacitance exists between one plate of each capacitor and ground. The voltage of these parasitic capacitor is a virtual ground and reduces the supply voltage seen at the capacitors by δV_b. Their charge can leak to true ground but cannot reach a load. As they are smaller than useful capacitance, they are significantly charged and discharged on each cycle of the converter. Loss is therefore expressed as $W = E_{Pc} \times F_\phi$ where $E_{Pc} = 1.5\alpha CV^2$. Literature reports bottom plate capacitance to be up to 5% of C_{tot} [4]
SC converters by topology have difficulty In SC converters then, careful design considering voltage specification and technology parameters

2.4 Inductor-capacitor converter critical parameters

How it works, critical parameters

2.5 Problems of an Integrated DC DC Converter

Definition of the system problem lives in
History of research
System type 1(Switched capacitor AND HISTORY)
Problems of bottom plate parasitic cap. Bottom plate parasitic capacitance limits the attractiveness of SC designs.
Problems of switching noise. These designs are noisier than Bucks, which have a filter by design

System type 2(Integrated buck AND HISTORY Kurson book)
Want to show how General CMOS components are made for this role and why they didn't work.

2.6 Performance drawbacks of Baseline DC DC Converters

Taxonomy of problem (deeper drill and more specifics of the problem)
what is wrong with the switches?
what is wrong with the control?
What is wrong with the capacitors?
. [**?**] evaluate the state of the art and plot an frontier of capacitor area to converter efficiency for Integrated converters. In general they find as capacitor area exponentially increases power density follows with only a linear cost in peak efficiency. However, efficiency exponentially decreases with power density in the non-ideal case.
What is wrong with the inductors?

2.7 Solutions

System: well defined, class of problems: well defined, now we will see "fixed" systems

- Switches fixes paper list and description DONT USE EXOTIC TECH! THESE WERE NEVER USED ON INTEGRATED DESIGNS!!!
- Control fixes paper list and description NOTE THAT THIS PROBLEM IS WELL UNDER CONTROL, CONCLUDE FROM THIS SECTION

- Capacitor fixes paper list and description NOTE THAT THIS PROBLEM CANNOT BE "SOLVED" FROM A SC TOPOLOGY POINT OF VIEW AND INDUCTORS ARE "BETTER" IN TERMS OF ENERGY DENSITY AND LINE REGULATION

- Inductor fixes paper list and description. NOTE THAT THIS IS "SOLVED" BUT FOR SEMI-INTEGRATED OR WHATEVER

3 Saving pins with DC DC converters

Solutions & Stakeholders, why is there still work to be done?
Need to define the problem of Signal to power pin ratio. We cannot optimize this today with DC DC converters, because the CMOS voltage stepdown means we need to have a lot of CORE power pins.
Our "stakeholder" is high voltage stepdown. If we do it we could reduce **DEFINE**"CORE POWER PINS" to an amount desirable for **DEFINE** signal integrity

3.1 The IO limit with integrated DC DC converters

Defines stakeholder specific problem
Think about this, it has to be differentiated from the section above

3.2 Solutions

Here we have to talk about:
3 the micro transformer solution to this problem (it could be made promising)
2 the MIT solution to this problem (it does not look promising)
1 the disruptive technology of Si on Insulator, and how it could be paired with interposers
In the mobile segment Silicon interposers can be used to solve the IO problem as seen in [Ultra-high I/O Density Glass/Silicon Interposer for high Band-witdh Smart Mobile Application].
This interposer allows signal integrity to be maintained at low voltage from the interposer to memory. a High voltage from the substrate and DC DC converter integrated to the interposer allows power density to be met with fewer pins on the package. In this scenario, the package can be made smaller to allow denser integration, or the io bandwidth can be bound to signal integrity requirements...

SHOULD HAVE SOME SIMULATION TO CHECK INSIGHT ON 1, 2 and 3

3.3 Conclusions

Basically conclude that given the solutions simulation we could reach a situation where IO pressure is lifted from core power perspective, but that isn't so great tbh.

References

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Notes

[1] Remember to use endnotes, not footnotes!