

2024 Fall IC Lab

Lab 12 Report

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Part I. APR Result

1. Core to IO boundary :

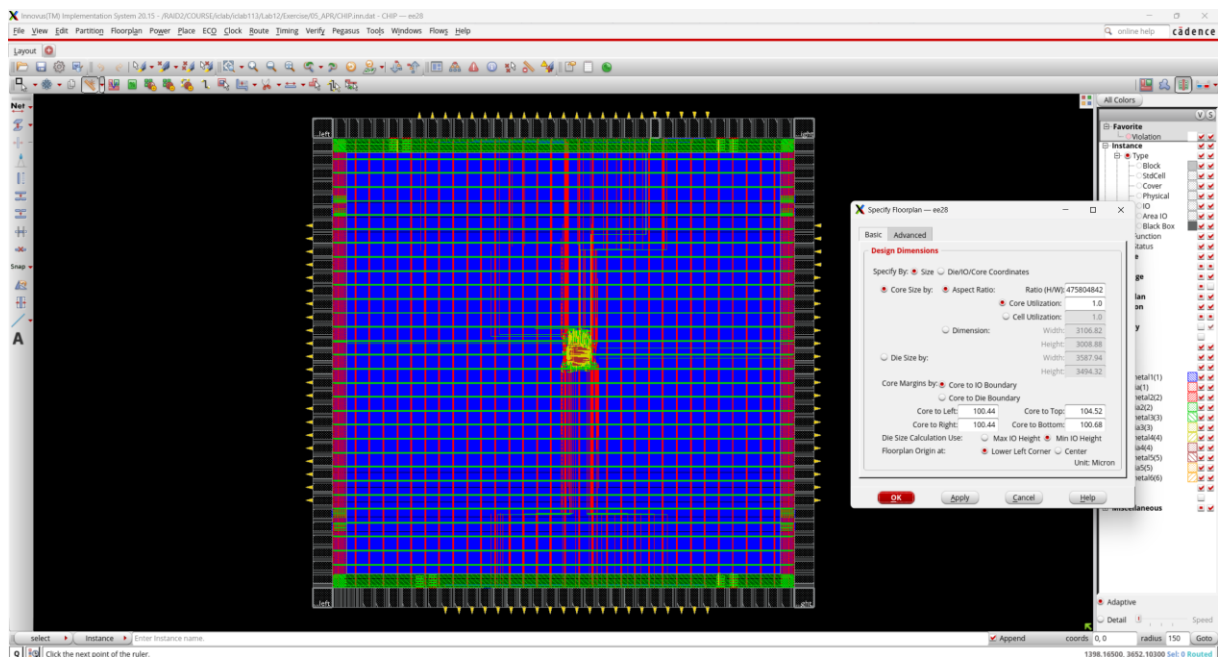
Core utilization: 1.0

Core to left: 100.44

Core to top: 104.52

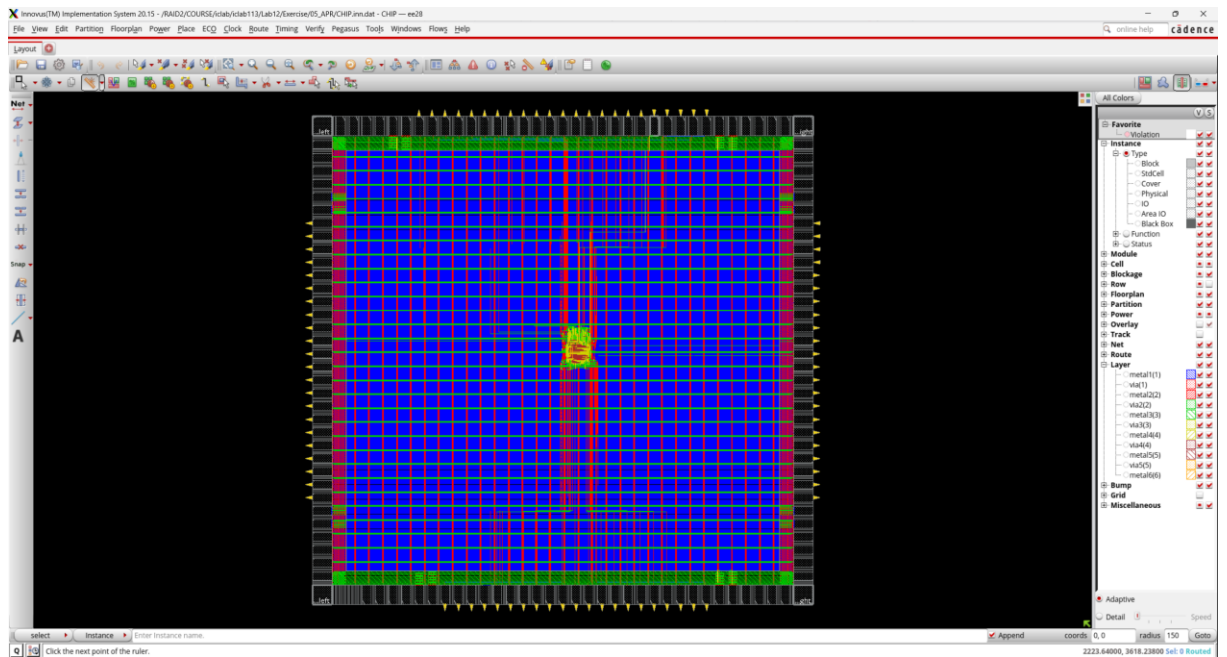
Core to right: 100.44

Core to bottom: 100.68



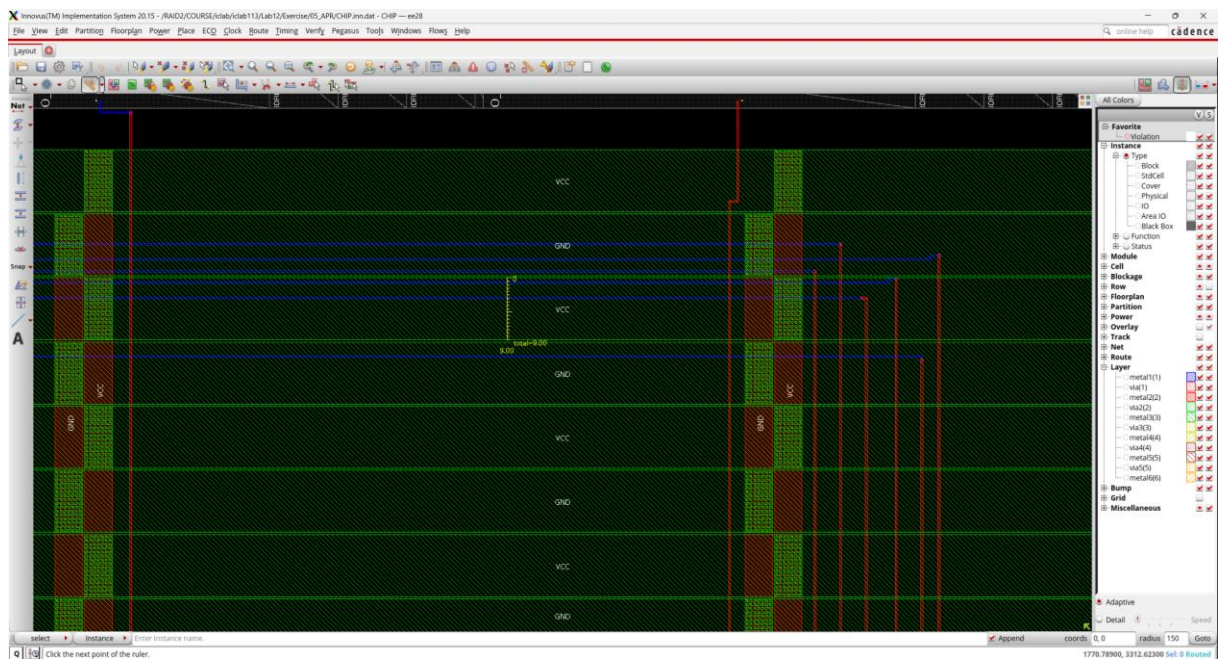
2. Core Ring :

Overview:

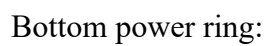


Top power ring:

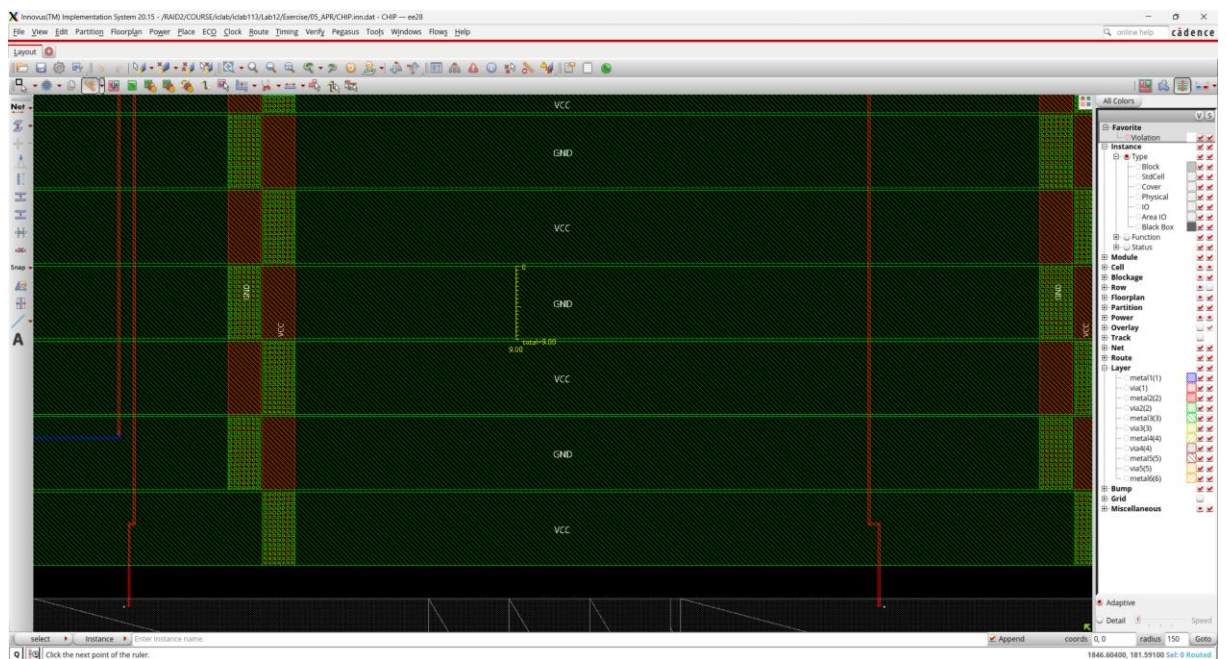
Total: 9



Total: 9

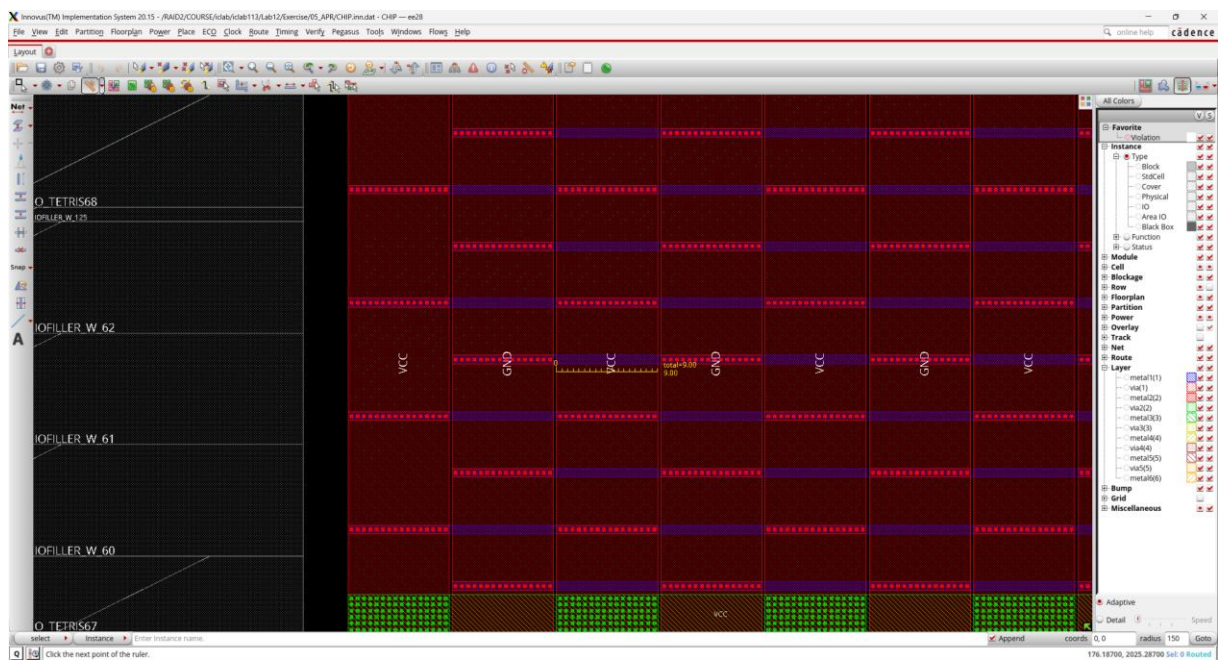


Total: 9



Left power ring:

Total: 9



3. Post-Route setup time analysis :

```
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 1382.
Total number of fetched objects 1382
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 1345, 0.3 percent of the nets selected for SI analysis
End delay calculation. (MEM=2466.1 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2466.1 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:01.8 real=0:00:02.0 totSessionCpu=0:01:13 mem=2466.1M)

-----
timeDesign Summary
-----

Setup views included:
av_func_mode_max

-----
| Setup mode | all | reg2reg | default |
|-----|-----|-----|-----|
| WNS (ns): | 13.853 | 31.285 | 13.853 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 595 | 247 | 366 |
|-----|-----|-----|-----|

-----
| DRVs | | Real | | Total |
|-----|-----|-----|-----|
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
|-----|-----|-----|-----|

Density: 0.412%
(126.704% with Fillers)
Total number of glitch violations: 0
-----
Reported timing to dir timingReports
Total CPU time: 7.37 sec
Total Real time: 9.0 sec
Total Memory Usage: 2455.035156 Mbytes
Reset AAE Options
*** timeDesign #1 [finish] : cpu/real = 0:00:07.3/0:00:09.8 (0.7), totSession cpu/real = 0:01:13.4/0:15:25.7 (0.1), mem = 2455.0M
innovus >

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```

4. Post-Route hold time analysis :

```
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 1382
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 1345, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2476.51 CPU=0:00:00.4 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=2476.51 CPU=0:00:00.5 REAL=0:00:01.0)
Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2476.5M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2476.5M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2439.63)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 1382.
Total number of fetched objects 1382
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 1345, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=2478.79 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2478.79 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.8 real=0:00:01.0 totSessionCpu=0:01:19 mem=2478.8M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min

-----
| Hold mode | all | reg2reg | default |
|-----|-----|-----|-----|
| WNS (ns): | 0.233 | 0.233 | 19.746 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 595 | 247 | 366 |
|-----|-----|-----|-----|

Density: 0.412%
(126.704% with Fillers)
-----
Reported timing to dir timingReports
Total CPU time: 1.25 sec
Total Real time: 2.0 sec
Total Memory Usage: 2412.058594 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:01.2/0:00:01.6 (0.8), totSession cpu/real = 0:01:18.9/0:16:43.3 (0.1), mem = 2412.1M
innovus >

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```

5. DRC result :

```
VERIFY DRC ..... Sub-Area: {2058.240 2956.800 2315.520 3225.600} 163 of 182
VERIFY DRC ..... Sub-Area: {163 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2315.520 2956.800 2572.800 3225.600} 164 of 182
VERIFY DRC ..... Sub-Area: {164 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2572.800 2956.800 2830.080 3225.600} 165 of 182
VERIFY DRC ..... Sub-Area: {165 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2830.080 2956.800 3087.360 3225.600} 166 of 182
VERIFY DRC ..... Sub-Area: {166 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3087.360 2956.800 3344.640 3225.600} 167 of 182
VERIFY DRC ..... Sub-Area: {167 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3344.640 2956.800 3587.940 3225.600} 168 of 182
VERIFY DRC ..... Sub-Area: {168 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 3225.600 257.280 3494.320} 169 of 182
VERIFY DRC ..... Sub-Area: {169 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {257.280 3225.600 514.560 3494.320} 170 of 182
VERIFY DRC ..... Sub-Area: {170 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {514.560 3225.600 771.840 3494.320} 171 of 182
VERIFY DRC ..... Sub-Area: {171 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {771.840 3225.600 1029.120 3494.320} 172 of 182
VERIFY DRC ..... Sub-Area: {172 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1029.120 3225.600 1286.400 3494.320} 173 of 182
VERIFY DRC ..... Sub-Area: {173 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1286.400 3225.600 1543.680 3494.320} 174 of 182
VERIFY DRC ..... Sub-Area: {174 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1543.680 3225.600 1800.960 3494.320} 175 of 182
VERIFY DRC ..... Sub-Area: {175 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1800.960 3225.600 2058.240 3494.320} 176 of 182
VERIFY DRC ..... Sub-Area: {176 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2058.240 3225.600 2315.520 3494.320} 177 of 182
VERIFY DRC ..... Sub-Area: {177 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2315.520 3225.600 2572.800 3494.320} 178 of 182
VERIFY DRC ..... Sub-Area: {178 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2572.800 3225.600 2830.080 3494.320} 179 of 182
VERIFY DRC ..... Sub-Area: {179 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2830.080 3225.600 3087.360 3494.320} 180 of 182
VERIFY DRC ..... Sub-Area: {180 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3087.360 3225.600 3344.640 3494.320} 181 of 182
VERIFY DRC ..... Sub-Area: {181 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3344.640 3225.600 3587.940 3494.320} 182 of 182
VERIFY DRC ..... Sub-Area: {182 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.8 ELAPSED TIME: 1.00 MEM: 19.0M) ***

innovus 1>
```

6. LVS result :

```
VERIFY DRC ..... Sub-Area: {1286.400 3225.600 1543.680 3494.320} 174 of 182
VERIFY DRC ..... Sub-Area: {174 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1543.680 3225.600 1800.960 3494.320} 175 of 182
VERIFY DRC ..... Sub-Area: {175 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1800.960 3225.600 2058.240 3494.320} 176 of 182
VERIFY DRC ..... Sub-Area: {176 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2058.240 3225.600 2315.520 3494.320} 177 of 182
VERIFY DRC ..... Sub-Area: {177 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2315.520 3225.600 2572.800 3494.320} 178 of 182
VERIFY DRC ..... Sub-Area: {178 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2572.800 3225.600 2830.080 3494.320} 179 of 182
VERIFY DRC ..... Sub-Area: {179 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2830.080 3225.600 3087.360 3494.320} 180 of 182
VERIFY DRC ..... Sub-Area: {180 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3087.360 3225.600 3344.640 3494.320} 181 of 182
VERIFY DRC ..... Sub-Area: {181 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3344.640 3225.600 3587.940 3494.320} 182 of 182
VERIFY DRC ..... Sub-Area: {182 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.8 ELAPSED TIME: 1.00 MEM: 19.0M) ***

innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 5 09:47:51 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3587.9400, 3494.3200)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu Dec 5 09:47:51 2024
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.2 MEM: 10.000M)

innovus 1>
```

7. Post Layout simulation result :

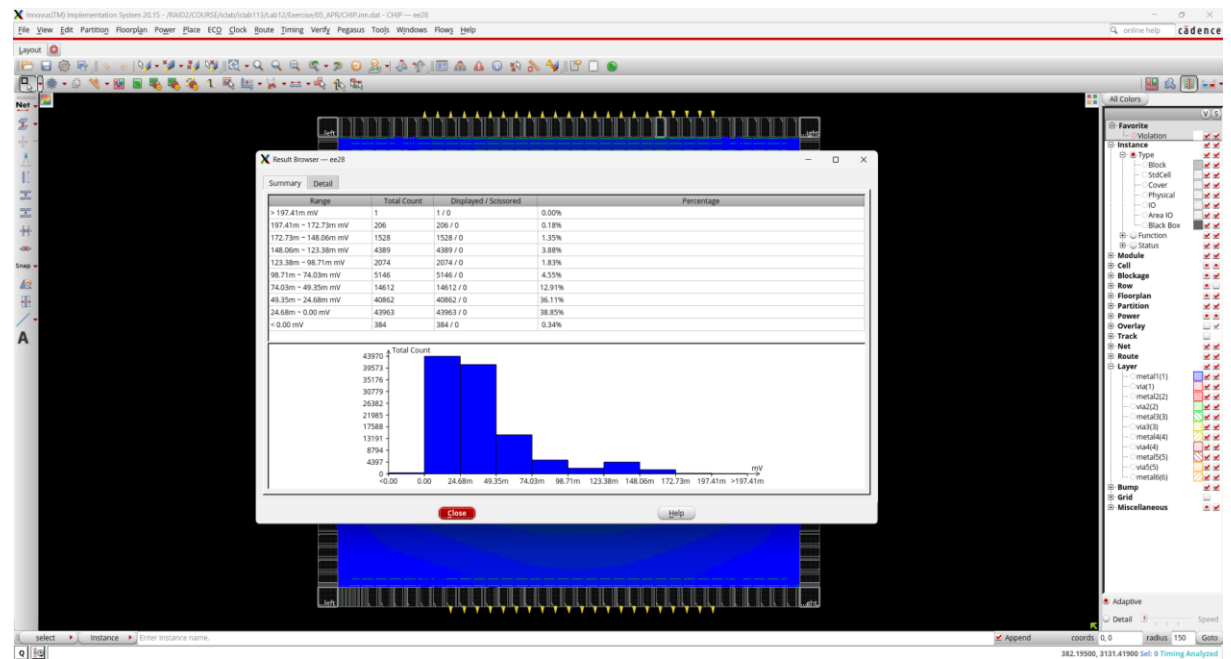
[illegible]

8. Power result :

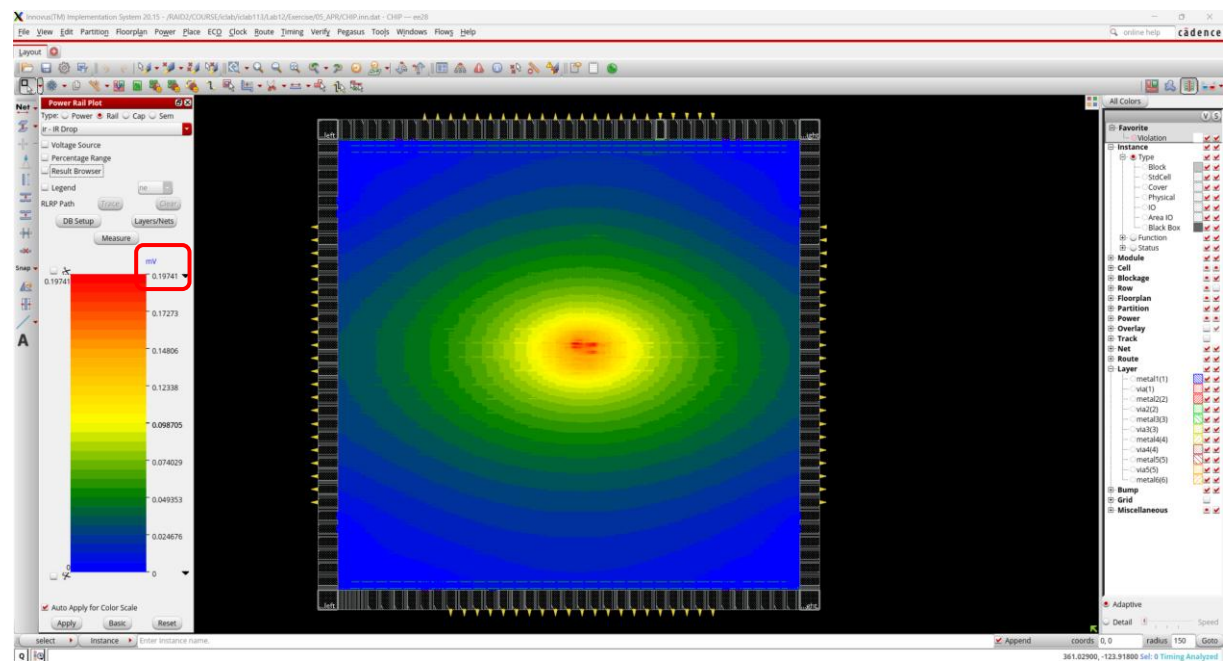
[illegible]

9. IR Drop Results :

Result browser:



Power rail plot:



Part II. IR Drop Reduction

1. Power grid design

藉由增加 power grid density，來確保 power distribution network 有足夠的 metal 層，減少電阻值，進一步降低 IR drop

2. Power stripes design

增加 power stripes 數量以及密度，在降低阻抗的同時減少 standard cell 供電路徑，以此降低 IR drop。