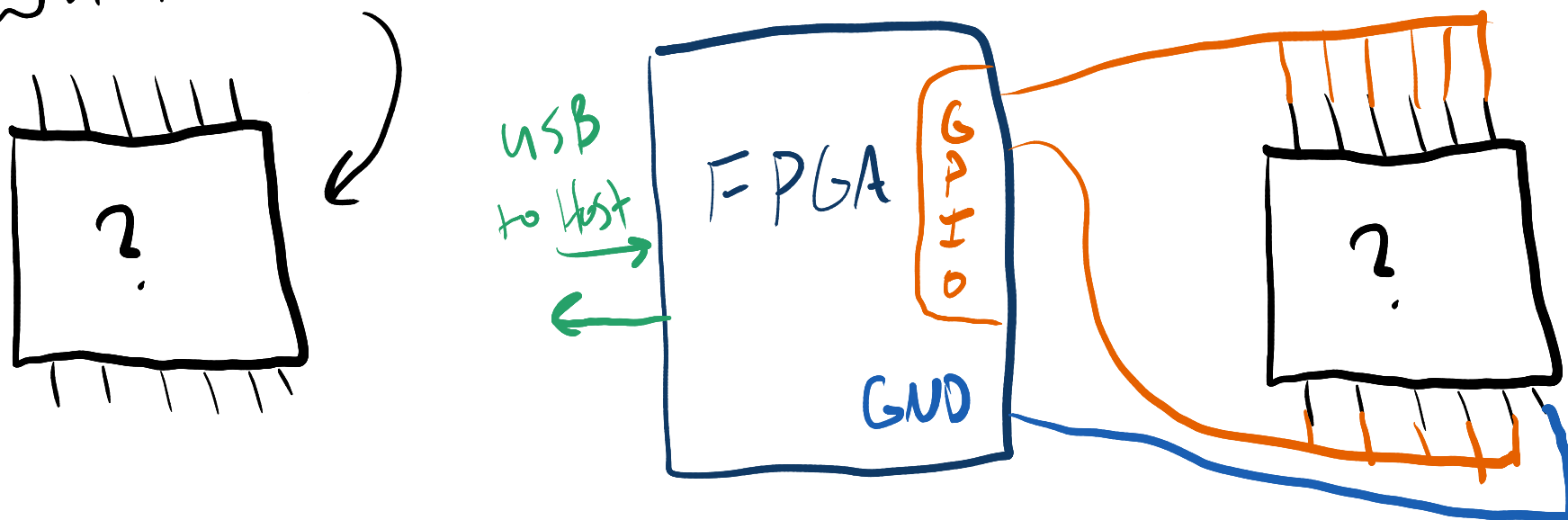
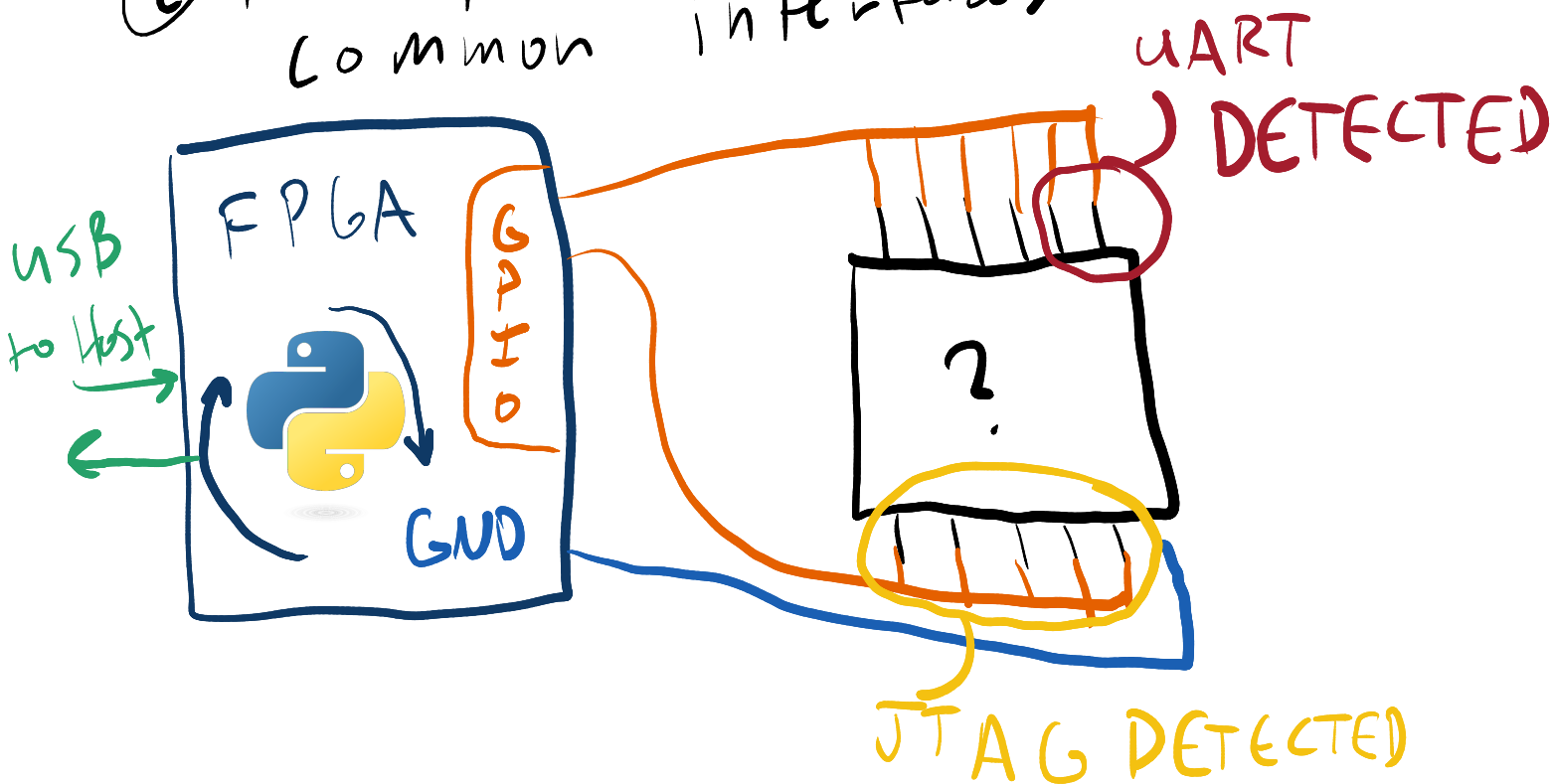


Unknown Device.  
What is it?

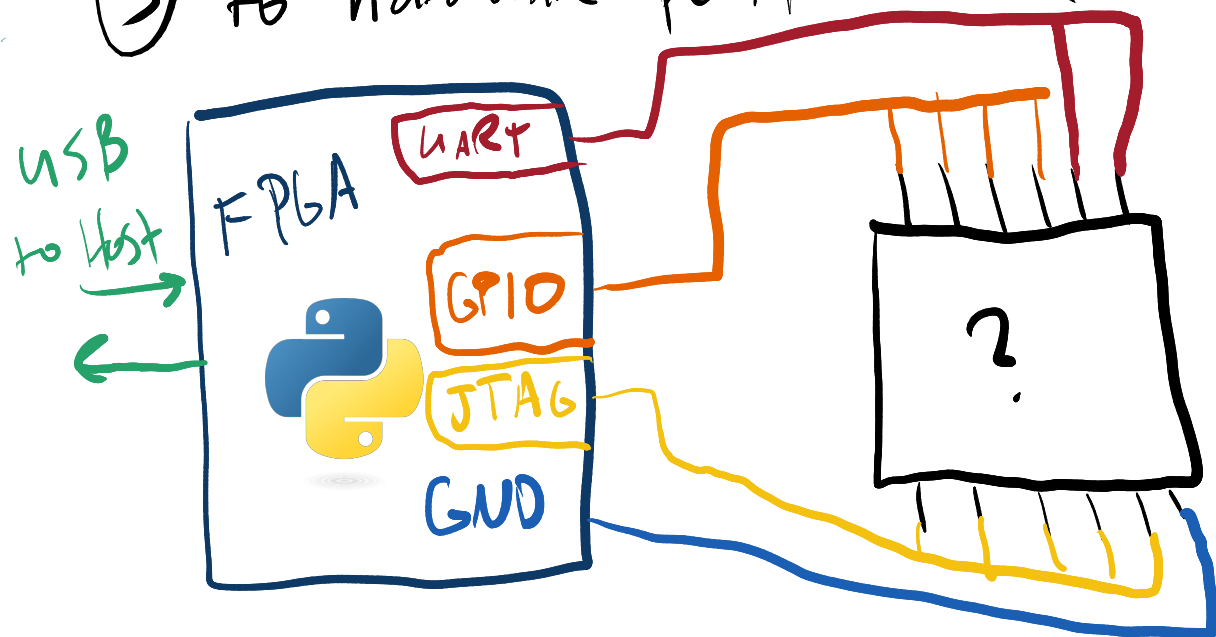
① Hook up to our device



② Probe pins through Python API to identify common interfaces



③ Reconfigure FPGA to connect detected interfaces to hardware peripherals (no bit-banging!)



④ Interact with DUT through USB like you had multiple physical adapters connected.

I/O 0 I/O 1 I/O 2 . . .

External I/O

OUT

TX

RX

PARTIAL RECONFIG

PERIPHERAL  
(eg. UART)

(Additional  
In/out pins  
depending on  
max needed  
by reconfig  
peripherals)

Data  
TX

Data Rx

to USB INTERFACE  
(Cypress FX3??)

Peripherals to implement:

UART

SPI

JTAG

SWD

What others: I2C

---

In  
RX

MISO

SPI

Out  
TX

MOSI

SDO, TMS, TCK, RST x2

Either?

SCK, CS

Questions:

Partial reconfig

+ how to do it?

+ how to determine correct area to allocate?

+ how many blocks are needed? / what interface signals

USB

+ How to present multiple peripherals to host?

+ How to prioritize I/O of specific peripherals

Hardware

+ what level shifting is required? Do we want ADCs?

+ High-speed PCB design? —

How is bidirectional I/O implemented on an FPGA  
is it better than dedicated I and O lines on reconfig block?

