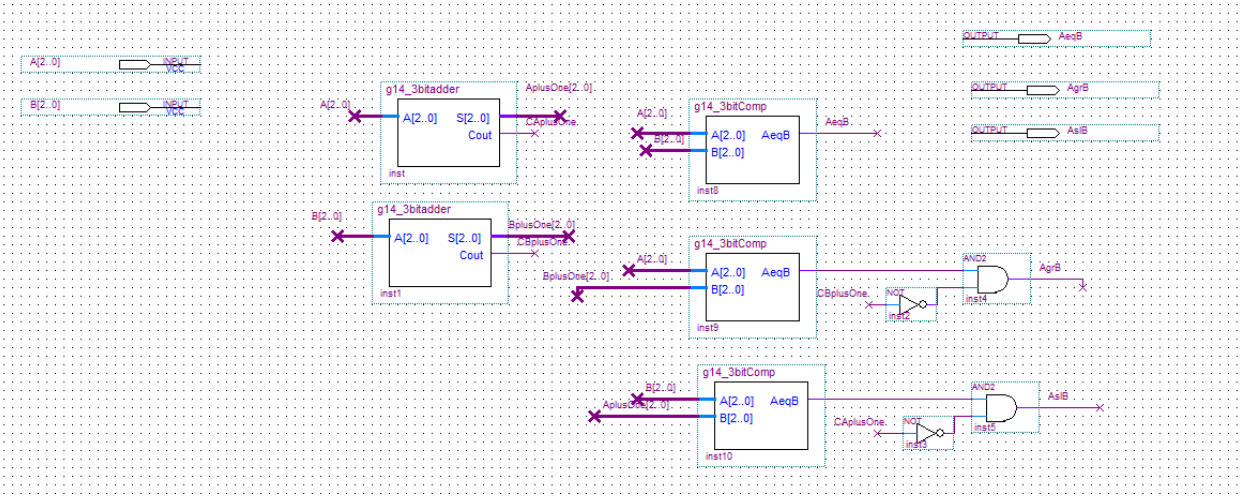
Group 14 -
Jerome Colomb 260349913
Matthew Johnston 260349319

Lab 1 Report

g14_comp3.bdf



Top-level I/O

Inputs

A[2..0] – 3 bit binary number

B[2..0] – 3 bit binary number

Outputs

AeqB – Boolean, high if A=B

AgrB – Boolean, high if A = B+1

AslB – Boolean, high if B = A+1

Description of Subcircuits

The top-level circuit contains two subcircuits. The first is a 3 bit adder, which itself is composed of 1 bit adders. The 3 bit adder adds one to a 3 bit number through the use of 1 bit adders. It returns the sum of the input plus one as well as the carry-ahead value. The second subcircuit of the top-level is a 3 bit comparator which takes in 2 3-bit binary numbers and returns high if they are equal. The comparators are used to check for the outputs' validity.

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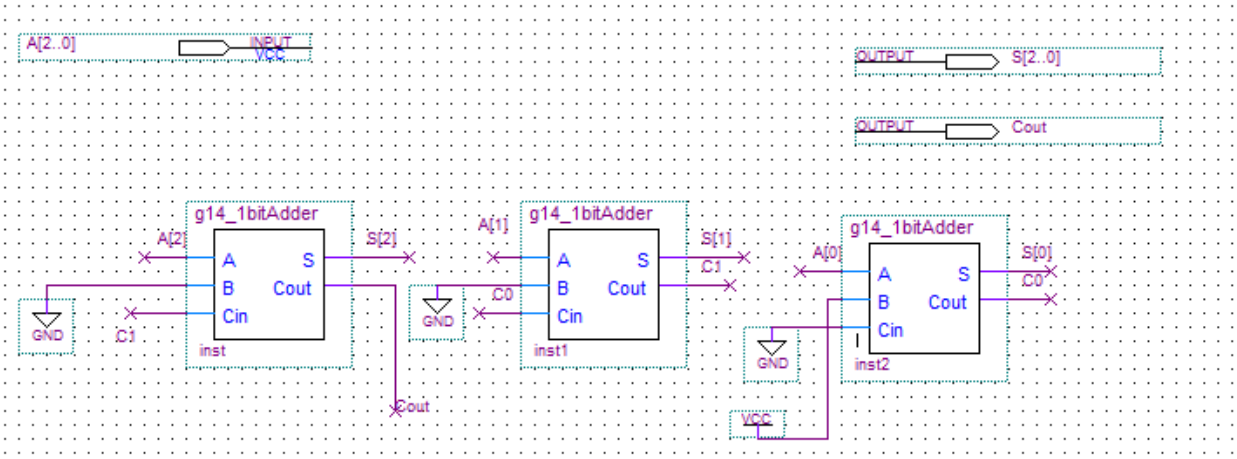
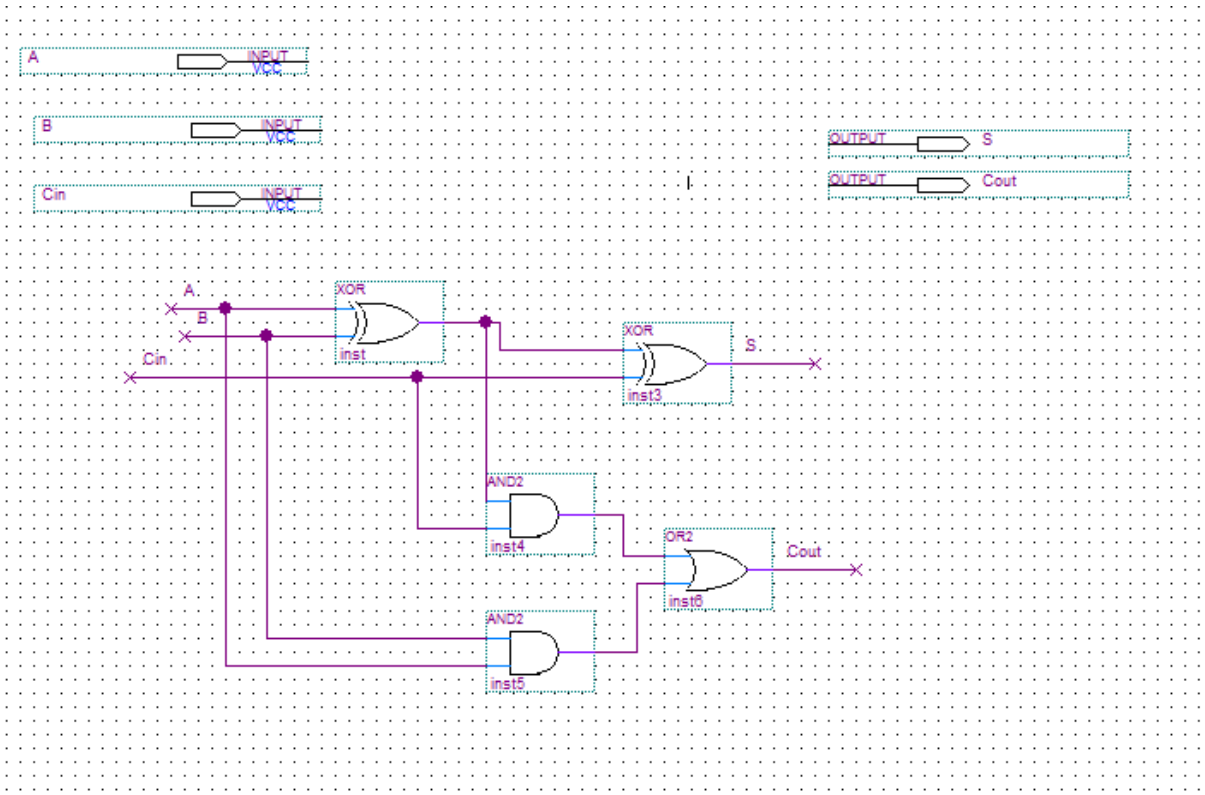
g14_3bitadder.bdf



g14_1bitadder.bdf



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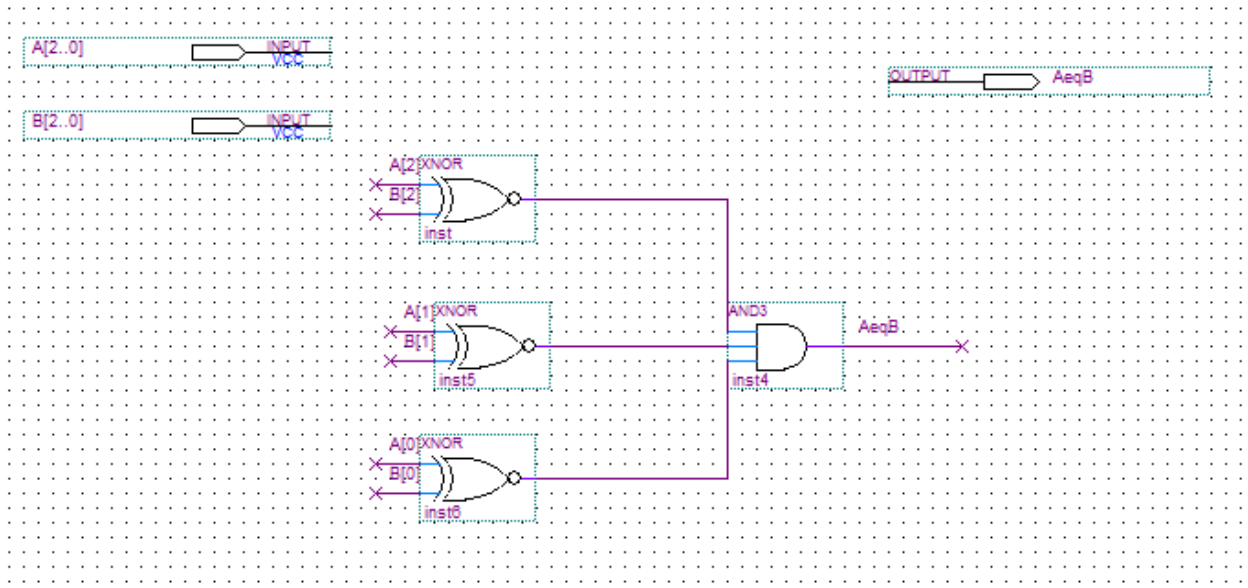
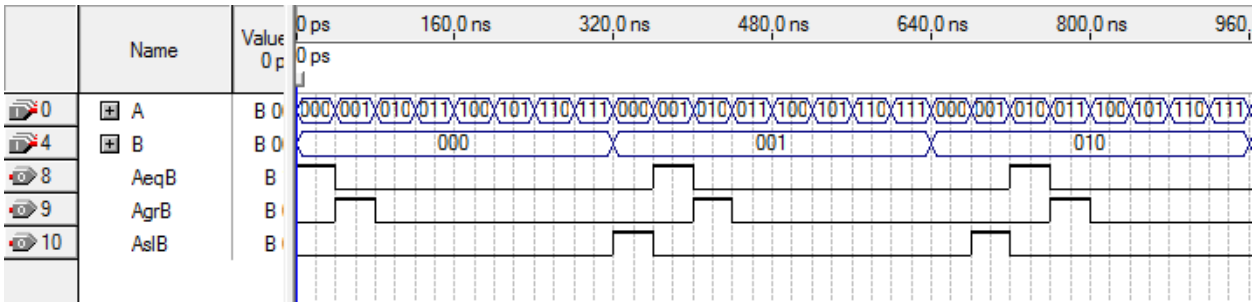
g14_3bitcomp.bdf



Testing

The circuit was tested by applying all the combinations of A and B to the inputs and observing the three outputs. B was held steady as A increased from 000 to 111, then B incremented by one as A cycled through its possibilities again. This process continued until all combinations were achieved. When B was 000, AslB never was never true and when B was 111, AgrB was never true. This proves that the wrap-around catching mechanism in the top-level circuit using the carry-ahead value was effective.



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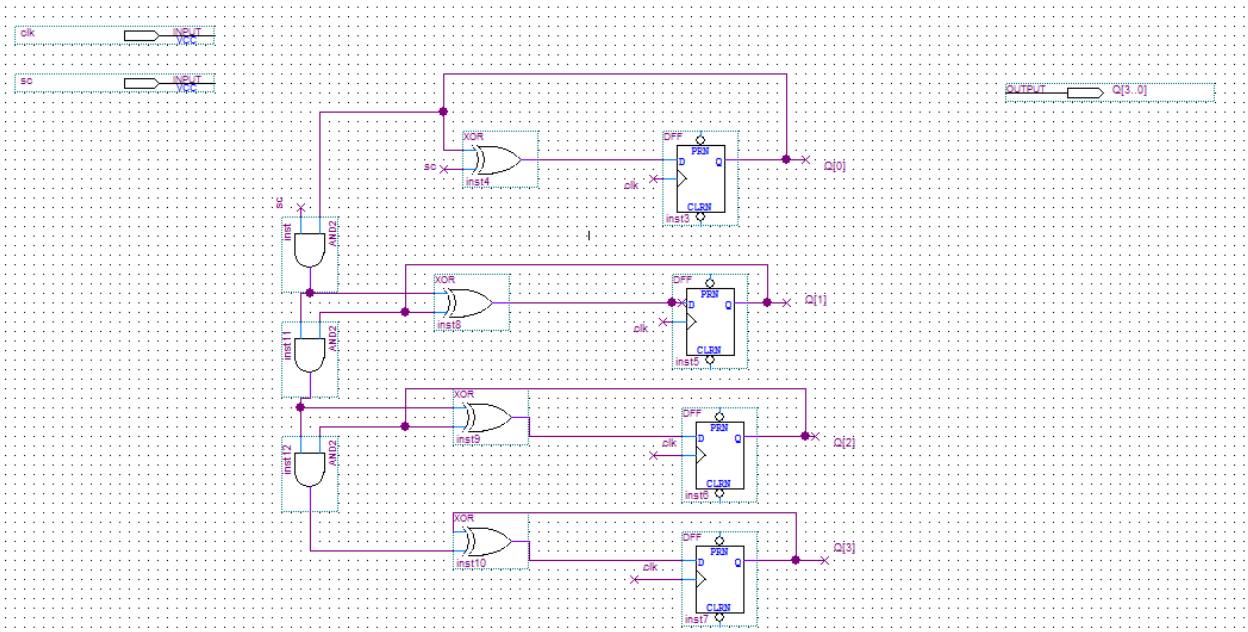
g14_count4.bdf

The 4-bit counter was implemented using D flip-flops per standard design.



Top-level I/O

Inputs

clk – Boolean clock

sc – Boolean count enable

Outputs

Q[3..0] – 3 bit binary output

Testing

The circuit was tested by starting with clk = 0 and sc = 0. clk then was set to switch every 40 ns. sc was set to 1 after 40 ns, and was kept high for the remainder of the test. Q started to change once sc was set to 1 and continued to increase. Thus, the circuit successfully implemented the 4-bit counter.