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DESIGN PROCEDURE OF A PUSH PULL CURRENT-FED DC-DC CONVERTER

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***Abstract*— Some of the major drawbacks of Voltage-fed converter can be resolved by its Current-fed counterpart with its certain practical advantages. The recent increase in interest and use of current-fed converters calls for establishing a systematic design methodology. While some papers have provided useful insights to these converters, elaborate design steps are not available in literature. This paper presents complete design process of a push-pull current-fed converter.**

Index Terms — Current-fed Converter, DC-DC Converter, Push-pull Converter, Boost-derived Converter.

INTRODUCTION

Voltage-fed isolated converter topologies have some serious drawbacks. They invariably consist of input capacitor to lower input voltage ripple & spikes and output low-pass filter to reduce output voltage ripple. This low-pass filter consists of an inductor in series with the secondary rectifier assembly, along with the shunt capacitor. For multi-output converter there would be inductors for each output. With increased number of outputs, size and cost of multiple inductors becomes a serious concern, while the presence of inductor at the output can make cross-regulation poor. Voltage-fed converter requires non-zero dead time between the turn-on of the switch sets. During this dead time the secondary diodes free-wheel to continue the inductor current. This freewheeling current must be nullified on the following turn-on. This can create a low impedance path across the voltage source due to diode turn-off time during this nullification duration. The low impedance may lead to transformer saturation. Flux imbalance is a major problem in voltage-fed converters. It can cause serious damage if proper preventive steps are not taken.

Most of the problems of voltage-fed converters can be resolved or restricted by bringing the output inductor to the primary. This series connected input inductor, provides an instantaneous high impedance, thereby restricting sudden change in current. The inductor, as in Weinberg circuit, can be brought in the form of a flyback transformer, feeding either the input or the output. This flyback transformer feeds its secondary when the push-pull transformer operates in non-overlapping mode. However, in the overlapping mode of operation, no energy is transferred through this transformer.

If it can be ensured that the push-pull switches (Q1 and Q2) are operating in the overlapping mode, an inductor can be safely connected in series with the input as shown in Figure 1. This topology can also be derived from boost converter by inserting a transformer. Thus, this is a boost-derived topology.

The very presence of series inductor at the input reduces turn-on and turn-off current transients, limits flux imbalance and restricts transformer saturation by providing instantaneous high impedance at the input. Further, there is no need of filter capacitors at the input, making the system compact and simple. There is no problem arising from long lead lengths of the input supply as this will merely add to the input inductance.

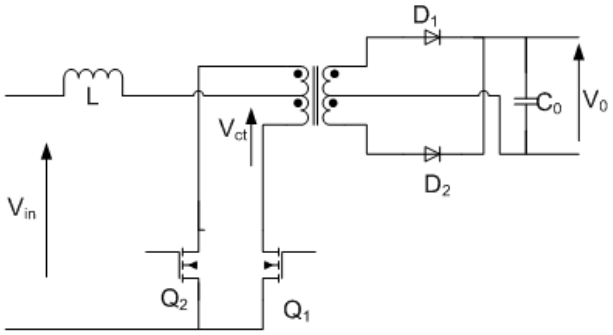

Figure 1 : Current-fed Push-Pull DC-DC converter

OPERATION

As stated earlier, the push-pull switches (Q1 and Q2) are operating in the overlapping mode, i.e., the duty cycle of each switch D, is greater than 0.5. As depicted in Figure 2, during interval [(D-1/2)T], (with T as the time period of one switching cycle), both Q1 and Q2 remain on. The flux in the transformer is cancelled by the simultaneous conduction of its two primary windings in mutually opposite directions. The transformer thus cannot sustain any voltage across its primary and will

appear shorted. The total input voltage, V_{in} is thus impressed across the inductor. Due to this applied voltage, current through the inductor rises in linear fashion. As there is no emf induced in the transformer secondary there is no energy transfer to the output side during this interval. Hence, from this perspective, this can be called as off period. Hence,

$$t_{off} = \left(D - \tfrac{1}{2}\right)T \quad (1)$$

During this interval, the load is supplied by the energy stored in the output capacitor. Switches Q1 and Q2 each carry half the inductor current.

During next interval upto T/2, only one switch, say Q2, remains on. The voltage across L reverses its polarity, to maintain the current level constant. Inductor current decreases linearly, transferring energy to the transformer through the upper primary. As a result, the lower secondary conducts and supplies energy to the output capacitor C_o and load. From the point of view of energy transfer to secondary, this interval can be called as the on period. Hence,

$$t_{on} = T/2 - (D - 1/2)T = (1 - D)T \quad (2)$$

For the next t_{off} period, both Q1 and Q2 remain on. During the next t_{on} interval, Q1 is turned on, thereby repeating a process as earlier for Q2, transferring energy to the secondary.

The output voltage can be controlled through pulse width modulation (PWM), as in voltage fed converters, except that the pulse width applied to a switch should lie between duty cycle above 0.5 to below 1.0, to ensure operation in the overlap mode. Operation below 0.5 duty cycle implies discontinuous mode of operation.

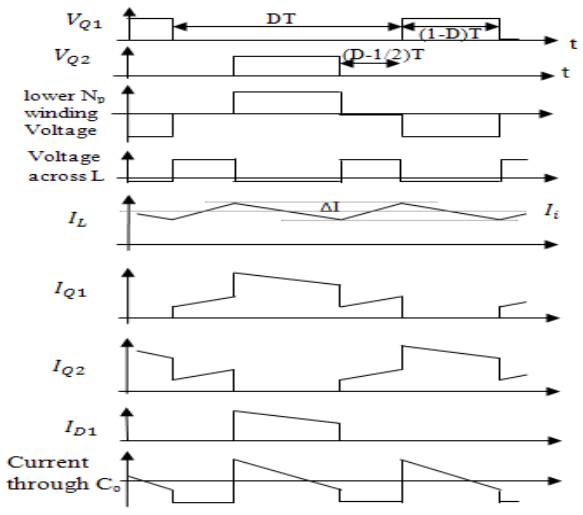

Figure 2 : Voltage & Current waveforms for the current-fed converter

DESIGN ASPECTS

Duty Ratio Determination

The voltage appearing across any switch in its off state, is twice the voltage across half of the primary. So the voltage level at the primary side of the transformer should not be boosted to a very high level, which would otherwise overstress the switches. Thus, for optimum voltage boost, the transformer center-tap voltage may be set as:

$$V_{ct} \simeq 1.05 \times V_{in,max} \quad (3)$$

When both the switches are on, there is no energy transfer to secondary. Transformer primary cannot sustain any voltage across it and so it is short circuited. Current through the inductor increases linearly during this interval. Thus,

$$V_{in} = \frac{2L\Delta I}{t_{off}} \quad (4)$$

Now, when only one switch is on i.e. for t_{on} duration, energy is fed to transformer secondary, when,

$$V_{ct} = V_{in} + \frac{2L\Delta I}{t_{on}} \quad (5)$$

Hence,

$$V_{ct} = V_{in} + \frac{V_{in} \times t_{off}}{t_{on}} = V_{in} \times \frac{1}{2(1-D)} \quad (6)$$

Transformer Turns Ratio

The transformer primary voltage is known and secondary voltage is the rated output voltage. Thus, the transformer turns ratio can be expressed as :

$$n = \frac{N_p}{N_s} = \frac{V_{ct}}{V_0} \quad (7)$$

Inductor Design

Considering an efficiency of η, the average input current can be expressed as:

$$I_i = \frac{P_0}{\eta \times V_d} \quad (8)$$

Now, a low value of inductance may cause the current to become discontinuous whereas a very high value of inductance will compromise size and weight constraints. Hence, putting a limit on the allowable current ripple magnitude,

$$\Delta I = x I_i \quad (9)$$

where, $0.05 \le x \le 0.3$ for optimal operation.

With output voltage V_o being constant and $n = \frac{V_{ct}}{V_0}$ (which is already fixed), it implies that V_{ct} is constant.

However,

$$V_{in} = V_{ct} \times 2(1-D) = \frac{2L\Delta I}{t_{off}} \quad (10)$$

Rearranging (10),

$$L\Delta I = V_{ct} \times 2(1-D) \times (D-\frac{1}{2})T$$
$$= \frac{V_{ct}}{2f_S} \times (3D-1-2D^2) \quad (11)$$

From (11), $(\Delta I)_{\max} = \frac{V_{ct}}{16Lf_S}$, from which,

$$L = \frac{V_{ct}}{16 \times f_S \times (\Delta I)_{\max}} \quad (12)$$

Input rms ripple current is given by :

$$I_{i,rms}^2 = \frac{1}{3}\{(I_i+\Delta I)^2 + (I_i-\Delta I)^2 + (I_i^2-\Delta I^2)\} \times (2D-1)$$
$$+\frac{1}{3}\{(I_i+\Delta I)^2 + (I_i-\Delta I)^2 + (I_i^2-\Delta I^2)\} \times 2(1-D)$$
$$= \frac{1}{3}(3I_i^2+\Delta I^2) \quad (13)$$

With $\Delta I = xI_i$,

$$I_{i,rms} = \sqrt{\frac{I_i^2}{3}(3+x^2)} \quad (14)$$

Here, primary peak current magnitude,

$$I_{i,pk} = I_i + \Delta I = I_i(1+x) \quad (15)$$

With L, $I_{i,rms}$, $I_{p,pk}$ available, the inductor can be designed using standard methodologies.

Maximum energy handled by the inductor, is :

$$E = \tfrac{1}{2} LI_{i,pk}^2 \quad (16)$$

Hence, Area Product is given by :

$$A_p = A_w A_c = \frac{2E}{K_w K_c J B_m} mm^4 \quad (17)$$

Here, A_w= window area in mm^2, A_c= core cross-sectional area in mm^2, K_w= window utilization factor, K_c= crest factor, J= current density in A/ mm^2, B_m= maximum flux density in Wb/ m^2.

Number of turns is given by :

$$N = \frac{LI_{i,pk}}{A_c B_m} \quad (18)$$

The length of air gap to be provided (neglecting Fringing), is given by :

$$l_g = \frac{\mu_0 N^2 A_c}{L} mm \quad (19)$$

Transformer Design

The rms current through half of the primary push-pull winding of transformer is equal to the rms current through a switch, which is given by :

$$I_{p,rms}^2 = \frac{1}{3}\left\{\frac{(I_i+\Delta I)^2}{4} + \frac{(I_i-\Delta I)^2}{4} + \frac{(I_i^2-\Delta I^2)}{4}\right\} \times (2D-1)$$
$$+\frac{1}{3}\{(I_i+\Delta I)^2 + (I_i-\Delta I)^2 + (I_i^2-\Delta I^2)\} \times (1-D)$$
$$= \frac{1}{3}(3I_i^2+\Delta I^2) \times (\frac{3-2D}{4}) \quad (20)$$

With $\Delta I = xI_i$,

$$I_{p,rms} = \sqrt{\frac{I_i^2}{12}(3+x^2) \times (3-2D)} \quad (21)$$

This is maximum when D is minimum.

Here also, peak current magnitude, $I_{i,pk} = I_i + \Delta I$

The rms current through half of the secondary center-tapped winding of transformer is equal to the rms current through a diode, which is given by :

$$I_{s,rms}^2 = \frac{1}{3}\{(I_i+\Delta I)^2 + (I_i-\Delta I)^2 + (I_i^2-\Delta I^2)\} \times (1-D) \times n^2$$
$$= \frac{1}{3}(3I_i^2+\Delta I^2) \times (1-D) \times n^2 \quad (22)$$

Again, with, $\Delta I = xI_i$,

$$I_{s,rms} = \frac{nI_I}{\sqrt{3}}\sqrt{(3+x^2) \times (1-D)} \quad (23)$$

Secondary peak current is given by :

$$I_{s,pk} = (I_i + \Delta I) \times n \quad (24)$$

The voltage induced at the center tap of transformer primary is given by :

$$V_{ct} = \frac{N_p(\Phi_m - (-\Phi_m))}{(1-D)T_S} = \frac{2N_p A_c B_m}{(1-D)T_S} = \frac{2N_p A_c B_m f_S}{(1-D)} \quad (25)$$

Similarly voltage induced at the secondary of transformer is given by :

$$V_o = \frac{2N_S A_c B_m f_S}{(1-D)} \quad (26)$$

The Primary turns is given by :

$$N_p = \frac{V_{ct}(1-D)}{2A_c B_m f_S} \quad (27)$$

The Secondary turns is given by :

$$N_s = \frac{V_O(1-D)}{2A_c B_m f_S} \quad (28)$$

To calculate Area Product required,

$$A_w K_w J = 2(I_{p,rms} N_p) + 2(I_{s,rms} N_s)$$
$$= 2.I_{p,rms} \cdot \frac{V_{ct}(1-D)}{2A_c B_m f_S} + 2.I_{s,rms} \cdot \frac{V_O(1-D)}{2A_c B_m f_S}$$
$$= \frac{(1-D)}{A_c B_m f_S}[V_{ct} \times I_{p,rms} + V_o \times I_{s,rms}] \quad (29)$$

or, $A_w A_c = \frac{(1-D)}{K_W J B_m f_S}[V_{ct} \times I_{p,rms} + V_o \times I_{s,rms}]$

Thus,

$$A_p = \frac{(1-D)}{K_W J B_m f_S}[V_{ct} \times I_{p,rms} + V_o \times I_{s,rms}] \quad (30)$$

Referring to cores with known Area Product data, the proper core can be selected and with known rms currents, conductors of required size can be selected. The actual primary and secondary turns can be calculated from (27) and (28).

Output Capacitor Selection

Rms current at the output of the common cathode diode pair is given by :

$$I_{o,rms}^2 = \frac{1}{3}\{(I_i+\Delta I)^2+(I_i-\Delta I)^2+(I_i^2-\Delta I^2)\}\times 2(1-D)\times n^2$$
$$= \frac{2}{3}(3I_i^2+\Delta I^2)\times(1-D)\times n^2 \quad (31)$$

The Average or output DC current is given by :

$$I_o = \frac{(I_i+\Delta I)+(I_i-\Delta I)}{2}\times 2\times(1-D)\times n$$
$$= 2(1-D)nI_i \quad (32)$$

The rms ripple current through capacitor is:

$$I_{d,cap}^2 = I_{o,rms}^2 - I_o^2$$
$$= \left[2(1-D)(2D-1)\times I_i^2 + \frac{2}{3}(1-D)\times\Delta I^2\right]\times n^2 \quad (33)$$

Substituting, $\Delta I = xI_i$, the rms ripple current is given by :

$$I_{d,cap} = nI_i\sqrt{2(1-D)[2D-1)+\frac{1}{3}x^2} \quad (34)$$

This current causes the pre-dominant ripple in the output voltage by virtue of the voltage drop across the ESR of the capacitor. Hence, the ESR of the capacitor should be less than :

$$ESR = \Delta V/I_{d,cap} \quad (35)$$

At the instant when capacitor starts discharging, energy in the capacitor is :

$$E_1 = 0.5CV_{d,\max}^2 \text{ Joules} \quad (36)$$

At the end of the discharge period, i.e. at $t_{off} = \left(D-\frac{1}{2}\right)T$, energy stored in the capacitor is :

$$E_2 = 0.5CV_{d,\min}^2 \text{ Joules} \quad (37)$$

Thus, for constant output power P_o, from (36) and (37) :

$$E_1 - E_2 = 0.5C(V_{d,\max}^2 - V_{d,\min}^2) = P_0(D-\frac{1}{2})T \quad (38)$$

Rearranging, the Capacitance value is given by :

$$C = \frac{P_O(2D-1)}{(V_{d,\max}^2 - V_{d,\min}^2)\times f_S} \quad (39)$$

Considering allowable output ripple voltage peak to peak as :

$$\Delta V_{p-p} = y\times V_o \quad (40)$$

$$V_{d,\max} = V_o + \Delta V_{p-p} \quad (41)$$

$$V_{d,\min} = V_o - \Delta V_{p-p} \quad (42)$$

Hence, the Capacitance value is given by :

$$C = \frac{P_o(2D-1)}{4y\times V_o^2\times f_s} \quad (43)$$

Semiconductor Selection

Primary Switches

Maximum voltage across switches is given by:

$$V_{DS,\max} = 2\times V_{ct} \quad (44)$$

Maximum current through switches is given by:

$$I_{D,\max} = I_{p,pk} = I_i + \Delta I = I_i\times(1+x) \quad (45)$$

Secondary diodes

Peak reverse voltage across diodes is given by:

$$PIV = 2V_o \quad (46)$$

The peak current through diodes is given by:

$$I_{D,\max} = I_{s,pk} = (I_i+\Delta I)\times n = I_i(1+x)\times n \quad (47)$$

For all the semiconductor components, an appropriate Safety Factor (SF) should be used. Hence, all the right hand side values in (44) to (47) must be multiplied by SF.

CONTROLLER DESIGN

In case of voltage-fed DC-DC converter, non-zero dead-time must be provided between turn-on of alternate switches. This is mandatory to prevent the occurrence of dead short across a voltage source with low impedance.

However, in current-fed converters, overlapping of the on duration of its switches is necessary for its operation. The instantaneous high impedance provided by the input inductor prevents current overshoot during overlapped operation.

The PWM controller can be realized by using a suitable combination of standard integrated circuits.

Transfer Function

The transfer function of the converter power stage can be derived by using state space average technique. The transfer function can be given as :

$$T_{ps}(s) = \frac{\tilde{v}(s)}{\tilde{d}(s)}$$
$$= \frac{V_o}{(1-D)}\times\frac{-\frac{i_L L}{2n(1-D)V_O}s+1}{\frac{LC_O}{4n^2(1-D)^2}s^2+\frac{L}{4n^2(1-D)^2R}s+1} \quad (48)$$

In the above model, the ESR of the output capacitor is neglected while R is the load resistance.

From (48), it can be seen that like other boost derived converter this converter also exhibit a right half plane zero (RHPZ) in small signal model. This can be attributed to the presence of the input inductor, which is used to store energy first and then feed to the secondary at a later instant, thereby producing a delay.

The right half plane zero (RHPZ) is a serious issue with these converters, as it limits the loop bandwidth and can cause instability, if not dealt

properly. Thus, it is very important to locate the position of the RHPZ and design the compensation network. From (48), the angular frequency of RHPZ is :

$$\omega_z = \frac{2n(1-D)V_o}{i_L L} \quad (49)$$

DESIGN EXAMPLE

Design Specification

Here a current-fed converter is designed with the following specifications:
Input Voltage Range, V_{in} = 42 to 55 V DC
Output Voltage, V_o = 110 V DC
Maximum output power, P_o = 300 W
Switching frequency, f_s = 50 kHz

Duty Ratios Determination

Here, $V_{ct} \simeq 1.05\times55 = 57.75 \approx 58V$
With $V_{in,\min} = 42V$, maximum duty cycle of a switch is given by :

$$D_{\max} = 1 - \frac{V_{in,\min}}{2V_{ct}} = 1 - 0.362 = 0.637$$

With $V_{in,\min} = 55V$, minimum duty cycle of a switch is given by : $D_{\min} = 1 - 0.474 = 0.525$

Transformer turns ratio

$$n = \frac{N_p}{N_s} = \frac{V_{ct}}{V_o} = \frac{58}{110} = 0.527$$

Inductor Design

Considering 90% efficiency, maximum average input current can be calculated as:

$$I_{i,\max} = \frac{P_O}{\eta \times V_{in,\min}} = \frac{300}{0.9\times42} = 7.94 \approx 8A$$

Allowing 20% ripple in input current (i.e. x=0.1 for 20% peak to peak ripple) maximum input current ripple magnitude is :

$$(\Delta I)_{\max} = 0.1\times8 = 0.8A$$

So, minimum inductance required is given by :

$$L_{\min} = \frac{58}{16\times50\times10^3\times0.8} = 90.63\mu H$$

Input ripple current rms is calculated as :

$$I_{i,rms} = \sqrt{\frac{8^2}{3}(3+0.1^2)} = 8.01A$$

Primary peak current magnitude, $I_{i,pk}$ = 8.8A
Maximum energy that must be handled by the inductor, E = $0.5\times90.63\times8.8^2$ = 3.5 $\times10^{-3}$ Joules
Thus, Area Product is given by :

$$A_p = \frac{2\times3.5\times10^{-3}}{0.4\times1\times3\times10^6\times0.2} = 2.9\times10^4 \ \text{mm}^4$$

The Ferrite core selected is EE 42/21/15 which has :
A_w= $2.56\times100\text{mm}^2$, A_p= $4.569\times10^4\text{mm}^4$, A_c= $1.82\times100\text{mm}^2$, l_m= mean magnetic length= 97.2mm
Number of turns :

$$N = \frac{90.63\times10^{-6}\times8.8}{1.82\times100\times10^{-6}\times0.2} = 22$$

With current density, J = 3A/mm^2, conductor area is a_c = 8.01/3 = 2.67 mm^2. Selected wire size is SWG 14.
Air gap length, l_g = 1.22mm
The actual air gap length needed will be higher due to Fringing effect.

Transformer Design

The maximum rms current of transformer half primary push-pull winding (for D_{min} = 0.525) is :

$$I_{p.rms} = \sqrt{\frac{8^2}{12}(3+0.1^2)\times(3-2\times0.525)} = 5.6A$$

The maximum rms current of transformer half secondary center-tap winding is given by :

$$I_{s,rms} = \frac{0.527\times8}{\sqrt{3}}\sqrt{(3+0.1^2)\times(1-0.525)} = 2.9A$$

Secondary peak current $I_{s,pk}$ = 8.8×0.527 = 4.64 A
Window area is calculated as :

$$A_p = \frac{(1-0.525)}{0.4\times3\times10^6\times0.2\times50\times10^3}[58\times5.6 + 110\times2.9] = 2.5\times10^4\ mm^4$$

Core selected is EE 42/21/15 with specification mentioned earlier.
Number of primary turns is :

$$2N_p = \frac{2\times58\times(1-0.525)}{2\times1.82\times100\times10^{-6}\times0.2\times50\times10^3} \approx 16$$

Secondary turns is calculated :

$$2N_s = \frac{2\times110\times(1-0.525)}{2\times1.82\times100\times10^{-6}\times0.2\times50\times10^3} \approx 30$$

Primary conductor size is given by :
$\alpha_p = 5.6/3 = 1.87mm^2$. Selected wire is SWG 16.
Secondary conductor size is given by :
$\alpha_s = 2.9/3 = 0.97mm^2$. Selected wire is SWG 18.

Output Capacitor Selection

With 3% allowable ripple in DC output voltage i.e. y = 0.015, the output capacitor is calculated as :

$$C = \frac{300\times(2\times0.637-1)}{4\times0.015\times110^2\times50\times10^3} = 2.26\mu F$$

The ripple current through the capacitor is :

$$I_{d,cap} = 0.527\times8\sqrt{2(1-0.525)[(2\times0.525-1)+\frac{1}{3}\times0.1^2}$$

= 0.948 A

Thus maximum permissible ESR of capacitor is given by: $ESR = \frac{0.03\times110}{0.948} = 3.48\Omega$

Semiconductor Selection

Consider Safety Factor, SF = 2.
Primary Switches:
Maximum voltage across the switches is:
$V_{DS,max}$ = 2×58×2 = 232 V
Maximum current though the switches is:
$I_{D,max}$ = 8.8×2 = 17.6A
Secondary diodes:
Peak reverse voltage across diodes is given by:
PIV = 2×110×2 = 440V
The peak current through diodes is given by:
$I_{D,max}$ = 8.8×0.527×2 = 9.27 A

MATLAB SIMULATION

Based on the designed values, MATLAB simulation was carried out for the converter system. The waveforms matched the theoretically predicted curve shapes, except for the starting transients.
In the simulation model the switches were considered ideal, and transformer was considered to have zero leakage inductance and zero winding resistance.
The source voltage was varied randomly between the limits specified in the design.
The simulation results are shown in Figure 3 & 4.

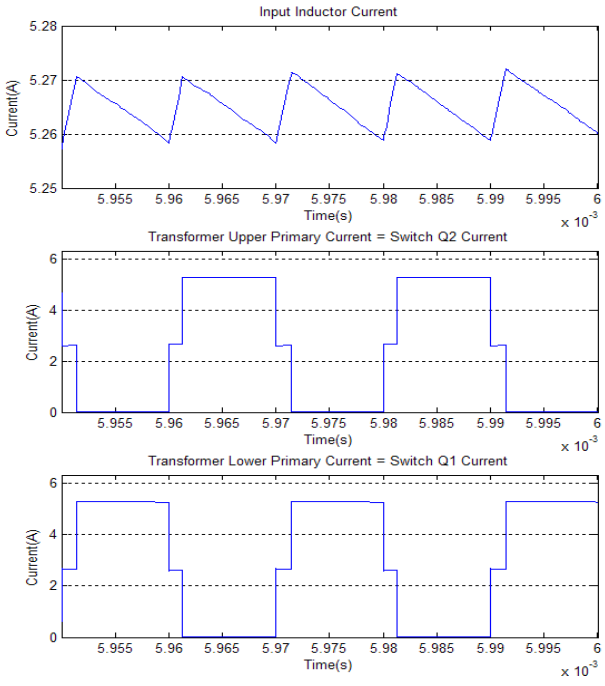

Figure 3 : MATLAB simulation waveforms for (a) inductor current and (b) & (c) switch currents or transformer primary winding currents

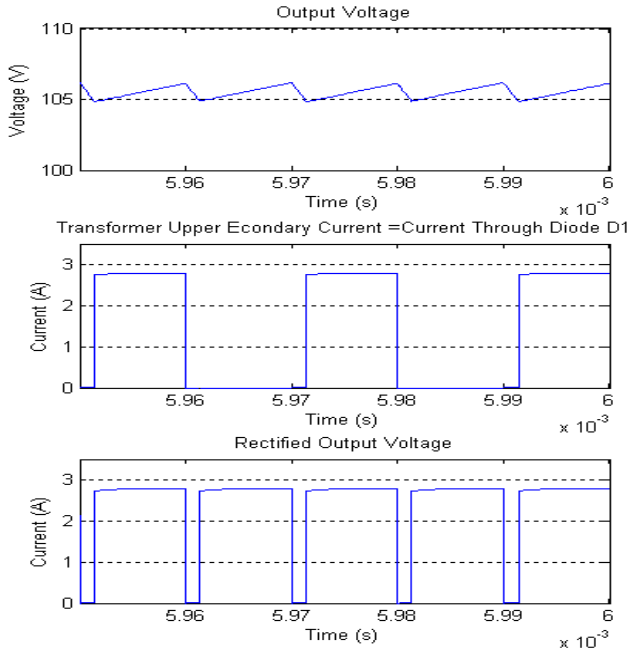

Figure 4 : MATLAB simulation result for (a) output voltage, (b) current of diode D1 and (c) output current at the common cathode of the diodes

LEAKAGE ENERGY RECOVERY BY CLAMP

One of the drawbacks of current fed topology is the generation of high voltage spikes across the switches due to the energy stored in transformer leakage inductance. Usually snubber/clamp circuits are used to protect the switches, thereby dissipating the stored energy. Alternatively, an energy recovery clamp can be used to recover this stored energy as depicted in Figure 5. This clamp should start to feed the energy back to the source when the voltage across the switches crosses a predetermined threshold.

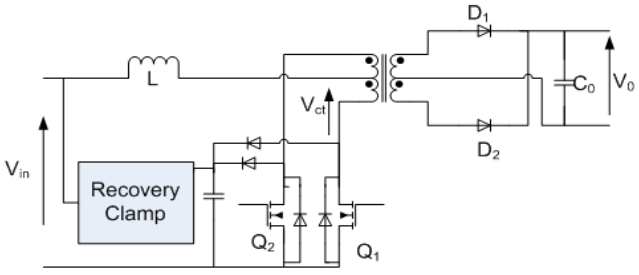

Figure 5 : Use of an energy recovery clamp to recover trapped energy in leakage inductance back to the source

EXPERIMENTAL RESULTS

An experimental prototype was fabricated in the laboratory using the above design and tested for

its performance. The set-up is shown in Figure 6. The control circuit is assembled onto a PCB. The power semiconductors are mounted on the heatsink with wire connections upto PCB and transformer. The transformer is visible in the middle and the inductor on the right hand side.

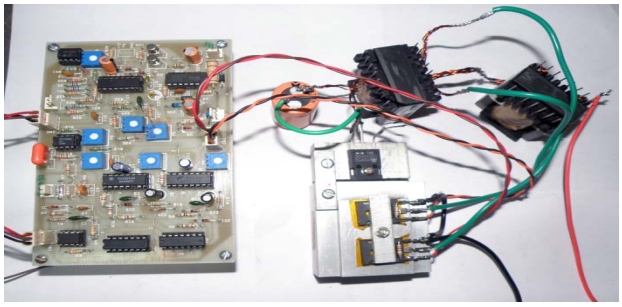

Figure 6 : Experimental prototype for laboratory testing

CONCLUSION

A detailed step-by-step design process of a push-pull current-fed DC-DC converter is presented in this paper. The theoretical design is supported by simulation and experimental verification. As further work, the design process can be extended to current-fed full bridge topology.

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