Name:_____

CSCE 587 – Project 0
Requirement A and B
Spring 2016
Tool Familiarization

I. Overall Project #0 Description – This project has two requirements (deliverables) that you will need to develop and submit for a grade, broken down into Project 0.A and Project 0.B. Ensure you read through the entire project description prior to beginning the project. The goal of this project is to design and test two simple devices establishing baseline knowledge in 1) the use of the tools for the course and 2) the Microprocessor/Digital system design flow.

A. Task A: Design and implement a simple 2-to-4 Decoder that accepts as input a 2-bit input and generates as an output one of four unique symbols as output. In short, you wish to illuminate one of four LEDs on the development board based on the binary input. From the customer, the requirements are

a. Must accept two data inputs, each of which is a 2-bit number representation.
b. Must accept an additional input allowing the selection of one of the 2-bit inputs to process. Both input-> output matchings will work the same.
c. The system will illuminate one of four output LEDs as outlined in the table below (0="Off", 1="On"):

Data Input Bit 1	Data Input Bit 0	LED 3	LED 2	LED 1	LED 0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

B. Task B: Design and implement a 8-Bit Counter that accepts as input two selection switches 1) to support an automated clock or manual clock toggle mode (where a single button push equates to a clock pulse) and 2) to support display of the values for bits [7 6 5 4] or bits [3 2 1 0] to output LEDs where a value of '1' is equated to an LED being "on" and a value of '0' is equated to an LED being turned "off". The change in output state should be humanly visible when the automated clock is used, therefore, a clock enable will be needed.

II. Overall Project #0 Instruction/Submission. Model and simulate in VHDL using Quartus II and Modelsim. Demonstrate correct operation for a subset of the possible inputs, full factorial testing is not necessary.

1. Deliverables (see "Additional Guidance and Hints" for formatting requirements):
   - Functional Block Diagrams (in PowerPoint) describing the primary modules and interconnects for both part A and B.
   - Your VHDL files with comments (submit both VHDL design and TB files).
   - Ensure proper naming of variables/signals/ports in keeping with templates.
   - Submit and demonstrate test bench VHDL code for both top level designs.

2. Demonstration :
   - Be prepared to demonstrate the operation on the FPGA board for both A and B. This may or may not happen depending on the comfort level of each student with the material and tools.

3. Due: In accordance with the current course schedule.

4. Instructor Initials _____ Date_____

III. Additional Guidance and Hints:

A. Project Directory Hierarchy: Before starting work, implement the following project directory hierarchy below:

```
lastname_firstname_CSCE587_Project_0
   hardware
      ModelSim_Sim - ModelSim VHDL simulation project directory
      Quartus_cores - all Quartus cores (and files generated or used by those cores)
      Quartus_project - Quartus project folder project files
      VHDL_Design - all of your VHDL model source code files
      VHDL_Testbench - VHDL test bench source code and test bench supporting files

   Software_Model_Sim -MATLAB files supporting simulation.
```

B. Softcopy submission guidance: archive your clean (i.e. remove temp files) Project folder into a .zip file. Change the zipped-file name to "`firstname_lastname_hardware_proj0.A.zip`" or "`firstname_lastname_hardware_proj0.B.zip`". Then submit the file via Blackboard.

C. Look at the VHDL code examples. Included are components to use (i.e. Clock Enable).

D. If it takes you longer than 10-15 minutes to figure out what to do next, clear an error message or get unstuck, stop what you are doing and get in touch with the instructor.

E. If you receive assistance from anyone other than the instructor or refer to material other than that provided on the course website or textbook, document it (where it was applied) in your code.