Analog to digital conversion
Exercises

Marcel Pelgrom

Pelgrom Consult
micro-electronics
training and consulting

pelgromconsult@kpnmail.nl

Slide 1

1

Exercises Analog-to-Digital conversion

Please note:
You are encouraged to work in teams of 1 or 2 students, no more.
Discuss and find the right solution.
Submit your solution in one pdf file to pelgromconsult@kpnmail.nl 24 hour before the next class. Handwritten and scanned solutions are okay, as long as I can read it (no Sanskrit, Mandarin, etc).
Start by mentioning your name(s) and university ID nr.
Teams can submit a single file with two names and university IDs.

In General:
You must argue any result you obtain.
A simulation is allowed as a form of illustration, but cannot replace thinking.

You are **never** allowed to copy text from any source, even not from my book. Pictures can be copied (please with ref)

2

Chapter 2, Sampling

1. The input signal to a sampling system consists of 4 frequencies: 3, 5, 9 and 15 MHz. The system samples at f_s=17 Ms/s. Draw the spectrum upto f_s. By accident the sample rate is set to f_s=17 ks/s. Draw the spectrum upto f_s.

2. How much SNR can be obtained if a signal of 10 MHz is sampled with a sample rate of 80 Ms/s with 5 ps_{rms} jitter. What happens with the SNR if the sample speed is increased to 310 Ms/s at the same jitter specification. A band-pass filter limits the bandwidth to a range from 9 to 11 MHz. What is the SNR in that 2MHz bandwidth for both sample rates. (2.10)

3. An FM signal of 100 kHz bandwidth at 10.7 MHz carrier is sampled. Unfortunately a neighboring digital circuit running at 13.5 MHz generates unwanted frequency components at 13.5 MHz and its second and third harmonic frequencies. Define a sub-sample frequency that maximizes the distance between the wanted and the spurious signals.

4. An audio system produces samples at a rate of 44.1 ks/s. With a maximum audio signal of -6 dB of the full-scale between 10 and 20 kHz, propose an alias filter (number of poles) that will reduce the frequency components over 20 kHz to a level below -90 dB? (2.9)

3

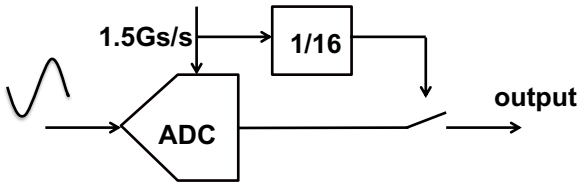
5. A sinusoidal signal of 33 MHz is distorted and generates 2nd and 3rd harmonics. It is sampled by a 32 Ms/s or a 132 Ms/s system. Draw the resulting spectra. What sample rate do you favor? (2.1)

6. A signal source delivers a signal that consists of three components: at 3MHz, 4MHz and 5MHz. The signal is processed by a sampling system with an unknown sample rate. The output contains in the 0-0.5MHz band only frequencies at 0.27 MHz, 0.36 MHz, 0.45 MHz and 0.46 MHz. What sampling frequency was used? Complete the spectrum till 1 MHz. (2.16)

7. An RF oscillator at 2.45 GHz contains harmonic distortion products at 2x and 3x time the oscillation frequency. The available spectrum analyzer can measure up to 10 MHz, but has a 10 GHz input bandwidth sampling circuit with variable sampling rate upto 10 GS/s. Advice how to measure the harmonic distortion. (2.17)

8. A 2 MHz signal is sampled by a 100 Ms/s clock with 10 ps_{rms} jitter. In the digital domain the band of interest is limited to DC-5 MHz, Calculate the SNR. The digital circuits repeat a process every 10 μs and this is the cause of the 10 ps jitter. What is the resulting spectrum in DC -5 MHz?(2.18)

4



9. A very fast ADC samples a 750.366 MHz sinewave at a 1.5 Gs/s sample rate. The fast data stream is subsampled: every 16th sample is passed to the output. Draw the resulting spectrum including a 2nd and 3rd order distortion component at -55 dB and -45 dB resp. Give a reason for using this subsample arrangement (Pernillo 2011).

10. A sinusoidal RF signal of unknown frequency is entering a 10 Ms/s sampling system. Its presence is clear from a 20 kHz tone in the spectrum of the sampled output signal. The sample rate is increased with 1 ks/s, shifting the 20 kHz output tone to 1 kHz. What is the lowest RF frequency that is responsible for this tone?

5

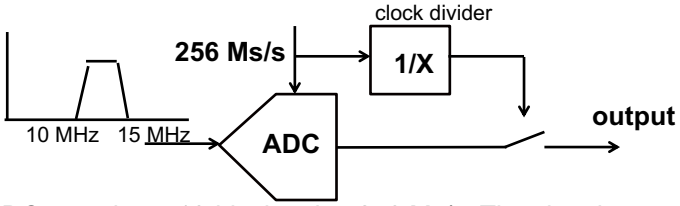
11. A 5G communication system uses the full 27-30 GHz band.
What is the minimum sample rate?
Draw the 0-40GHz spectrum after sampling with a downsample rate of fs=9 Gs/s .
Give one advantage and one disadvantage of this fs choice.
The input signal is distorted with 2nd and 3rd order components resulting in spurious tones from 54-60 GHz and 81-90 GHz.
Draw the 0-40GHz spectrum after sampling.
Chose an alternative fs, where no distortion components fold into the signal bandwidth after sampling.

12. A 5G communication system uses the 27-30 GHz band.
A RF mixer stage performs a perfect down modulation with f_{LO}=26 GHz followed by a sharp 5 GHz low-pass filter and an AD converter.
What is the lowest sample rate? Draw the 0-10 GHz spectrum after sampling with that rate.
Available AD converters can maximally operate at 7 Gs/s. Propose a better system solution (you may change anything except the 27-30 GHz band and no faster sampling than 7 Gs/s).

6

13. A signal source delivers a signal that consists of three components: at 27MHz, 38MHz and 41MHz. The signal is processed by a sampling system with an unknown sample rate. The output contains in the 0-5MHz band only frequencies at 1 MHz, 2 MHz, 3 MHz and 5 MHz without overlap. What sampling frequency was used? Complete the spectrum till $2f_s$.

14.



An ADC samples a 10-bit signal at 256 Ms/s. The signal occupies the band from 10 MHz to 15 MHz.
A clock divider reduces the output sample rate to 256/X Ms/s.
What is the ENOB in 10-15 MHz if X=1?
What is the ENOB in 10-15 MHz if X=8?
Propose X for the lowest output rate. Draw for that X the frequency spectrum.

7

Chapter 3, T&H circuits

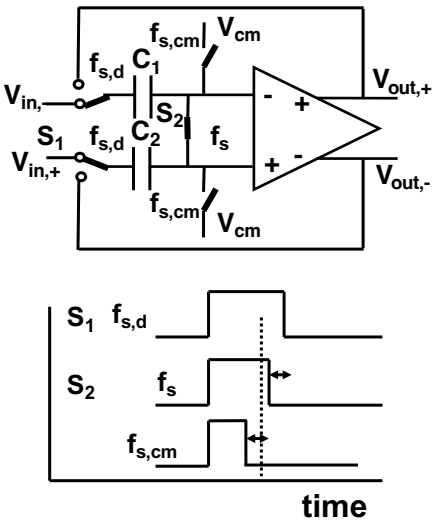
1. In a sampling system the sample rate is 500 Ms/s with an input signal of range of 1 Vpeak-peak and a clock jitter of 1 ps_{rms}. A performance of 50 dB is required for all signals in the Nyquist baseband. Calculate the capacitor size. (3.10)

2. In an analog-to-digital converter the sampling speed is 250 Ms/s with an input range of 1.41 $V_{peak-peak}$. A performance of 90 dB is requested in a band from 30 to 40 MHz. The input sampling capacitor may contribute half of the noise energy. Calculate its size. (3.9)

3. A differential track-and-hold circuit shows a random offset. Design a switching sequence that performs the track-and-hold function and implements chopping to cancel the offset. Is there is practical solution for a singe-sided track-and-hold circuit? (3.12)

8

Project 1-A



This fully differential T&H circuit uses bottom plate sampling. C_1=C_2. The input signal is a 1 GHz sine wave, where each input swings between +250 mV and -250 mV.

9

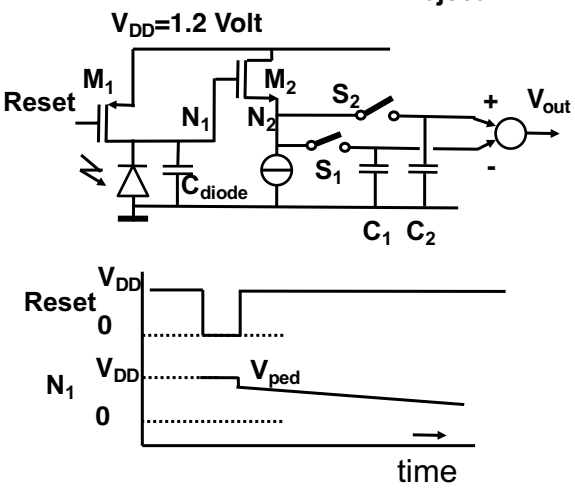
This fully differential T&H circuit uses bottom plate sampling. The input signal is a 1 GHz sine wave, where each input swings between +250 mV and -250 mV. f_s=3 Gs/s, C_1=C_2.

A. Determine C_1=C_2, for SNR=70 dB as the SNR on the hold capacitor(1 pts)
B. What is the signal to noise ratio on C_1? (1 pts)
C. Use now: C_1=C_2=1 pF, Calculate the W/L ratios of S1 and S2 when β_{square}= 200 $\mu A/V^2$ and L_{min}=0.1 μm, V_T=0.35V and V_{DD}=1.2 V. (1 pts)
D. The sample pulse is jittery: σ_t=0.1ps_{rms}. Calculate the **total** SNR. (1 pts)
E. The switch S_2 is designed with a PMOS and NMOS transmission gate (parallel transistors driven by opposite phase fs clocks), while Vcm=0.6 Volt. The PMOS switches off 5 ps later than the NMOS. What will happen? (1 pts)
F. Propose alternative (you may change anything). (1 pts)
G. For 10-bit performance calculate the A_{DC} and the UGBW of the OTA. (2 pts)

The use of a simulator is permitted, however points will only be awarded for reasoning, not for simulation.

10

Project 1-B



This is a typical T/H circuit for sensing radiation hitting a diode. The diode is biased to V_{DD} when M1 is conductive. After this reset, radiation will generate hole-electron pairs in the diode, causing its voltage to drop.
After a certain period of time the voltage drop is sampled as the required signal.

Transistor data: $V_{T,M1}$=-0.3 Volt, W_{M1}=0.5 μm, L_{M1}=0.1 μm, $V_{T,M2}$=0.1+0.1√(|V_{BS}|+0.6) Volt, $\beta_{square,M2}$= 200 μA/V^2 , L_{M2}=0.1 μm, ($V_{GS,M2}$-$V_{T,M2}$)=150 mV.
for both transistors: C_{ox}=4 fF/μm^2, C_{olap}=1 fF/μm. The effective diode capacitance C_{diode} = 10 fF is constant over voltage. The current source delivers 20 μA and requires V_{N2}>0.1 Volt for proper operation.

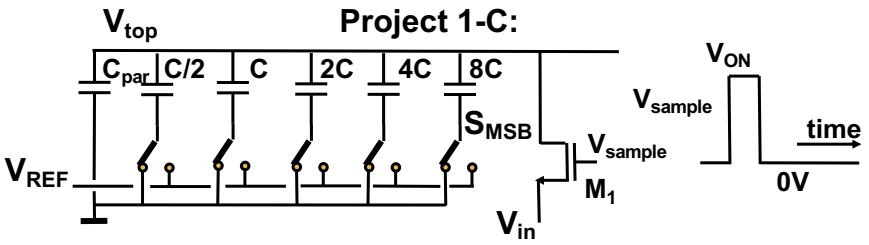
11

A. Calculate W_{M2} if the current source delivers 20 μA. (1 pt)
B. Calculate the maximum usable voltage swing on node N_1 and N_2. Take the pedestal step into account (cross talk of reset pulse and charge splitting) and the attenuation of the source follower. Ignore the capacitance of M_2 (2 pts)
C. What is the signal to noise ratio SNR on N_1 (ignore M_2)? (1 pt)
D. Give an estimate of the additional capacitance M_2 contributes and the SNR when M_2 is included. (1 pt)
E. With S_1, S_2, C_1, C_2 and the subtraction node, a correlated double sampling system is implemented. Complete the timing diagram with the signals S_1 and S_2 (where V_{DD} level means “on” and 0 means “off” and S_1 switches before S_2). (1 pt)
F. Explain which errors are cancelled by correlated double sampling and which errors remain. (1 pt)
G. Use now: C_1=C_2=1 pF, Calculate the SNR of V_{out}. (1 pts)
H. Give an estimate for the time S_1 and S_2 should be “on”, the resistance and capacitance of the switches is zero. (1 pt)

The use of a simulator is permitted, however points will only be awarded for reasoning, not for simulation.

12

Project 1-C:



This capacitor array is often used in ADCs and DACs and is used for building a signal on V_{top} that is controlled by toggling the switches from ground to a reference voltage V_{REF}=1Volt.
The voltage V_{in} is sampled on the top-plates of the capacitors V_{top}.
C=10 fF, 2C=20 fF etc, C_{par}=0 fF, $V_{in}= V_{DC}+0.3\sin(\omega t)$ Volt. V_{DC}=0.3 V

The sampling switch is implemented by NMOS transistor M_1 with the following parameters: threshold voltage M_1: 0.2 Volt, current factor for a square (W=L) transistor: 200 $\mu A/V^2$, dimensions
W/L= 10/0.2 μm, Cox=4fF/μm^2, $C_{gate,drain,overlap}$=0.3 fF/ μm.
In case your computer gives trouble, read microAmp and micrometer,
Use the strong-inversion square root transistor equation.

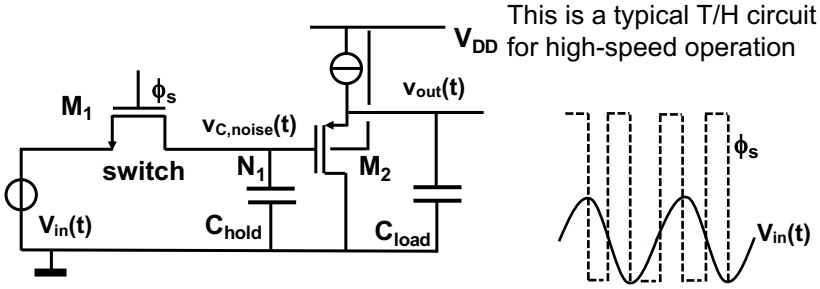
13

A. Calculate the SNR after sampling.
B. The C/2 capacitor is implemented as a series connection of two capacitors of 1C. How does the SNR change?
C. After sampling all switches are toggled to V_{REF}, what is the SNR?
D. A parasitic C_{par}=45 fF is present from now on. What is the SNR?
E. Due to a design error the bottom-plate-to-ground switch of 8C is missing! What is the SNR after sampling, what is the SNR when after sampling without ground connection of 8C, this 8C bottom-plate is connected to V_{REF}? Assume 8C was uncharged V_{8C}=0.
F. The sample switch is implemented with an NMOS transistor M_1. M_1 needs a drive voltage (V_{GS}-V_T) of 0.2 V. What is the minimum voltage for V_{ON}?
G. What is in that case the pedestal step? Make a drawing of V_{top} for a full sampling cycle.
H. What is the settling time for lowest and highest signal level?
I. Sketch the expected distortion THD from DC to max.
J. Comparing the SNR and the THD: advice whether to increase or decrease C_{par}.

14

Project 1-D:

This is a typical T/H circuit for high-speed operation



Transistor data:
$V_{T,M1}$=0.3 Volt, $\beta_{square,M1}$= 250 $\mu A/V^2$, W_{M1}=10 μm, L_{M1}=0.1 μm,
$V_{T,M2}$=-0.4 Volt, $\beta_{square,M2}$= 100 $\mu A/V^2$, L_{M2}=0.1 μm,
$(V_{GS,M2}-V_{T,M2})$=150 mV. $V_{in}(t)>=0$ V for all time.
for both transistors: C_{ox}=4 $fF/\mu m^2$, C_{olap}=1 $fF/\mu m$. The current source delivers 200 μA and requires >0.1 Volt for proper operation.
V_{DD}=1.2 V, C_{hold}= 1pF, C_{load}= 0.25pF, ϕ_s switches with 50% duty cycle between 0 and V_{DD}.
The amplification factor of the source follower is 0.9.

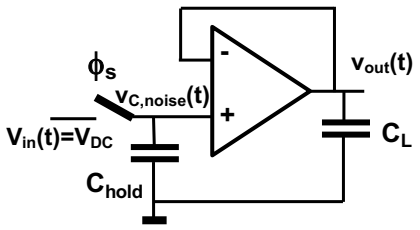
15

A. Calculate W_{M2} if the current source delivers 200 μA. (1 pt)
B. Calculate the pedestal step (cross talk of reset pulse and charge splitting) Ignore the capacitance of M_2 (1 pts)
C. What is the maximum usable voltage swing on the input node.
D. What is the signal to noise ratio SNR on N_1 (ignore M_1,M_2)? (1 pt)
E. Give an estimate of the additional capacitance that M_1,M_2 contribute to C_{hold}, in hold mode, assume W_{M2}=20 μm. (1 pt)
F. For V_{in}=0.25 V calculate the bandwidth input-output. (1pt)
G. The input signal is $v_{in}(t)=0.25+0.25\sin(2\pi t/T)$ with T=2 ns, see graph. The sample pulse has a frequency of 1 GHz. Its falling edges are on the highest and lowest values of the sine wave. The switch turns on/off infinitely fast. Plot the voltages on N_1 and on the output for a complete period of the sine wave. Explain the shape of each part of the curves.
H. What is wrong with the circuit?
J. What is the THD due to the input switch for an input signal: $v_{in}(t)=0.25+0.25\sin(2\pi ft)$ V, with f=100 MHz.

The use of a simulator is permitted, however points will only be awarded for reasoning, not for simulation.

16

Project 1-E:



17

Chapter 4, Quantization

1. An ideal 6-bit quantizer samples at 160 Ms/s, in the following digital circuit a filter section limits the band of interest to 5 MHz, what is the expected signal to noise ratio in this band due to the quantization white noise. What combinations of resolution and sampling speeds are possible for digital representation of this signal next to an 6-bit resolution and a sample rate at 160 Ms/s.

2A. A 500 MHz signal with 50 $mV_{peak\text{-}peak}$ amplitude must be converted by an N-bit ADC. The sample clock shows a jitter of 1 ps_{rms}, samplimng on a 2 pF sample capacitor. The second order harmonic distortion of the signal is at -60 dB. An ENOB=7 bit is required, Calculate N, round up to integer. The signal amplitude is now increased.
2B. All values (jitter, sample cap, distortion) remain the same and use N=8. At what amplitude is ENOB=7.4 bit reached?

3. A 12-bit ADC is fully differential with an input range of -0.25 V to +0.25 V on each input pin. An INL curve showing a third order behavior with INL excursions between +1 LSB, -1 LSB is present. The input sampling capacitor between the input pins equals 100 fF. Calculate the ENOB, give an improvement advice.

18

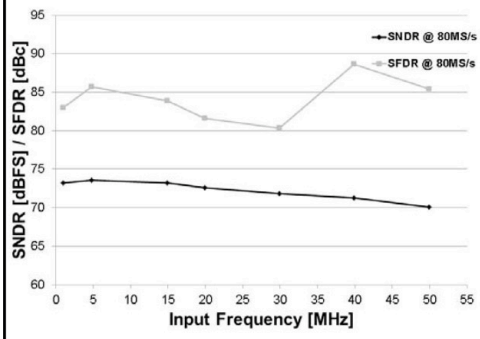
4. A 14-bit ADC has to convert a 2 $V_{peak\text{-}peak}$ signal at a quality level corresponding to ENOB=12.5 bit. The sampling capacitor is 1 pF. How much in-band distortion can you tolerate? (4.4)

5. An ideal 6-bit ADC samples at 200 Ms/s. The band of interest is DC to 6.25 MHz. What is the expected signal to noise ratio in this band due to the quantization white noise? What combinations of resolution and sampling speeds are possible next to 6-bit resolution and a sample rate at 200 Ms/s?

6. The output signal of an FM intermediate frequency circuit has a bandwidth of 100 kHz at a carrier frequency of 10.7 MHz. An analog-to-digital converter samples this signal at 5.35 Ms/s. What resolution is needed to obtain a SN_QR due to quantization of 13.8 bit in 100 kHz bandwidth.

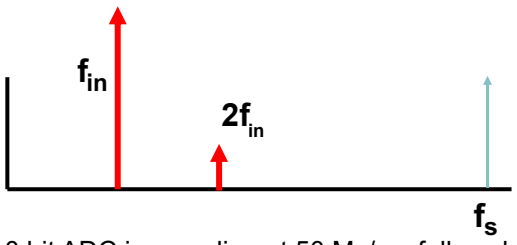
19

7. Calculate the Walden F.o.M. for this converter.
Is this a good number for a recent (2012-15) design?



Technology	65nm CMOS
Resolution	14 bit
Sample Rate	80 MS/s
Input Range	2.4 $V_{PP\text{-}DIFF}$
ADC Core Area	0.55mm²
Supply Voltage	1.2V
SNDR @ 80MS/s	73.6dBFS @ 5MHz
	71.3dBFS @ 40MHz
SFDR @ 80MS/s	85.7dBc @ 5MHz
	≥80.3dBc thru 40MHz
Power	23.0mW (analog)
	8.1mW (digital)
	31.1mW (total)
FoM [SNDR + $10\log_{10}(f_s/(2*P))$]	164.7dB

20



8. An ideal 10 bit ADC is sampling at 50 Ms/s a full-scale 12 MHz input signal with 2nd harmonic. The second harmonic is expected worst case to be around 54 dB level. What is the expected SNDR?
The measurement shows an SNDR of 56 dB. At what level is the 2nd harmonic? In order to measure the 2nd harmonic exactly, a filter around $2f_{in}$ is applied to limit the quantization noise to -90 dB. What bandwidth is required?
There are only low-pass filters (from DC to BW) available. How can you measure the 12 MHz signal and its harmonic?

21

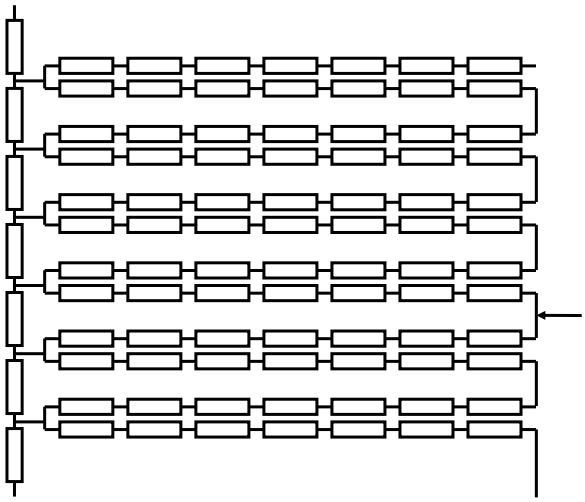
9. An 10-bit ADC samples at 200 Ms/s an input signal of 500 mV_{pp} in a band between 80-90MHz.
The input uses a 3 pF capacitor and the jitter on the sampling signal is $1ps_{rms}$.
What is the effective resolution (ENOB) in the 10 MHz band between 80 MHz and 90 MHz?

The succeeding digital electronics uses only every second sample and discards the intermediate samples, thereby halving the sample rate.
What will happen to the signal and what is the ENOB in the resulting 10 MHz bandwidth?
Is it a good idea to reduce the sample rate of the ADC to 100 Ms/s?
Is there a better solution resulting in a higher ENOB?

22

Chapter 7 DAC

1. A 10-bit digital-to-analog converter is constructed from a 4-bit coarse ladder with 16 resistors of 300 Ω and 16 6-bit fine ladder sections with 64 resistors of 50 Ω each, calculate the maximum resistance in this ladder to the grounded reference terminals.



27

3. In a resistor string digital-to-analog converter all resistors are 10% larger. What is the change in INL? What other changes must be expected?

In a resistor string digital-to-analog converter all even numbered resistors are 2% larger, while the odd numbered are on spec. What is the change in INL and in THD? What other changes must be expected?

In a resistor string digital-to-analog converter all resistors are randomly either 1% larger or 1% smaller. What is the change in INL, THD and SNR? What other changes must be expected?

28

4. An 8-bit unary current-steering digital-to-analog converter is driving a 1 kΩ load.
Each current source has a parallel impedance of 5 MΩ and 0.2 pF. Sketch the resulting distortion behavior over frequency. Now the unused current is fed in a second 1 kΩ load allowing differential operation. There is a mismatch of 1% between both load resistors. Sketch the distortion as a function of frequency.

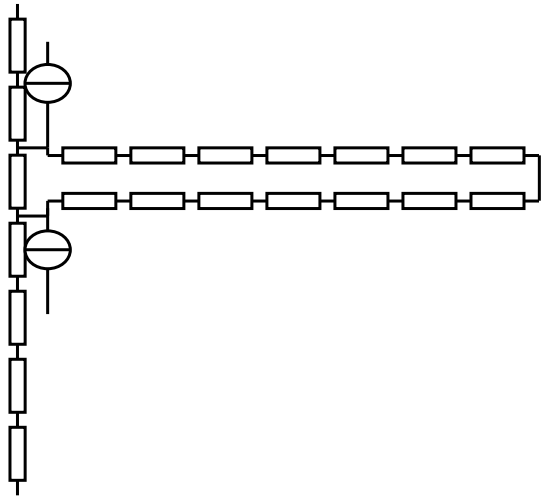
5. An 8-bit digital-to-analog converter based on a resistor string, suffers from a linear gradient of 1% over the entire structure. So $R(i+1)=R(i)+\Delta R$. where $\Delta R = 0.01R_{average}/256$. What is the INL, DNL and THD?

6. In a current -steering digital-to-analog converter the current sources suffer each from random mismatch: Gaussian sigma=5% . What DNL can be achieved for a 12-bit unary architecture? How many bits can be implemented in binary format if a DNL 0.5 LSB ($=2\sigma$) must be achieved.

7. A level of HD2=-80 dB is required for a digital-to-analog converter. What is the maximum gradient that can be tolerated and what is the maximum random mismatch.

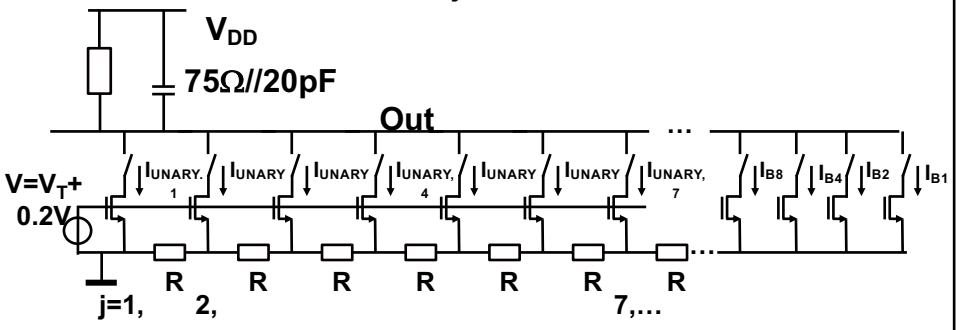
29

7.8 A 5-bit fine resistor string is directly via switches connected to a 5-bit coarse resistor string. As a consequence current from the coarse string will run via the fine resistor string. The resistors of the coarse string are 100 Ω each. What should be the value of the fine resistors if the maximum DNL due to the resistive loading of the coarse string must be less than 0.5 LSB?
Connect in the previous example a current source to both ends of the fine ladder. Does this resolve the DNL problem? Is this solution free of other DNL problems?



30

Project 2-A



An 10-bit current-steering digital-to-analog converter consists of a 6-bit unary array of MOS current sources and a 4-bit binary array. The output is loaded with a 75 Ohm resistor and a 20 pF capacitor. An output swing of $1V_{pp}$ is required. All INL and DNL values are referring to a 10-bit level. Assume R=0.

31

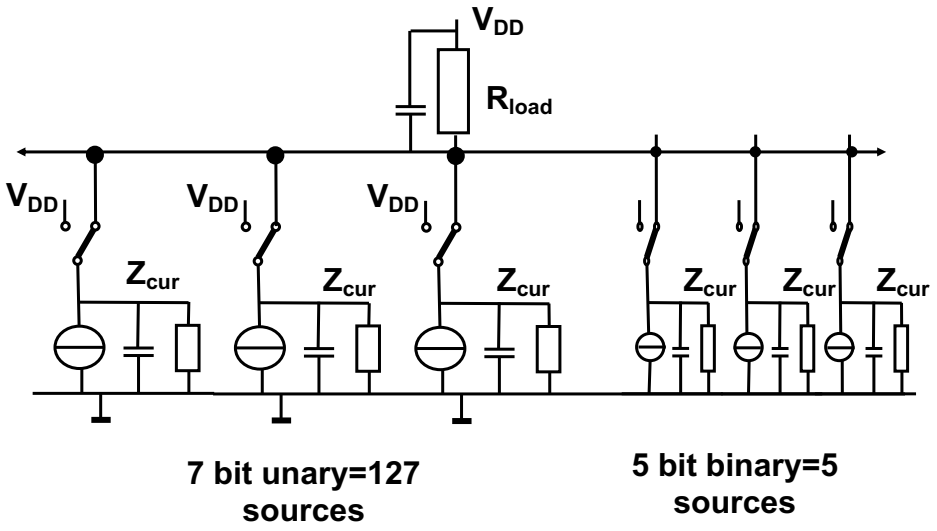
A. Calculate the values of the currents in the unary and binary part.
B. What is the small-signal -3 dB bandwidth.
C. What is the highest dV/dt at the output?
D. In the unary array, current source #35 deviates 0.02 mA,
where all other elements are perfect. Sketch the INL and DNL.
E. All unary current sources are subject to a Gaussian probability function with a mean=I_{unary} and a standard deviation.
Binary sources are ideal.
What is the maximum standard deviation of the Gaussian,
if the 3σ value of the DNL must be smaller than 0.5LSB.
F. What is the minimum area of the unary current source transistor when only the threshold mismatch is taken into account and A_{VT}=4mVμm

G. R=10 milliohm. All unary current sources are aligned in one long row connected by an ohmic line, which is perfectly grounded on the left side. How much will the 63th current deviate from ideal?

H. For the INL=0.5LSB case calculate the THD.

32

Project 2-B



33

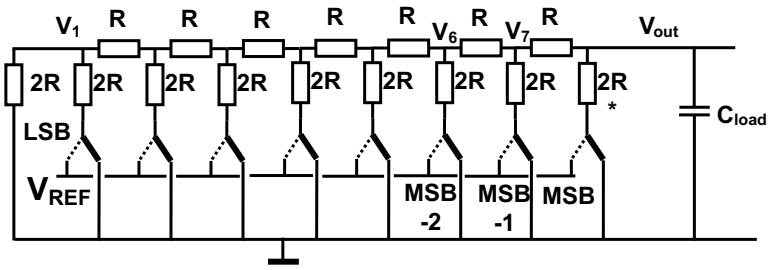
Project 2-B

An 12-bit current-steering digital-to-analog converter consists of a 7-bit unary array of MOS current sources and a 5-bit binary array. The output is loaded with a 75 Ohm resistor and a 20 pF capacitor. An output swing of $1V_{pp}$ is required.
All INL and DNL values are referring to a 12-bit level.

A. Calculate the currents in the unary and binary sections.
B. All current sources have a Gaussian variation of σ=1% of their unary or binary values. Estimate the 1-sigma variation of the INL and DNL.
C. The unary array consists of 127 currents sources. Now a gradient causes the currents to increase monotonically with a rate of 1%/127 for every next source. So current source #127 carries exactly 1% more current than #1, What is the HD2?
D. What is the frequency response?
E. All unary current sources have a parallel impedance of 100 MΩ//100 fF. Draw the HD2 in the output current as a function of frequency due to this impedance only.

34

Project 2-C



Note: due to the complexity of the circuit, it will be difficult to calculate some results exactly, a good estimate with correct arguments are sufficient.

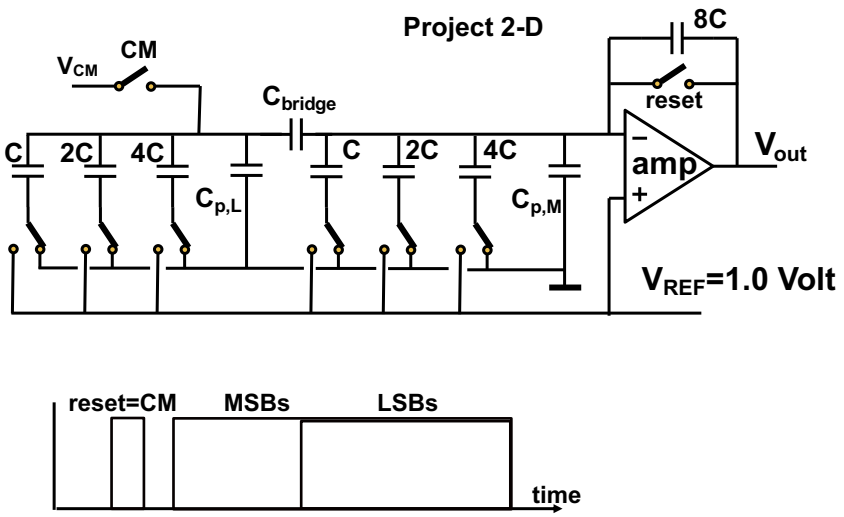
35

Project 2-C

An 8-bit R-2R ladder is given. R=1 kΩ, 2R= 2 kΩ, C_{load}=10 pF

A. Give the exact voltages on V_{out}, V_7, and V_6 if only the MSB switch toggles, only the MSB-1 switch toggles and only the MSB-2 switch toggles for ideal switches (9 results in total).
B. Estimate the maximum on-resistance of the switches for a maximum |DNL|=0.5 LSB.
C. Estimate the minimum off-resistance of the ground switch of the MSB only, for a maximum |DNL|=0.5 LSB.
D. Make a graph of the load current for V_{REF} for all codes.
E. Explain when this load current is a problem for the performance.
F. What is the maximum sample frequency if the output voltage needs to be stable within 0.5 LSB.
G. What is the THD of this circuit if only the 2R resistor (marked with *) deviates +1%?
H. Propose a CMOS transistor implementation of the switch for the MSB.
I. If all resistors show a resistance value varying with a Gaussian distribution around the nominal value of σ_R=0.01R and σ_{2R}=0.02R what is the maximum resolution of an R-2R digital-to-analog converter if 95% of the devices must show a |DNL| smaller than 0.5 LSB.

36



The amplifier has an amplification of 10^3 with a Unity Gain Bandwidth of 159 MHz.

37

Project 2-D

A 6-bit capacitive DAC is given (switch resistance =0, $C_{p,L}$=$C_{p,M}$ = 0)

A. What is the value for C_{bridge} to get a perfect transfer curve.

B. Draw the output voltage V_{out} for the digital input word: 101101 assuming an ideal opamp, the MSB is the first bit.

C. Now the opamp has a limited gain and bandwidth: what is the time constant for reset and what are the time constants for the MSB and LSB settling?

D. Now $C_{p,L}$=C and $C_{p,M}$ = 2 C, plot the transfer curve for the digital input range 101101 (45) to 110101 (53) what is the DNL of this converter.

E. Modify the bridge capacitor value to get an optimum transfer curve.

F. $C_{p,L}$=0 and $C_{p,M}$ = 0. In the LSB section, the actual value of the "4C" capacitor is 3.5C. Plot the transfer curve from 45 to 53 and what is the DNL?

G. In addition to the error in the LSB section now in the MSB section the "1C" capacitor is 1.25C in value. Plot the transfer curve from 45 to 53 and what is the DNL?

H. What is the signal-to-quantization power ratio of the output signal?

I. What is the signal-to-thermal noise ratio of the D-A conversion assuming no noise contribution of the opamp. C=10 fF.

J. Propose a CMOS transistor implementation of the switches

38

Chapter 8. ADC

1. A 7-bit full-flash converter with a total ladder impedance of 1kΩ is designed: the input transistors of the comparators have W/L=5/0.1 μm. During latching the drains of the input pair change 200 mV. The effective gate-drain capacitance is 0.2 fF/μm. What is the shape of the spike on the ladder and its time constant τ. Estimate the spike if Vin=0 and $V_{ref}/2$.

2. Rank the following design parameters for achieving a low BER in order of importance: the gate width of the latch transistors, the length, the current, the gate oxide thickness, the gate-drain overlap capacitance?

3 In a 6-bit full-flash 10 Gs/s analog-to-digital converter the wires of the clock lines must be kept as equal as possible. What is the maximum wireline difference that can be tolerated if the converter must operate at Nyquist frequency. Assume a propagation speed of 10^8 m/s.

4 Show that for a sinusoidal signal the digital output power of an N bit parallel output port is smaller than for a serialized single pin output.

5 How will comparator mismatch in a multiplexed successive approximation converter affect the performance?

39

6 A 7-bit flash converter uses 128 resistors of 25 Ω each with a 50 fF parasitic capacitance to each comparator. If the internal signal swing of the comparator is 1 V, calculate the kick-back amplitude. Does the kick-back vary with input signal level? Where is the worst case level?

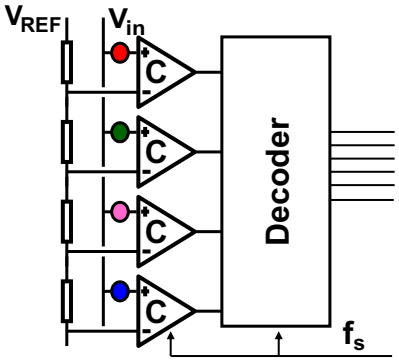
7 A sine wave must be converted with good absolute accuracy (without DC-offsets). No auto-zero or calibration mechanism is available. Give a reason why a flash converter is a better choice than a successive approximation converter.

8 Draw a transfer curve of a 2-bit coarse, 4 bit fine analog-to-digital converter. Both sub-ADCs are flash-type. Add the transfer curve in case one of the coarse comparators has an offset of 1% of the input range. Do the same if this offset applies to one fine comparator.

9 A 1.6 Gs/s analog-to-digital converter is build by multiplexing 64 successive approximation converters. If offsets are normally distributed calculate σ_{comp} for a 50 dB performance of 95% of the dies. The bandwidth of the T&H circuits is 1.5 GHz. How much variation is allowed on this bandwidth?

40

10, A Flash converter 6 bit, f_s=2.1Gs/s, has in input referred mismatch per comparator of σ_{in}=2 mV, the input range is 564 mV. The clock shows a jitter of σ_{fs}=1 ps_{rms}.
Advice whether a 1 GHz signal is converted >5.5ENOB in the presence of jitter and comparator mismatch.



41

11. In a 7-bit flash 10 Gs/s analog-to-digital converter the wires of the clock lines to the comparators vary in length. The lengths can be modelled as a Gauss distribution with a sigma of σ_L= 50 μm. Assume a propagation speed on the wires of 10^8 m/s.
What is the SNDR?

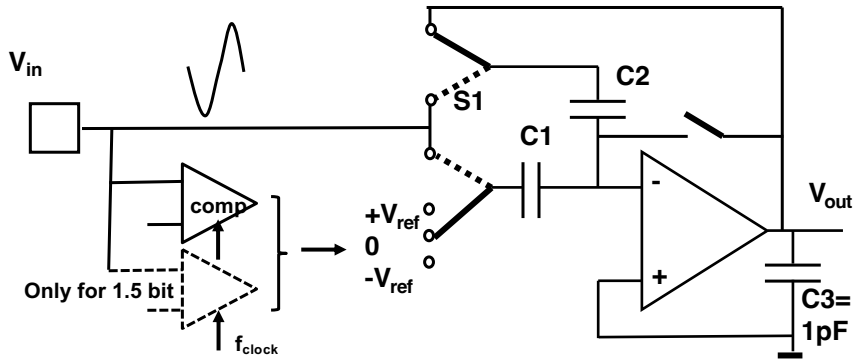
12. The ladder of a 7-bit flash ADC shows a linear gradient of 2%, so each resistor is 0.02 x $2^{-7}R_{tot}$ larger than its neighbor. V_{REF}=1V. What is the SNDR?

13. The comparators of a 7-bit flash analog-to-digital converter suffer from mismatch from the input transistors. If V_{REF}=1 Volt, and A_{VT}=4 mVμm, what is the area (WxL) of the input transistors for 95% yield on monotonicity.

14. A 7-bit, 10 Gs/s converter suffers from 2nd order distortion at -46 dB and 3rd order distortion at -50 dB, moreover the clock jitter is 0.2 ps_{rms}.
What is the best-case and the worst-case SNDR for a a maximum amplitude sine wave within bandwidth from DC to 1.5 GHz.
Still a bandwidth of 1.5 GHz is required, between what frequencies do you choose this 1.5 GHz, in order to get the highest SNDR for all signals in that band.

42

Project 3-A: MDAC



Design the FIRST MDAC stage for a pipeline converter.
Desired specification: 10-bit resolution, f_s=100 Ms/s, 50% duty cycle. 1 Vpp input. VDD=1.8V. Single ended. Mismatch sigma for capacitors:

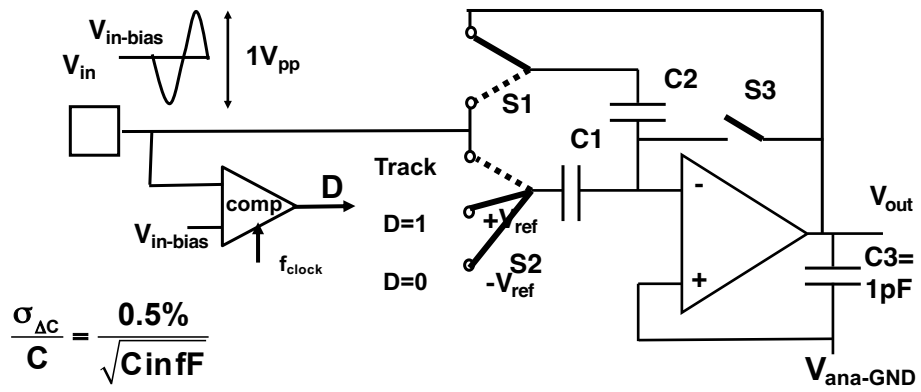
$$\frac{\sigma_{\Delta C}}{C} = \frac{0.5\%}{\sqrt{C \text{ in fF}}}$$

43

a. The MDAC is used for an exact multiply-by-2 converter (only 1 comparator is used). Suppose switches and opamp are ideal, calculate the value of C_1 and C_2 for 10-bit noise performance and 2-sigma yield. 2 pt
b. The capacitors are set to 1 pF each. The opamp gain and bandwidth are now modeled as a first order system with A_v as the gain and ω_{UGBW} as the unity gain bandwidth. Calculate both, to yield an error less than 0.5LSB. Give a minimum power estimate (based on slewing). 3pts
c. Sketch the voltages on the negative input terminal and the output terminal of the opamp for one clock cycle (sample, decide, subtract and transfer). 1 pt
d. Propose a suitable opamp structure (only schematic no W/L values) 1pt
e. The MDAC is modified to serve in a 1.5-bit pipeline ADC, with an extra comparator, and ref voltage what are the other necessary changes (capacitor values, A_v, ω_{UGBW}, I_{slew})?
f. When the drawn schematic is directly fed with an analog signal, this topology is called SHA-less (sample-and-hold amplifier less). The danger of this topology is timing skew between comparator and signal sample. Calculate for a 1.5 bit architecture the maximum allowable skew for a 1 V_{pp} 20 MHz signal.

44

Project 3-B: MDAC



$$\frac{\sigma_{\Delta C}}{C} = \frac{0.5\%}{\sqrt{C \text{ in fF}}}$$

The available opamp has a gain of 16000 (16.10^3) and a unity gain bandwidth of 159 MHz. Its input stage consists of a differential NMOST pair on top of a current source. The input transistors and the current source use V_{GS}-V_T=0.2 Volt. The power supply is 2.5Volt. The threshold voltage of the NMOST is V_T=0.4 Volt and the PMOST V_T= -0.4 Volt. Design an Input MDAC stage for a 12-bit pipeline converter with this opamp.

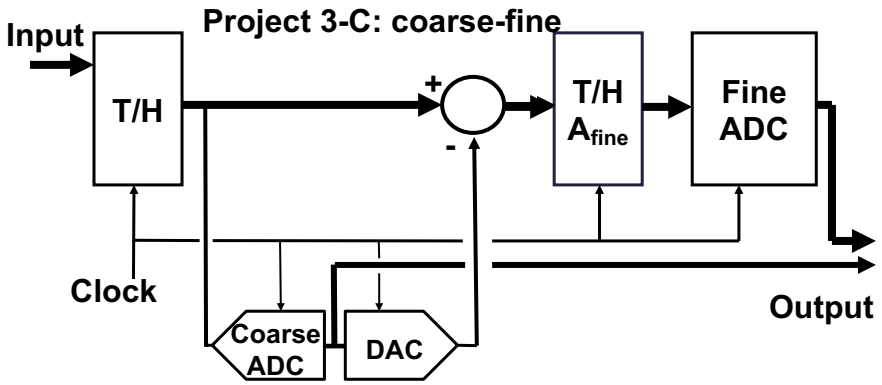
Slide 45

45

a. The MDAC is used for an exact multiply-by-2 converter for an $1V_{pp}$ input signal on a bias signal $V_{in-bias}$. Choose V_{ref+},V_{ref-},$V_{in-bias}$ and $V_{ana-GND}$ (1pt)
b. Sketch the voltages on the negative input terminal and the output terminal of the opamp for one clock cycle (sample, decide, subtract and transfer).
c. Replace the switches S1, S2 and S3 by suitable MOS transistors and sketch the drive voltages for each transistor. (2pts)
d. Indicate the change needed for bottom-plate sampling. (1pt)
e. Calculate the capacitor values based on an input sampling SNR of 74 dB. What 1-sigma error in amplification do you expect from capacitor mismatch? (2pt)
f. What is the maximum sample rate? (1pt)
g. The MDAC is modified to serve in a 1.5-bit pipeline ADC, with an extra comparator, and ref voltage what are the other necessary changes (capacitor values, A_v, ω_{UGBW}, I_{slew})? (1pt)
h. When the drawn schematic is directly fed with an analog signal, this topology is called SHA-less (sample-and-hold amplifier less). The danger of this topology is timing skew between comparator and signal sample. Calculate for a 1.5 bit architecture the maximum allowable skew for a 1 V_{pp} 20 MHz signal.

Slide 46

46



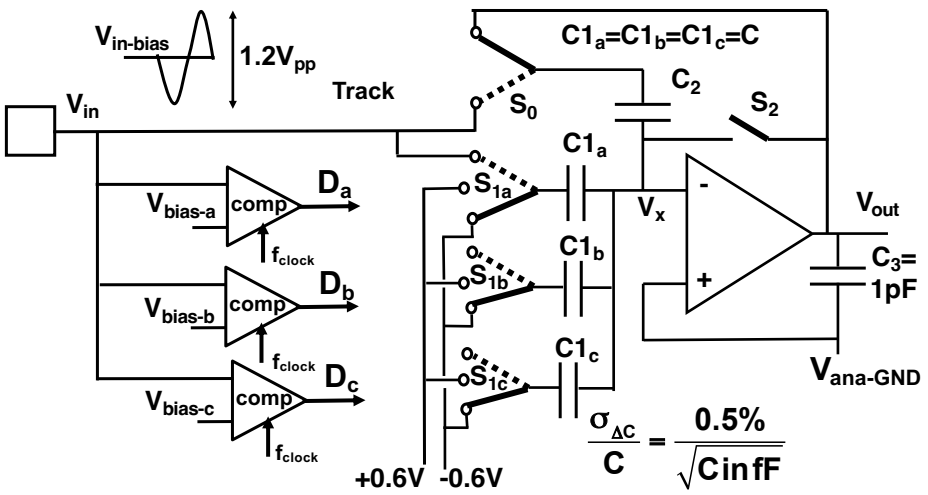
11 A 4-bit coarse, 4 bit fine analog-to-digital converter is used for 8-bit conversion of a 1 Vpp signal. The input TH is built with a flip-around architecture. The used opamps have a unity gain of f_{UGBW}=80 MHz.
The DC gain of the 2nd TH is A_{fine}=1.
Both sub-ADCs are flash-type.

47

a. What is the input voltage range of the fine ADC in case all components are ideal?
b. What is the maximum input referred mismatch error of the comparators in the coarse ADC to have a |DNL|<0.5LSB?
All other components are ideal (no need for statistics, just …mV)
c. All comparators in the coarse ADC are perfect, except the middle comparator (out of 15). The expected input referred mismatch of that comparator is +10 mV. Sketch the INL and DNL.
d. All components are perfect, except A_{fine}=0.9, draw the INL and DNL.
e. A_{fine}=1. All comparators of the **coarse** converter can have input referred mismatches between -10 and +10 mV. So the ideal fine ADC is extended to allow overrange. How many additional comparators must be used in the fine ADC?
f. All comparators of the coarse and the **fine** converter can have input referred mismatches between -10 and +10 mV. Propose a solution that achieves |DNL|<1 LSB.
g. If all comparators are perfect, to what sample rate is this converter limited if no overrange is used and |DNL|<0.5LSB is required?
h. What is the sample rate if the overrange of the fine ADC is 50% on each side with A_{fine}=1?
i. And what is the sample rate with A_{fine}=4.

48

Project 3-D: MDAC



This MDAC stage uses three comparators, their outputs determine whether after sampling, the switches S1 are connected to $+V_{REF}$ or $-V_{REF}$.
The opamp has a gain of 1000 (10^3) and a unity gain bandwidth of 159 MHz. $V_{in-bias}$=$V_{ana-GND}$=0V.

Slide 49

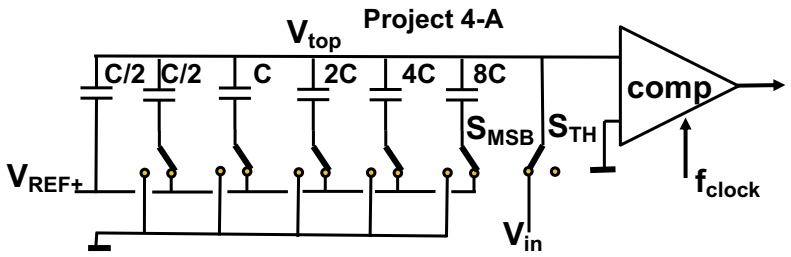
49

a. The MDAC is used in a pipeline converter for an 1.2V_{pp} input signal on a bias signal $V_{in-bias}$. What value is C_2 if the input range equals the output range for a 3x amplification.(1pt)
b. Calculate the capacitor values based on an input sampling SNR of 66 dB. (1pt)
c. What error do you expect from the limited DC-gain and the 1-sigma error in gain due to capacitor mismatch (calculate the error based on the difference between C_{1a} and C_{1b})? (1pt)
d. Choose the V_{bias} voltages of the three comparators for maximum tolerances at the comparator switching voltages. (1pt)
e. Draw the transfer curve: V_{out} versus V_{in}. (1pt)
f. Sketch the voltages on the negative input terminal V_x and the output terminal of the opamp V_{out} for one cycle (sample, decide, subtract and transfer) assuming V_{in}=0.1V. Indicate the settling tau's.(2pt)
g. What is the maximum sample rate? (1pt)
h. Replace the switches S_0, S_1 and S_2 by NMOS transistors and sketch the drive voltages for each transistor, include bottom-plate sampling. (1pt)
i. The danger of this topology is timing difference (skew) between comparators and signal sample. Calculate the maximum allowable skew for a 1 V_{pp} 8 MHz signal. (1pt)

Slide 50

50

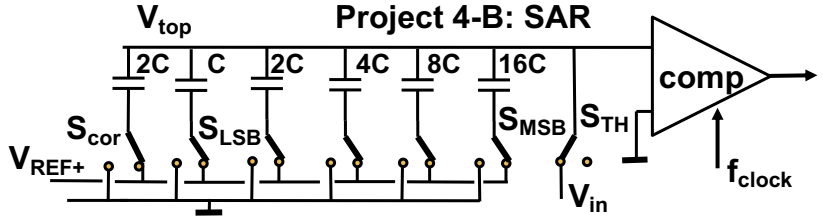
Project 4-A



A successive approximation converter with reference: V_{REF+}= +1.6 Volt.
A. Draw for V_{in}=0.43 Volt, the top plate voltage V_{top} starting with sampling till the last conversion cycle.
B. Due to a misunderstanding the left most C/2 was omitted, redraw the top plate voltage during conversion.
C.The C/2 capacitor is found! It is connected parallel to the 4C capacitor, redraw the top plate voltage during conversion.
D. Draw the transfer curve for all three cases.
E. When C=5 fF and the other capacitances scale with their indicated multiplier, what is the SNR for a 1 $V_{peak-peak}$ sine wave.
F. Make a plot of the energy delivered by V_{ref+} versus code.
G. Suppose all switches are 10 kOhm, and the comparator and decoding require 100 ps per decision independent of code, what is the maximum sampling speed of this converter.

51

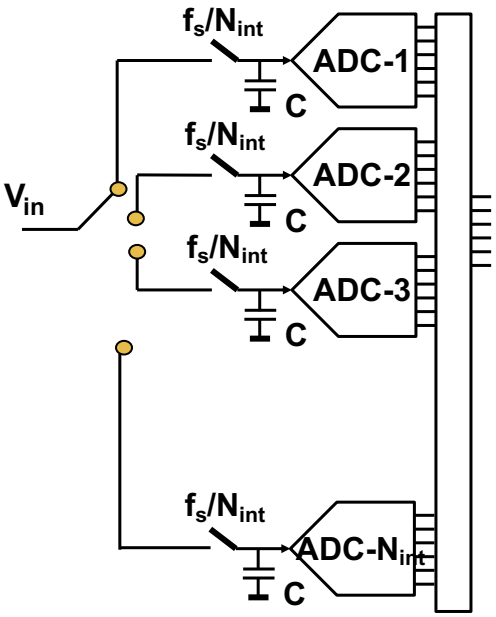
Project 4-B: SAR



A successive approximation converter with reference: V_{REF+}= +1.0 Volt.
A. Draw the top plate voltage V_{top} starting with sampling till the last conversion cycle for V_{in}=0.49 Volt and S_{cor} is not used and remains in its drawn position. What is the quantization error (in LSB)?
B. The comparator takes a wrong decision at the first cycle. Draw the top plate voltage and give the quantization error.
C. The error correction switch S_{cor} is now used. Draw for V_{in}=0.49 Volt the top plate voltage V_{top} and give the quantization error.
D. When C=5 fF and the other capacitances scale with their indicated multiplier, what is the SNR for a 1 $V_{peak-peak}$ sine wave.
E. What will determine the THD, and how can you improve?
F. Suppose all switches are 10 kOhm, and the comparator and decoding require 100 ps per decision independent of code, what is the maximum sampling speed of this converter.

52

Project 5-A Time Interleaved



A Time Interleaved ADC is designed to deliver 8 ENOB in a BW=500 MHz. $V_{in,peak\text{-}peak}$=1V

The following ADCs are available for this task:
- a full-flash converter f_s= 2 Gs/s and ENOB=5.5.
- a pipeline converter f_s=280 Ms/s and 9 ENOB.
- a SAR converter f_s=70 Ms/s and 11 ENOB.
- a dual-slope converter f_s=10 Ms/s and 10 ENOB.

53

A. Compare for every ADC what the consequences are for usage in a time-interleaved configuration, w.r.t. speed, resolution, N_{int}, expected overhead, comparator offset, and other relevant issues.
BW=500 MHz, fs>1 Gs/s.
B. What needs to be improved in the sampling mechanism of the pipeline and SAR converters so they can be used to implement the time-interleaving. What additional measures are needed to reach the required bandwidth?
C. For the pipeline converter the Walden F.o.M. is 60 fJ/conv. The SAR runs at 10 fJ/conv. Compare the power for both realizations, if the additional overhead for clock distribution and digital is 20%.
D. If no tricks (bridge cap in SAR and scaling in pipeline) are used, estimate how much capacitance will be used for the time-interleaved chip.
E. What is the jitter specification for the clock?
F. If the clock skew must be limited to 50 femtosec and the propagation speed of e-m waves over wires in ICs is 10^8 m/s, what is the maximum clock wire difference? What is the maximum signal wire difference?

54

Chapter 9 Sigma-Delta

2 An 6-bit analog-to-digital converter has to convert a signal bandwidth from DC to 50 kHz, but the converter can run up to 200 Ms/s. How much resolution by oversampling can be obtained? How would you implement that? A dither source is available. Can it be used to improve the accuracy?

3 A DC-voltage is applied to a first-order 1-bit sigma-delta modulator running at 1 MHz. What output frequencies are generated for input voltage values of 0%,10%,...100% of the range. What changes if the quantizer is replaced by a 3-bit analog-to-digital converter?

4 A first-order sigma-delta converter is extended with an integration stage in the feed-back path. Draw the STF and the NTF. Is this now a second-order sigma-delta modulator?

5 An oversample ratio of 64 is available to reach 110 dB SNR gain.What filter order is needed to achieve this result.

6 The digital-to-analog converter in the feedback path shows a 0.1% distortion component ($y=x+0.001x^2$). Sketch or simulate the effect in the frequency domain.

55

7 The second integrator of a second-order signal delta modulator shows a 0.1% distortion component. Sketch or simulate the effect.

8 A time-continuous sigma-delta modulator runs at a sample rate of 100 Ms/s. The filter has single poles at 30 kHz and 60 kHz and a zero at 10 MHz. Calculate the NTF and the STF.

9 Give an expression for the NTF and STF in a time-discrete sigma-delta modulator running at 100 Ms/s and with poles at 30 and 60 kHz.

10 A 1-1 cascaded sigma-delta modulator converts a bandwidth of 10 kHz with an oversampling factor of 512. There is a 2% mismatch between the gain of the analog filter in the first loop and the digital inverse filter. What will happen?

11 A first-order sigma delta modulator runs at a sampling rate of 10 Ms/s. The feed-back signal switches between 0 and 1 Volt. What is the output frequency if the input equals 0.5, 0.6, 0.9 Volt?

56

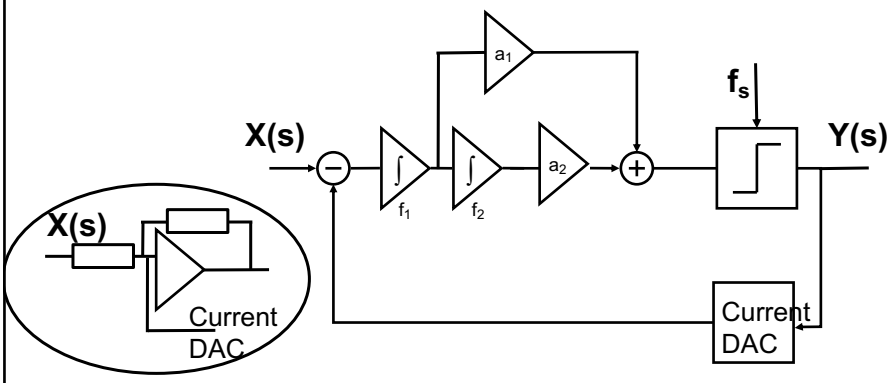
12 A first-order sigma delta modulator is part of a 1-1 cascade sigma-delta modula- tor. Its time-discrete filter is described by $z^{-1}/(1-z^{-1})$. Give a time discrete description for the digital compensation filter.
13 Is it possible to multiplex two identical first-order sigma-delta modulators that run on a sample-rate clock and a half-period delayed sample rate.
14 A 3rd order time-continuous sigma delta converter is used to convert a base band of 2 MHz with an oversample ratio of 64. At what level and frequency will a 255 MHz interferer signal of equal strength as the input signal, show at the output? What happens if this converter is changed into a time-discrete implementation.

15 What is the maximum SNR that can be obtained in a 1 MHz bandwidth that is 128 × oversampled if the feed-back DAC clock jitters 2 ps_{rms}?

16 A third-order time-continuous sigma delta modulator runs at a sampling rate of 5 Ms/s. A signal band of 20 kHz is required. The comparator and DAC can be assumed ideal, with only the gain uncertainty and the sampling uncertainty of the comparator needs to be taken into account. Set-up a 3nd order filter using capacitors, resistors and ideal opamps, that gives a maximum SNR ratio in this band.

57

Project 5: Sigma Delta



A second-order time-continuous sigma delta modulator runs at a sampling rate of f_s=5 Gs/s. A signal band of 20 MHz is required. The 1-bit comparator and DAC can be assumed ideal.

Slide 58

58

Project 5: Sigma Delta

a. Set-up a 2nd order filter: propose a_1 and a_2 for proper operation, that gives a maximum SNR ratio in the 20 MHz band. Assume the summation node ideal. Make a plot of the filter function.
b. Calculate the SN_QR at 20 MHz.
c. The input referred noise is 18mircoV$_{rms}$. Give a filter implementation using capacitors and ideal transconductances. Calculate the transconductance values and capacitors.
d. If the input summation node is designed with an opamp with equal resistors (see oval), propose a value for the resistors if their contribution to thermal noise is equal to the total input referred noise of the transconductances.
e. What is the effect of a 1 ps$_{rms}$ jitter on the SNDR if the jitter occurs only in the comparator? And if the jitter only affects the DAC?
f. The comparator and DAC produce a total delay of 40 ps. Is excess delay compensation needed?

Slide 59

59