



## Section 12. I/O Ports with Peripheral Pin Select (PPS)

This section of the manual contains the following topics:

|      |                                     |    |
|------|-------------------------------------|----|
| 12.1 | Introduction .....                  | 2  |
| 12.2 | I/O Port Control Registers .....    | 2  |
| 12.3 | Peripheral Multiplexing .....       | 7  |
| 12.4 | Peripheral Pin Select.....          | 9  |
| 12.5 | Port Descriptions.....              | 19 |
| 12.6 | Change Notification (CN) Pins ..... | 19 |
| 12.7 | Register Maps .....                 | 21 |
| 12.8 | Related Application Notes.....      | 22 |
| 12.9 | Revision History .....              | 23 |

12

I/O Ports

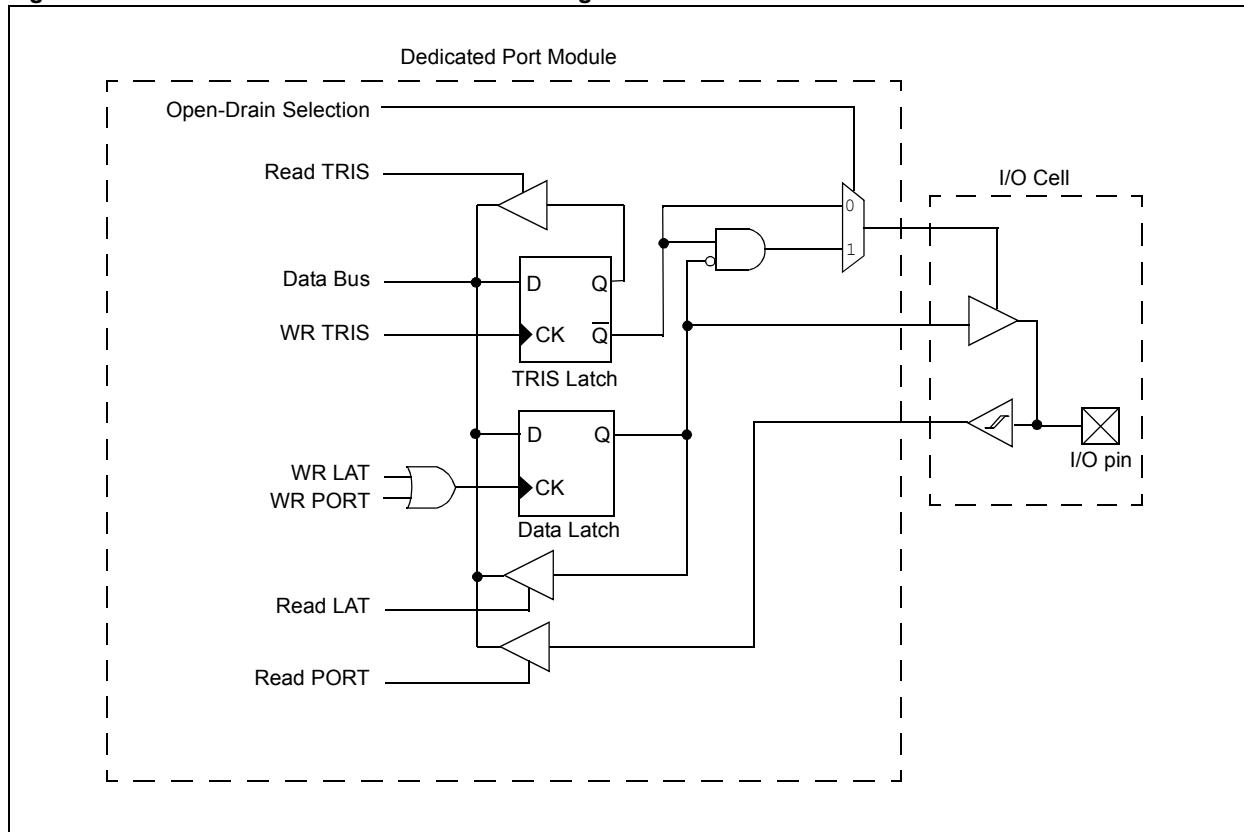
## 12.1 INTRODUCTION

The general purpose I/O pins can be considered the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality to a device, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Most of the PIC24F family devices support the Peripheral Pin Select (PPS) feature. The PPS constitutes pins which users can map to the input and/or output of some digital peripherals.

Figure 12-1 shows a block diagram of a typical I/O port. This block diagram does not take into account peripheral functions that may be multiplexed onto the I/O pin.

**Figure 12-1: Dedicated Port Structure Block Diagram**



## 12.2 I/O PORT CONTROL REGISTERS

All I/O ports have four registers directly associated with the operation of the port, where 'x' is a letter that denotes the particular I/O port:

- TRISx: PORTx Data Direction Control register
- PORTx: I/O Port register
- LATx: PORTx Data Latch register
- ODCx: PORTx Open-Drain Control register

Each I/O pin on the device has an associated bit in the TRIS, PORT, LAT and ODC registers.

**Note:** The total number of ports and available I/O pins will depend on the device variant. In a given device, all of the bits in a PORT register may not be implemented. Refer to the specific device data sheet for further details.

## 12.2.1 TRIS Registers

The TRIS<sub>x</sub> register control bits determine whether each pin associated with the I/O port is an input or an output. If the TRIS bit for an I/O pin is a '1', then the pin is an input. If the TRIS bit for an I/O pin is a '0', then the pin is configured for an output. An easy way to remember this is that a '1' looks like an I (Input) and a '0' looks like an O (Output). All port pins are defined as inputs after a Reset.

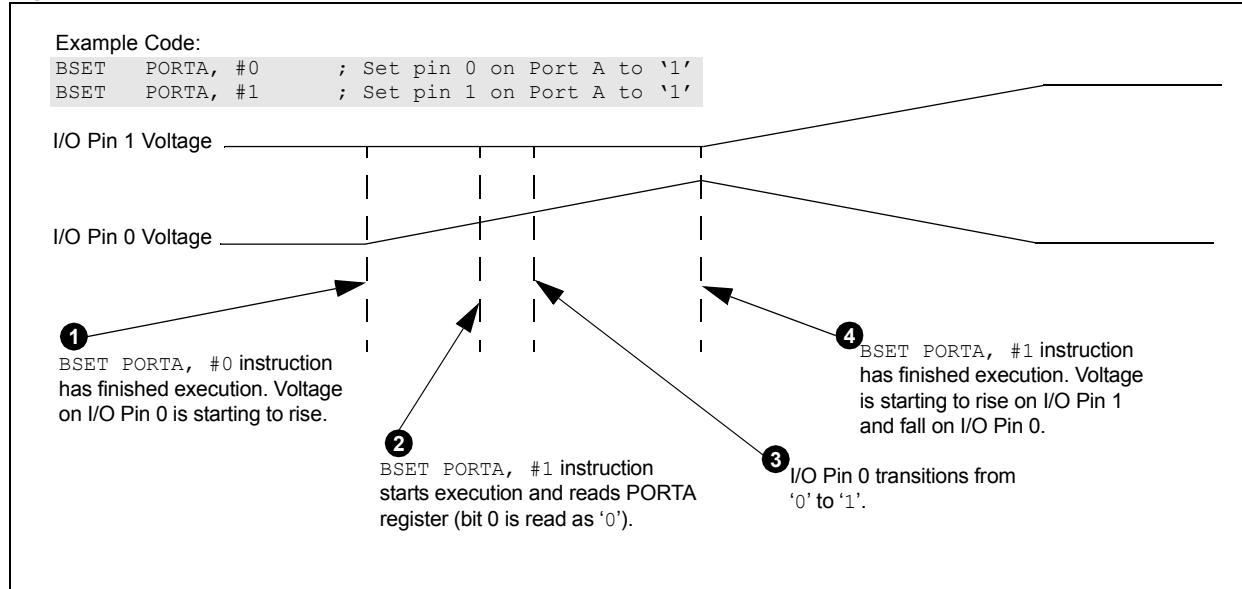
## 12.2.2 PORT Registers

Data on an I/O pin is accessed via a PORT<sub>x</sub> register. A read of the PORT<sub>x</sub> register reads the value of the I/O pin, while a write to the PORT<sub>x</sub> register writes the value to the port data latch. This will also be reflected on the PORT<sub>x</sub> pins if the TRIS<sub>x</sub> is configured as an output and the multiplexed peripherals (if any) are disabled.

Many instructions, such as BSET and BCLR, are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written back to the port data latch. Care should be taken when read-modify-write instructions are used on the PORT<sub>x</sub> registers when some I/O pins associated with the port are configured as inputs. If an I/O pin configured as an input is changed to an output, at some later time, an unexpected value may be output on the I/O pin. To avoid this, first write to the associated PORT<sub>x</sub> bit and then change the direction of the pin as an output.

In addition, if read-modify-write instructions are used on the PORT<sub>x</sub> registers while I/O pins are configured as outputs, unintended I/O behavior may occur based on the device speed and I/O capacitive loading. Figure 12-2 illustrates unintended behavior that occurs if the user application attempts to set I/O bits, 0 and 1, on PORTA, with two consecutive read-modify-write instructions in the PORTA register. At high CPU speeds and high capacitive loading on the I/O pins, the unintended result of the example code is that only I/O bit 1 is set high.

Figure 12-2: Example of Unintended I/O Behavior



### 12.2.3 LAT Registers

The LAT<sub>x</sub> register associated with an I/O pin eliminates the problems that could occur with read-modify-write instructions. A read of the LAT<sub>x</sub> register returns the values held in the port output latches instead of the values on the I/O pins. A read-modify-write operation on the LAT<sub>x</sub> register, associated with an I/O port, avoids the possibility of writing the input pin values into the port latches. A write to the LAT<sub>x</sub> register has the same effect as a write to the PORT<sub>x</sub> register.

The differences between the PORT<sub>x</sub> and LAT<sub>x</sub> registers can be summarized as follows:

- A write to the PORT<sub>x</sub> register writes the data value to the port latch.
- A write to the LAT<sub>x</sub> register writes the data value to the port latch.
- A read of the PORT<sub>x</sub> register reads the data value on the I/O pin.
- A read of the LAT<sub>x</sub> register reads the data value held in the port latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LAT<sub>x</sub> and TRIS<sub>x</sub> registers, and the port pin, will read as zeros.

### 12.2.4 ODC Registers

Each I/O pin can be individually configured for either normal digital output or open-drain output. This is controlled by the PORT<sub>x</sub> Open-Drain Control register, ODC<sub>x</sub>, associated with each I/O pin. If the ODC bit for an I/O pin is '1', then the pin acts as an open-drain output. If the ODC bit for an I/O pin is '0', then the pin is configured for a normal digital output (ODC bit is valid only for output pins). After a Reset, the status of all the bits of the ODC<sub>x</sub> register is set to '0'.

The open-drain feature allows a load to be connected to a voltage higher/lower than V<sub>DD</sub> on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V<sub>IH</sub> specification and the minimum is V<sub>SS</sub>. The ODC<sub>x</sub> register setting takes effect in all the I/O modes, allowing the output to behave as an open-drain even if a peripheral is controlling the pin. Although the user could achieve the same effect by manipulating the corresponding LAT and TRIS bits, this procedure will not allow the peripheral to operate in Open-Drain mode (except for the default operation of the I<sup>2</sup>C™ pins). Since I<sup>2</sup>C pins are already open-drain pins, the ODC<sub>x</sub> settings do not affect the I<sup>2</sup>C pins. Also, the ODC<sub>x</sub> settings do not affect the JTAG output characteristics as the JTAG scan cells are inserted between the ODC<sub>x</sub> logic and the I/O.

**Note:** Please note that the maximum V<sub>IH</sub> spec for the PIC24FXXKXXXX family is limited to V<sub>DD</sub>. This limits open-drain capability for higher voltage generation, though it can still be connected to lower voltage than V<sub>DD</sub>.

# PIC24F Family Reference Manual

## Register 12-1: TRISx: PORTx Data Direction Control Register

|                            |       |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1                      | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| TRISx<15:8> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 15                     |       |       |       |       |       |       | bit 8 |

|                           |       |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1                     | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| TRISx<7:0> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 7                     |       |       |       |       |       |       | bit 0 |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **TRISx<15:0>**: PORTx Data Direction Control bits<sup>(1)</sup>

1 = The pin is an input

0 = The pin is an output

**Note 1:** Refer to the specific device data sheet for the actual implementation.

## Register 12-2: PORTx: I/O Port Register

|                            |       |       |       |       |       |       |
|----------------------------|-------|-------|-------|-------|-------|-------|
| R/W-0                      | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PORTx<15:8> <sup>(1)</sup> |       |       |       |       |       |       |
| bit 15                     |       |       |       |       |       |       |

|                           |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|
| R/W-0                     | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PORTx<7:0> <sup>(1)</sup> |       |       |       |       |       |       |
| bit 7                     |       |       |       |       |       |       |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **PORTx<15:0>**: I/O Port bits<sup>(1)</sup>

1 = The pin data is '1'

0 = The pin data is '0'

**Note 1:** Refer to the specific device data sheet for the actual implementation.

### Register 12-3: LATx: PORTx Data Latch Register

|                           |       |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0                     | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| LATx<15:8> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 15                    |       |       |       |       |       |       | bit 8 |

|                          |       |       |       |       |       |       |       |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0                    | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| LATx<7:0> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 7                    |       |       |       |       |       |       | bit 0 |

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **LATx<15:0>**: PORTx Data Latch bits<sup>(1)</sup>

1 = The latch content is '1'

0 = The latch content is '0'

**Note 1:** Refer to the specific device data sheet for the actual implementation.

### Register 12-4: ODCx: PORTx Open-Drain Control Register

|                           |       |       |       |       |       |       |       |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0                     | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ODCx<15:8> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 15                    |       |       |       |       |       |       | bit 8 |

|                          |       |       |       |       |       |       |       |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0                    | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ODCx<7:0> <sup>(1)</sup> |       |       |       |       |       |       |       |
| bit 7                    |       |       |       |       |       |       | bit 0 |

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **ODCx<15:0>**: PORTx Open-Drain Control bits<sup>(1)</sup>

1 = The pin acts as an open-drain output pin if TRISx is '0'

0 = The pin acts as a normal pin

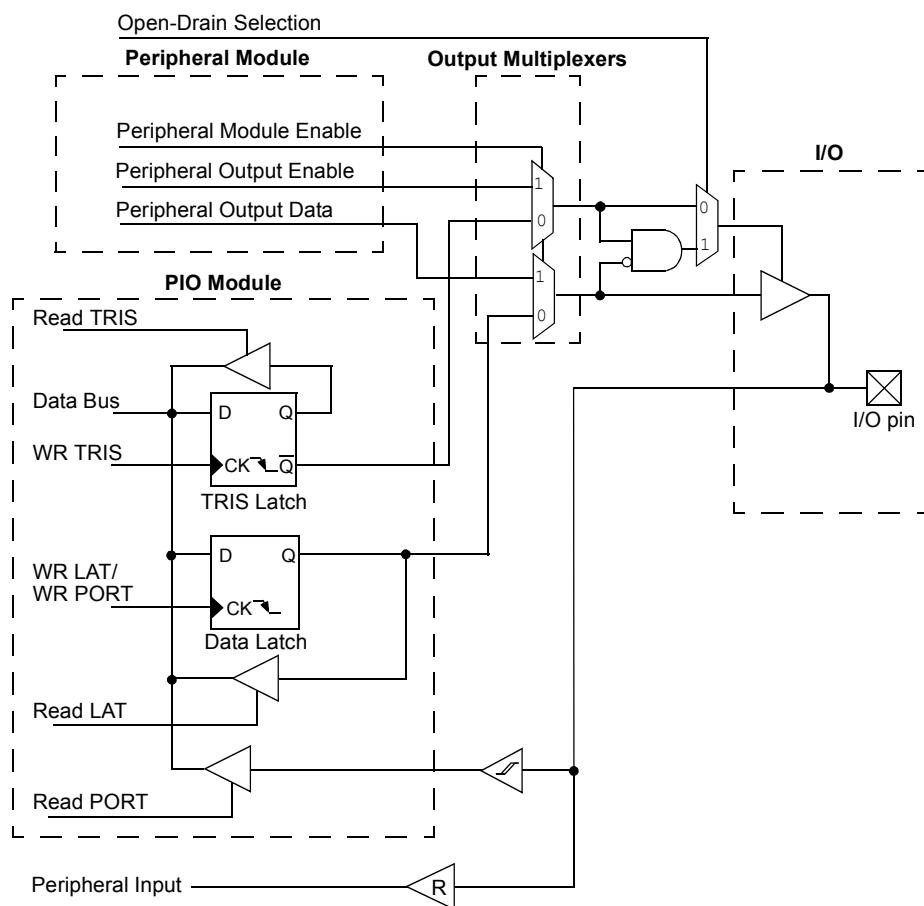
**Note 1:** Refer to the specific device data sheet for the actual implementation.

## 12.3 PERIPHERAL MULTIPLEXING

Pins can also be configured as digital inputs or outputs, and analog inputs or outputs. When configured as digital inputs, they are either TTL buffers or Schmitt Triggers. When configured as digital outputs, they are either CMOS drivers or open-drain outputs.

Many pins also support one or more peripheral modules. When configured to operate with a peripheral, a pin may not be used for general input or output. In many cases, a pin must still be configured for input or output, although some peripherals override the TRIS configuration. Figure 12-3 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected. For some PIC24F devices, multiple peripheral functions may be multiplexed on each I/O pin. The priority of the peripheral function depends on the order of the pin description in the pin diagram of the specific product data sheet.

**Figure 12-3:** Structure of Port Shared with Non-PPS Peripherals



### 12.3.1 Multiplexing Digital Input Peripheral

- Peripheral does not control the TRIS<sub>x</sub> register. The TRIS bits should be maintained for input.
- PORT<sub>x</sub> data input path is unaffected. On reading the PORT<sub>x</sub> register, the status of the pin will be read.
- Peripheral input path is independent of I/O input path with a special input buffer.

### 12.3.2 Multiplexing Digital Output Peripheral

- Peripheral controls output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type is selected by peripheral (e.g., drive strength, slow rate, etc.).
- User needs to configure the pin as an output by clearing the associated TRISx bit.
- If an output has an automatic tri-state feature (e.g., PWM outputs), the peripheral has the ability to tri-state the pin.

### 12.3.3 Multiplexing Digital Bidirectional Peripheral

- Peripheral can automatically configure the pin as an output but not as an input. User needs to configure the pin as an input by setting the associated TRISx bit.
- Peripherals control output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type could be affected by peripheral (e.g., drive strength, slow rate, etc.).

### 12.3.4 Multiplexing Analog Input Peripheral

- All digital port input buffers are disabled and PORTx registers read ‘0’ to prevent crowbar current.

### 12.3.5 Multiplexing Analog Output Peripheral

- All digital port input buffers are disabled and PORTx registers read ‘0’ to prevent crowbar current.
- Analog output is driven onto the pin independent of the associated TRISx setting.

**Note:** In order to use pins multiplexed with the A/D for digital I/O, the corresponding bits in the AD1PCFG register must be set to ‘1’, even if the A/D module is turned off.

### 12.3.6 Software Input Pin Control

Some of the functions assigned to an I/O pin may be input functions that do not take control of the pin output driver. An example of one such peripheral is the input capture module. If the I/O pin associated with the input capture is configured as an output, using the appropriate TRIS control bit, the user can manually affect the state of the input capture pin through its corresponding PORT register. This behavior can be useful in some situations, especially for testing purposes, when no external signal is connected to the input pin.

Referring to Figure 12-3, the organization of the peripheral multiplexers will determine if the peripheral input pin can be manipulated in software using the PORT register. The conceptual peripherals shown in this figure disconnect the port data from the I/O pin when the peripheral function is enabled.

In general, the following peripherals allow their input pins to be controlled manually through the PORT registers:

- External Interrupt pins
- Timer Clock Input pins
- Input Capture pins
- PWM Fault pins

Most serial communication peripherals, when enabled, take full control of the I/O pin so that the input pins associated with the peripheral cannot be affected through the corresponding PORT registers. These peripherals include the following:

- SPI
- I<sup>2</sup>C™
- UART

## 12.4 PERIPHERAL PIN SELECT

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral is needed to be assigned to a single pin, inconvenient work arounds in application code or a complete redesign may be the only option.

Peripheral pin select configuration provides an alternative to these choices by enabling users peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral pin select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

**Note:** Some devices do not have this feature. Please refer to the specific device data sheet for more details.

### 12.4.1 Available Pins

The peripheral pin select feature is used with a range of pins. The number of available pins is dependent on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation, "RPn", in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number. If the [REDACTED] function peripheral pin select feature, then it [REDACTED]. For more details, refer to the device pinout in the respective device data sheet.

### 12.4.2 Available Peripherals

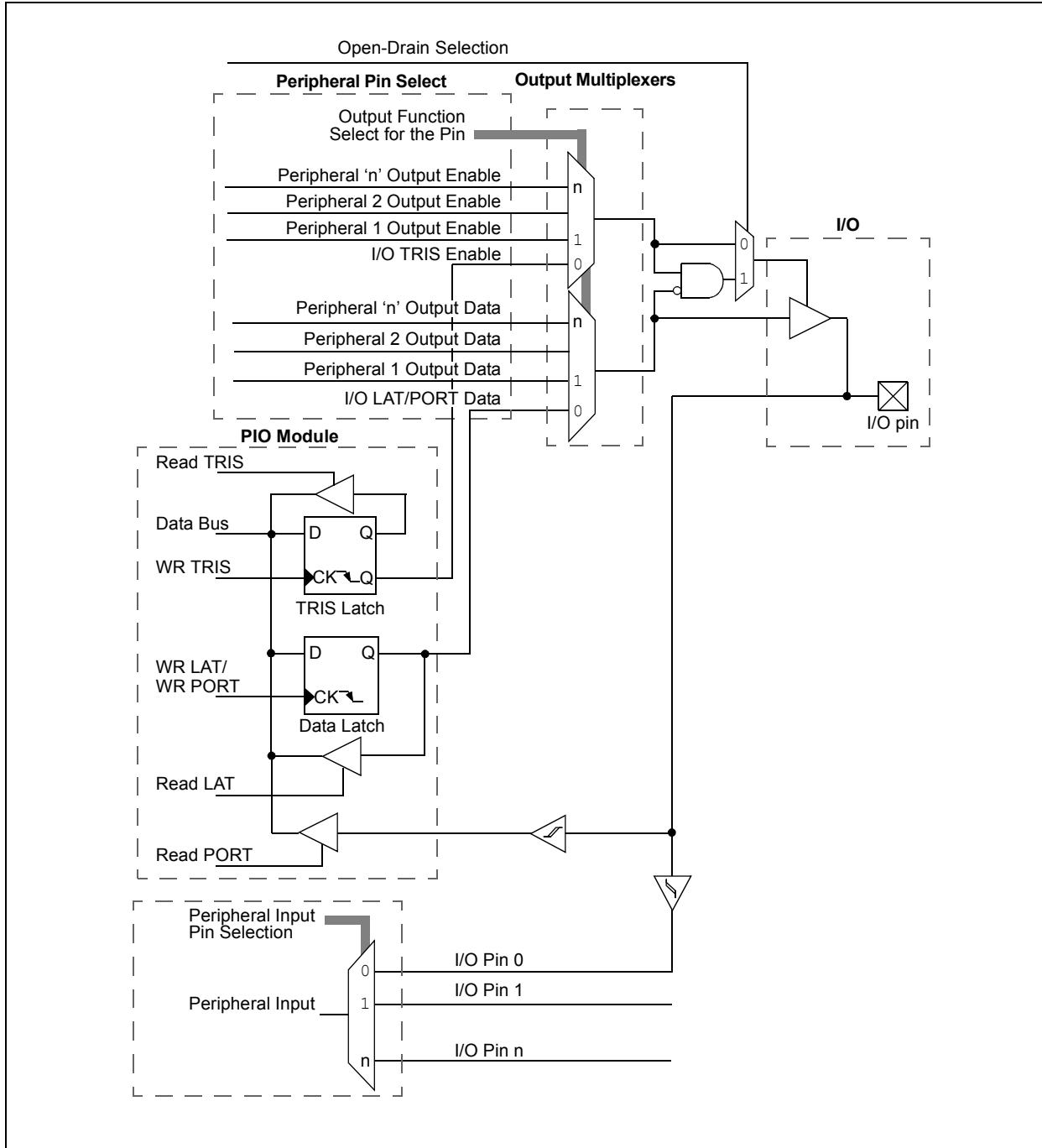
The peripherals managed by the peripheral pin select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs.

In comparison, some digital only peripheral modules are not currently included in the peripheral pin select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C, speciality communication (Ethernet and USB), change notification inputs, RTCC alarm output and all modules with analog inputs, such as the A/D Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped.

Figure 12-4: Structure of Port Shared with PPS Peripherals



## 12.4.3 Controlling Peripheral Pin Select

Peripheral pin select features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map peripheral outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways depending if an input or output is being mapped.

### 12.4.3.1 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral; that is, a bit field associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (refer to Register 12-1 and Table 12-1) contain sets of 6-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an R<sub>n</sub> value maps the R<sub>n</sub> pin to that peripheral. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of peripheral pin selections supported by the device.

The peripheral inputs that support peripheral pin selection have no default pins. Since the implemented bit fields of RPINRx registers reset to all '1's, the inputs are all tied to V<sub>ss</sub> in the device's default (Reset) state.

For example, assigning RPINR18<5:0> to 0x2 selects RP2 as the U1RX input. Figure 12-5 illustrates remappable pin selection for the U1RX input.

Figure 12-5: Remappable Input for U1RX

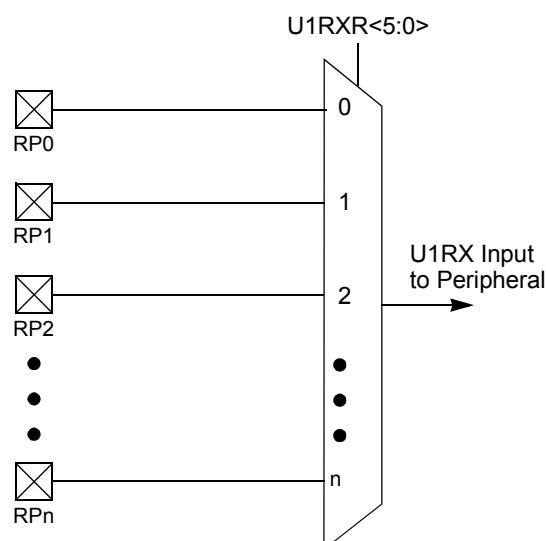


Table 12-1: Selectable Input Sources (Maps Input to Function)

| Input Name <sup>(1)</sup> | Function Name | Register Bits | Configuration Bits |
|---------------------------|---------------|---------------|--------------------|
| External Interrupt 1      | INT1          | RPINR0<13:8>  | INT1R<5:0>         |
| External Interrupt 2      | INT2          | RPINR1<5:0>   | INT2R<5:0>         |
| External Interrupt 3      | INT3          | RPINR1<13:8>  | INT3R<5:0>         |
| External Interrupt 4      | INT4          | RPINR2<5:0>   | INT4R<5:0>         |
| Timer2 External Clock     | T2CK          | RPINR3<5:0>   | T2CKR<5:0>         |
| Timer3 External Clock     | T3CK          | RPINR3<13:8>  | T3CKR<5:0>         |
| Timer4 External Clock     | T4CK          | RPINR4<5:0>   | T4CKR<5:0>         |
| Timer5 External Clock     | T5CK          | RPINR4<13:8>  | T5CKR<5:0>         |
| Input Capture 1           | IC1           | RPINR7<5:0>   | IC1R<5:0>          |
| Input Capture 2           | IC2           | RPINR7<13:8>  | IC2R<5:0>          |
| Input Capture 3           | IC3           | RPINR8<5:0>   | IC3R<5:0>          |
| Input Capture 4           | IC4           | RPINR8<13:8>  | IC4R<5:0>          |
| Input Capture 5           | IC5           | RPINR9<5:0>   | IC5R<5:0>          |
| Output Compare Fault A    | OCFA          | RPINR11<5:0>  | OCFAR<5:0>         |
| Output Compare Fault B    | OCFB          | RPINR11<13:8> | OCFBR<5:0>         |
| UART1 Receive             | U1RX          | RPINR18<5:0>  | U1RXR<5:0>         |
| UART1 Clear To Send       | U1CTS         | RPINR18<13:8> | U1CTSR<5:0>        |
| UART2 Receive             | U2RX          | RPINR19<5:0>  | U2RXR<5:0>         |
| UART2 Clear To Send       | U2CTS         | RPINR19<13:8> | U2CTSR<5:0>        |
| SPI1 Data Input           | SDI1          | RPINR20<5:0>  | SDI1R<5:0>         |
| SPI1 Clock Input          | SCK1          | RPINR20<13:8> | SCK1R<5:0>         |
| SPI1 Slave Select Input   | SS1           | RPINR21<5:0>  | SS1R<5:0>          |
| SPI2 Data Input           | SDI2          | RPINR22<5:0>  | SDI2R<5:0>         |
| SPI2 Clock Input          | SCK2          | RPINR22<13:8> | SCK2R<5:0>         |
| SPI2 Slave Select Input   | SS2           | RPINR23<5:0>  | SS2R<5:0>          |

**Note 1:** The device may have more or less number of input functions. For actual details, please refer to the specific device data sheet.

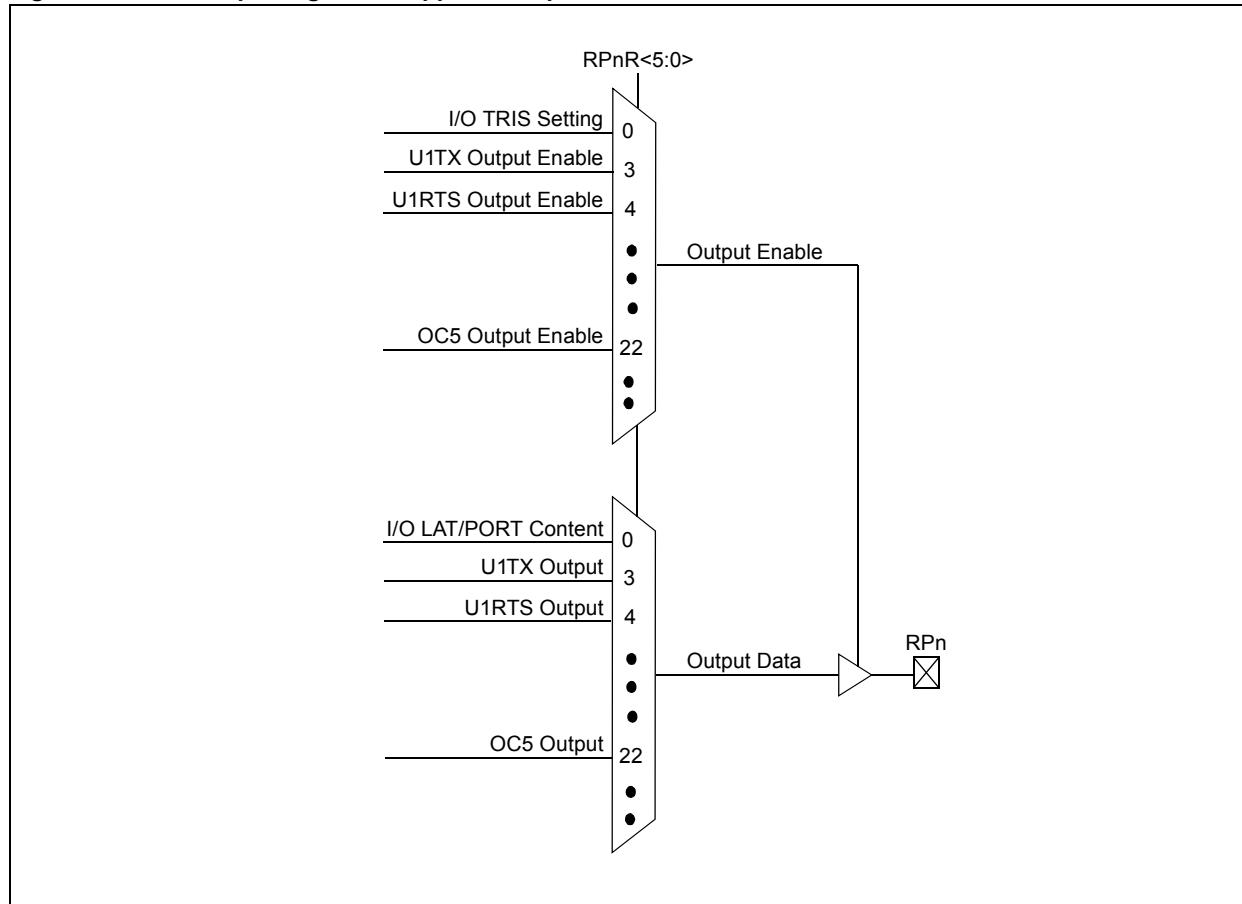
## 12.4.3.2 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a bit field associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers contain sets of 6-bit fields, with each set associated with one RPn pin (see Register 12-2). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-5).

The peripheral outputs that support peripheral pin selection have no default pins. Since the RPORx registers reset to all '0's, the outputs are all disconnected in the device's default (Reset) state.

The list of peripherals for output mapping also includes a null value of '000000' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin-selectable peripherals.

**Figure 12-6: Multiplexing of Remappable Output for RPn**



**Table 12-2: Output Selection for Remappable Pin (RPn)**

| Function <sup>(1)</sup> | RPnR<5:0> | Output Name                           |
|-------------------------|-----------|---------------------------------------|
| NULL                    | 0         | The pin is an I/O Port pin.           |
| C1OUT                   | 1         | RPn tied to Comparator 1 Output.      |
| C2OUT                   | 2         | RPn tied to Comparator 2 Output.      |
| U1TX                    | 3         | RPn tied to UART1 Transmit.           |
| U1RTS                   | 4         | RPn tied to UART1 Ready To Send.      |
| U2TX                    | 5         | RPn tied to UART2 Transmit.           |
| U2RTS                   | 6         | RPn tied to UART2 Ready To Send.      |
| SDO1                    | 7         | RPn tied to SPI1 Data Output.         |
| SCK1OUT                 | 8         | RPn tied to SPI1 Clock Output.        |
| SS1OUT                  | 9         | RPn tied to SPI1 Slave Select Output. |
| SDO2                    | 10        | RPn tied to SPI2 Data Output.         |
| SCK2OUT                 | 11        | RPn tied to SPI2 Clock Output.        |
| SS2OUT                  | 12        | RPn tied to SPI2 Slave Select Output. |
| OC1                     | 18        | RPn tied to Output Compare 1.         |
| OC2                     | 19        | RPn tied to Output Compare 2.         |
| OC3                     | 20        | RPn tied to Output Compare 3.         |
| OC4                     | 21        | RPn tied to Output Compare 4.         |
| OC5                     | 22        | RPn tied to Output Compare 5.         |

**Note 1:** The device may have more or less number of output functions. For actual details, please refer to the specific device data sheet.

**Table 12-3: Registers Associated with Output Function on RPn pin**

| Pin     | Register     | Associated bits |
|---------|--------------|-----------------|
| RP0     | RPO0<5:0>    | RP0R<5:0>       |
| RP1     | RPO0<13:8>   | RP1R<5:0>       |
| RP2     | RPO1<5:0>    | RP2R<5:0>       |
| RPn     | RPOn/2<5:0>  | RPnR<5:0>       |
| RPn + 1 | RPOn/2<13:8> | RPn + 1R<5:0>   |

**Legend:** n = 0, 2, 4, . . . , etc.

#### 12.4.3.3 MAPPING LIMITATIONS

The control schema of peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware enforced lockouts between any of the peripheral mapping SFRs; literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, the user must ensure the selected configurations are supportable from an electrical point of view.

#### 12.4.4 Controlling Configuration Changes

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit remapping lock

## 12.4.4.1 CONTROL REGISTER LOCK

Under normal operation, writes to the RPINRx and RPORx registers are not allowed; attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 46h to OSCCON<7:0>.
2. Write 57h to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

The unlock/lock sequence must be executed as an assembly language routine in the same manner as changes to the oscillator configuration because the unlock sequence is timing critical. If the bulk of the application is written in C, or another high-level language, the unlock sequence should be performed by writing inline assembly or using built-in functions provided by the MPLAB® C30 C Complier.

IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

**Note:** MPLAB® C30 C Compiler provides built-in C language functions for unlocking the OSCCON register:  
`__builtin_write_OSCCONL(value)`  
`__builtin_write_OSCCONH(value)`

See “*MPLAB C30 C Compiler User’s Guide*” for more information.

## 12.4.4.2 CONTINUOUS STATE MONITORING

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset will be triggered.

## 12.4.4.3 CONFIGURATION BIT PIN SELECT LOCK

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<IOL1WAY>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows users unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

## 12.4.5 Considerations for Peripheral Pin Selection

The ability to control peripheral pin selection introduces several considerations into application design that should be considered. This is particularly true for several common peripherals which are only available as remappable peripherals.

Before any other application code is executed, the user must initialize the device with the proper peripheral configuration. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For the sake of application safety, however, it is always a good idea to set IOLOCK and lock the configuration after writing to the control registers.

Choosing the configuration requires the review of all peripheral pin selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled. Unused peripherals should have their inputs assigned to Vss. I/O pins with unused RPn functions should be configured with the NULL ('0') peripheral output.

The assignment of a RPn pin to the peripheral input or output depends on the peripheral and its use in the application. It is better to be done immediately following device Reset and before the peripheral configuration.

The assignment of a peripheral output to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. This means adding a pin selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that share a remappable pin. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Configuring a remappable pin for a specific peripheral input does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled, as if it were tied to a fixed pin.

A final consideration is that peripheral pin select functions neither override analog inputs, nor reconfigure pins with analog functions for digital I/O. If a pin is configured as an analog input on device Reset, it must be explicitly reconfigured as digital I/O when used with a peripheral pin select.

### 12.4.5.1 BASIC STEPS TO USE PERIPHERAL PIN SELECTION (PPS)

1. Disable any fixed digital peripherals on the pins to be used.
2. Switch pins to be used for digital functionality (if they have analog functionality) using the ADxPCFG register.
3. Unlock the OSCCON register and clear bit, IOLOCK (not needed after device Reset).
4. Set RPINRx and RPORx registers appropriately.
5. Unlock the OSCCON register and set bit, IOLOCK, to '1'.
6. Configure and enable newly mapped PPS peripherals.

Example 12-1 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, U1CTS
- Output Functions: U1TX, U1RTS

## Example 12-1: Configuring UART1 Input and Output Functions

```
/*
// Unlock Registers
// *****
__builtin_write_OSCCONL(OSCCON & 0xbf)      //clear the bit 6 of OSCCONL to
//unlock Pin Re-map
// *****
//This code is used when interested in inline assembly. If this code is
//used then the above two lines should not be used for unlocking.
// *****
/*
asm volatile  ( "push    w1          \n"
                "push    w2          \n"
                "push    w3          \n"
                "mov     #OSCCON, w1  \n"
                "mov     #0x46, w2    \n"
                "mov     #0x57, w3    \n"
                "mov.b   w2, [w1]     \n"
                "mov.b   w3, [w1]     \n"
                "bclr   OSCCON, #6   \n"
                "pop    w3          \n"
                "pop    w2          \n"
                "pop    w1");         \n"
/*
// *****
// Configure Input Functions
// *****
// *****
// Assign U1Rx To Pin RP0
// *****
RPINR18bits.U1RXR = 0;                      // '0' represents RP0

// *****
// Assign U1CTS To Pin RP1
// *****
RPINR18bits.U1CTSR = 1;                     // '1' represents RP1

// *****
// Configure Output Functions
// *****
// *****
// Assign U1Tx To Pin RP2
// *****
RPOR1bits.RP2R = 3;                         // '3' represents U1TX

// *****
// Assign U1RTS To Pin RP3
// *****
RPOR1bits.RP3R = 4;                         // '4' represents U1RTS

// *****
// Lock Registers
// *****
__builtin_write_OSCCONL(OSCCON | 0x40)        //set the bit 6 of OSCCONL to
//lock Pin Re-map
// *****
//This code is used when interested in inline assembly. If this code is
//used then the above two lines should not be used for unlocking.
// *****
/*
asm volatile  ( "push    w1          \n"
                "push    w2          \n"
                "push    w3          \n"
                "mov     #OSCCON, w1  \n"
                "mov     #0x46, w2    \n"
                "mov     #0x57, w3    \n"
                "mov.b   w2, [w1]     \n"
                "mov.b   w3, [w1]     \n"
                "bset   OSCCON, #6   \n"
                "pop    w3          \n"
                "pop    w2          \n"
                "pop    w1";           \n"
/*
*/
```

#### 12.4.6 Peripheral Pin Select Registers

These registers are used to configure input and output functionality of the PIC24F device pins.

- **RPINRx:** Peripheral Pin Select Input Register x
- **RPORy:** Peripheral Pin Select Output Register y

**Register 12-5: RPINRx: Peripheral Pin Select Input Register x<sup>(2)</sup>**

| U-0    | U-0 | U-0 | R/W-0                                   | R/W-0 | R/W-0 | R/W-0 | R/W-0 |  |  |
|--------|-----|-----|---|-------|-------|-------|-------|--|--|
| —      | —   |     | Input Function bits<5:0> <sup>(1)</sup> |       |       |       |       |  |  |
| bit 15 |     |     |   |       |       |       | bit 8 |  |  |

| U-0   | U-0 | U-0 | U-0                                     | U-0 | U-0 | U-0 | U-0   |  |  |
|-------|-----|-----|---|-----|-----|-----|-------|--|--|
| —     | —   |     | Input Function bits<5:0> <sup>(1)</sup> |     |     |     |       |  |  |
| bit 7 |     |     |   |     |     |     | bit 0 |  |  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'

bit 13-8      **Input Function Bits<5:0>:** Assign Peripheral to Corresponding RPn Pin bits<sup>(1)</sup>

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **Input Function Bits<5:0>** Assign Peripheral to Corresponding RPn Pin bits<sup>(1)</sup>

**Note 1:** Here, 'n' represents the peripheral select input pin number.

**2:** Here, 'x' represents the Peripheral Pin Select Input register number and it varies from device to device.

**Register 12-6: RPORy: Peripheral Pin Select Output Register y<sup>(2)</sup>**

| U-0    | U-0 | U-0 | R/W-0                    | R/W-0 | R/W-0 | R/W-0 | R/W-0 |  |  |
|--------|-----|-----|--------------------------|-------|-------|-------|-------|--|--|
| —      | —   |     | RPnR<5:0> <sup>(1)</sup> |       |       |       |       |  |  |
| bit 15 |     |     |                          |       |       |       | bit 8 |  |  |

| U-0   | U-0 | U-0 | R/W-0                    | R/W-0 | R/W-0 | R/W-0 | R/W-0 |  |  |
|-------|-----|-----|--------------------------|-------|-------|-------|-------|--|--|
| —     | —   |     | RPnR<5:0> <sup>(1)</sup> |       |       |       |       |  |  |
| bit 7 |     |     |                          |       |       |       | bit 0 |  |  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'

bit 13-8      **RPnR<5:0>:** Peripheral Output Function is Assigned to RPn Pin bits<sup>(1)</sup>  
(see Table 12-2 for peripheral function numbers)

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **RPnR<5:0>:** Peripheral Output Function is Assigned to RPn Pin bits<sup>(1)</sup>  
(see Table 12-2 for peripheral function numbers)

**Note 1:** Here, 'n' represents the peripheral pin select output pin number.

**2:** Here, 'y' represents the Peripheral Pin Select Output register number and it varies from device to device.

## 12.5 PORT DESCRIPTIONS

Refer to the specific device data sheet for a description of the available I/O ports, peripheral multiplexing details and available peripheral pin select pins.

## 12.6 CHANGE NOTIFICATION (CN) PINS

The Change Notification (CN) pins provide PIC24F devices the ability to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. The total number of available CN inputs is dependent on the selected PIC24F device. Refer to the specific device data sheet for further details.

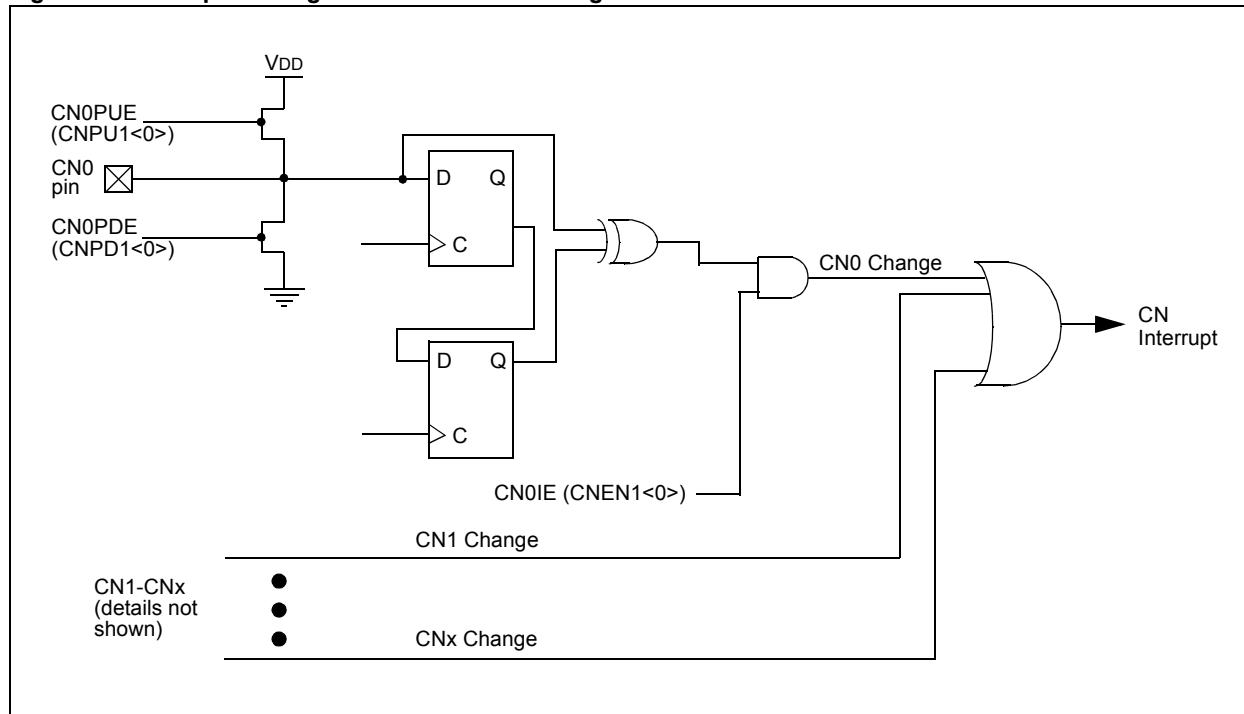
Figure 12-7 shows the basic function of the CN hardware.

### 12.6.1 CN Control Registers

There are four control registers associated with the CN module. The CNENx registers contain the CNxIE control bits, where 'x' denotes the number of the CN input pin. The CNxIE bit must be set for a CN input pin to interrupt the CPU.

The CNPUx/CNPDX registers contain the CNxPUE/CNxPDE control bits. Each CN pin has a weak pull-up/pull-down device connected to the pin which can be enabled or disabled using the CNxPUE/CNxPDE control bits. The weak pull-up/pull-down devices act as a current source/sink that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. Refer to the “**Electrical Characteristics**” section of the specific device data sheet for CN pull-up/pull-down device current specifications.

Figure 12-7: Input Change Notification Block Diagram



## 12.6.2 CN Configuration and Operation

The CN pins are configured as follows:

1. Ensure that the CN pin is configured as a digital input by setting the associated bit in the TRISx register.
2. Enable interrupts for the selected CN pins by setting the appropriate bits in the CNENx registers.
3. Turn on the weak pull-up devices (if desired) for the selected CN pins by setting the appropriate bits in the CNPUx registers.
4. Clear the CNxF interrupt flag.
5. Select the desired interrupt priority for CN interrupts using the CNxIP<2:0> control bits.
6. Enable CN interrupts using the CNxE control bit.

When a CN interrupt occurs, the user should read the PORT register associated with the CN pin(s). This will clear the mismatch condition and set up the CN logic to detect the next pin change. The current PORT value can be compared to the PORT read value obtained at the last CN interrupt to determine the pin that changed.

The CN pins have a minimum input pulse-width specification. Refer to the “**Electrical Characteristics**” section of the specific device data sheet for further details.

## 12.6.3 CN Operation in Sleep and Idle Modes

The CN module continues to operate during Sleep or Idle mode. If one of the enabled CN pins changes states, the CNxF status bit will be set. If the CNxE bit is set, the device will wake from Sleep or Idle mode and resume operation.

If the assigned priority level of the CN interrupt is equal to, or less than, the current CPU priority level, device execution will continue from the instruction immediately following the `SLEEP` or `IDLE` instruction.

If the assigned priority level of the CN interrupt is greater than the current CPU priority level, device execution will continue from the CN interrupt vector address.

## 12.7 REGISTER MAPS

A summary of the registers associated with the PIC24F I/O ports is provided in Table 12-4, Table 12-5 and Table 12-6.

**Table 12-4: Special Function Registers Associated with I/O Ports<sup>(1)</sup>**

| Name  | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------------|
| TRISx |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| LATx  |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| PORTx |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| ODCx  |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |

**Note 1:** Refer to the specific device data sheet for the I/O Ports register map details.

**Table 12-5: Special Function Registers Associated with Peripheral Pin Selection<sup>(1)</sup>**

| Name   | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------------|
| RPINRx |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| RPORy  |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |

**Note 1:** Refer to the specific device data sheet for Peripheral Pin Select register map details.

**Note 2:** The number of bits implemented varies with the number of pins the device has.

**Table 12-6: Special Function Registers Associated with Change Notification Pins<sup>(1)</sup>**

| Name  | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------------|
| CNENx |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| CNPUX |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |
| CNPDX |        |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |            |

**Note 1:** Refer to the specific device data sheet for Change Notification Pin register details.

## 12.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the I/O Ports with Peripheral Pin Select (PPS) are:

| Title                              | Application Note # |
|------------------------------------|--------------------|
| Implementing Wake-up on Key Stroke | AN552              |

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC24F family of devices.

## 12.9 REVISION HISTORY

### **Revision A (August 2006)**

This is the initial released revision of this document.

### **Revision B (May 2007)**

Added PPS section, removed JTAG boundary scan section and added PPS SFR table.

**NOTES:**

**12**

**I/O Ports**