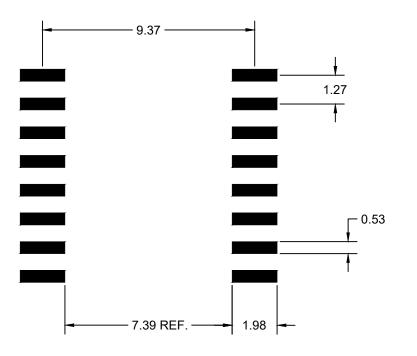
### RECOMMENDED LAND PATTERN



# PACKAGE OVERLAY

| PKG. CODES  |
|-------------|
| DM40 - 41   |
| [W16+1]     |
| [W16+2]     |
| [W16+3]     |
| [W16+4F]    |
| [W16+6]     |
| [W16+7]     |
| [W16+10]    |
| [W16+11]    |
| [W16+12]    |
| [W16+H2]    |
| [W16M+3]    |
| [W16M+6]    |
| [W16MK+1]   |
| [W16M+8]    |
| [W16M+9]    |
| [W16M+10]   |
| [W16MS+11]  |
| [W16MS+12]  |
| [W16MS+12C] |
| [W16MS+13]  |
| [W16MS+13C] |
| [W16MS+14]  |
|             |

#### NOTES:

- REFERENCE PKG. DUTLINE: 21-0042
- 2. LAND PATTERN COMPLIES TO: IPC7351A.
- TOLERANCE: +/- 0.02 MM.
- 4. ALL DIMENSIONS APPLY TO PHFREE (+) PKG, CODE ONLY.
- 5. ALL DIMENSIONS IN MM.

### -DRAWING NOT TO SCALE-

This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice. Contact technical support at http://www.maxim-ic.com/support for further questions.



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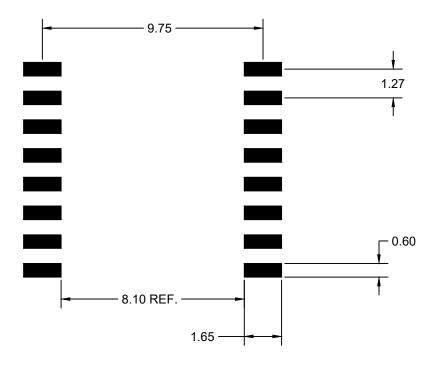
PACKAGE LAND PATTERN, [W16] 0.300" SOIC, 16 LEADS

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90-0107

REV.

# OPTION FOR IMPROVED HV ISOLATION ( CLEARANCE/CREEPAGE OF 8.1MM )



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PACKAGE LAND PATTERN, [W16] 0.300" SOIC, 16 LEADS

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