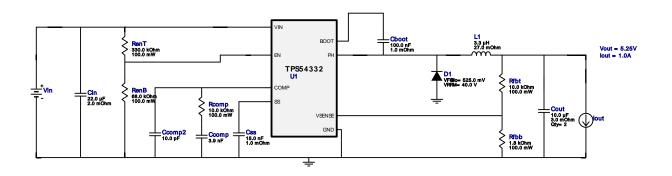


VinMin = 11.5V VinMax = 12.5V Vout = 5.25V Iout = 1.0A Device = TPS54332DDAR Topology = Buck Created = 2020-08-25 13:11:51.595 BOM Cost = \$1.85 BOM Count = 15 Total Pd = 0.43W

# WEBENCH® Design Report

Design: 1 TPS54332DDAR TPS54332DDAR 11.5V-12.5V to 5.25V @ 1.5A

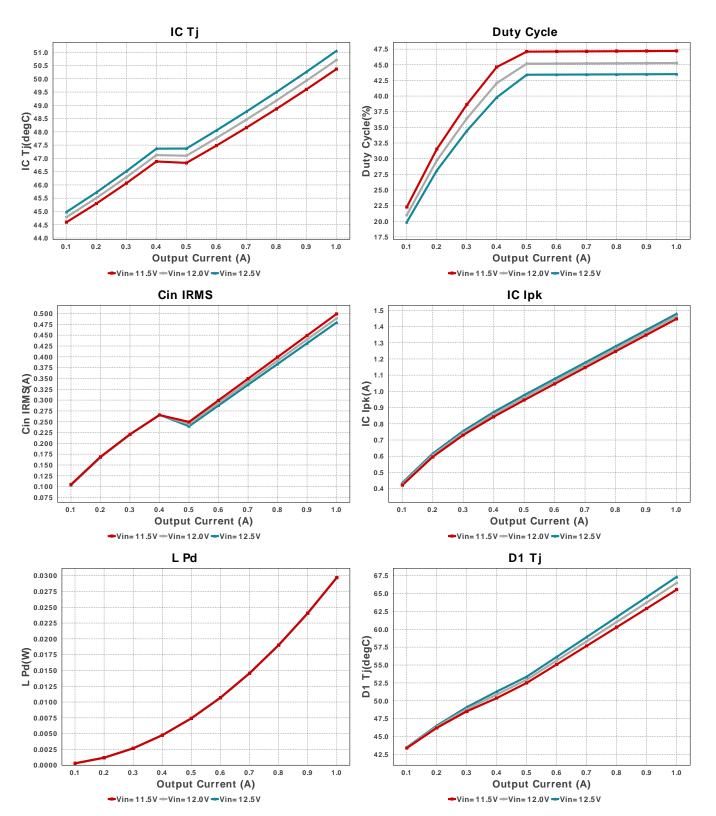


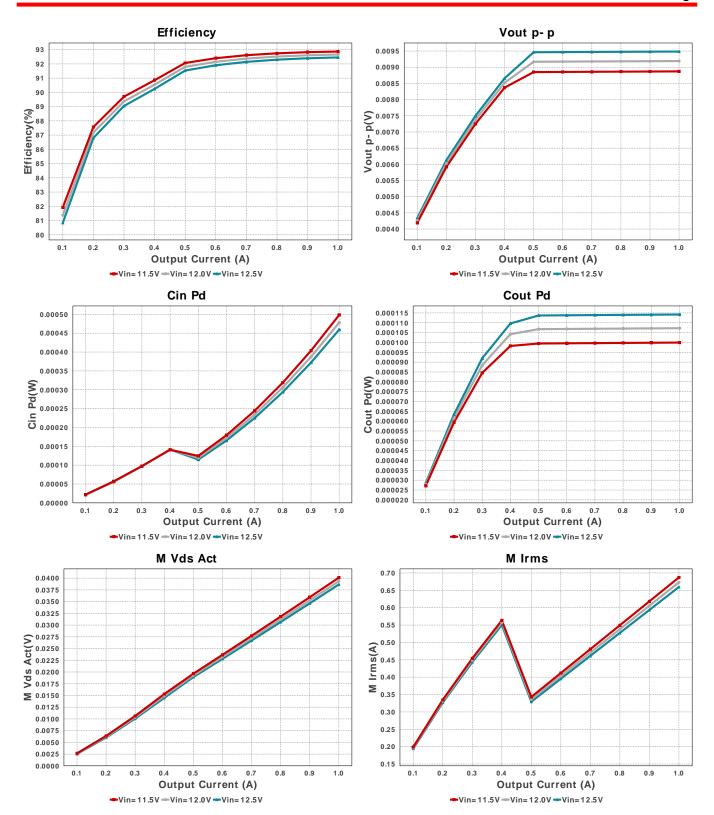
#### **Electrical BOM**

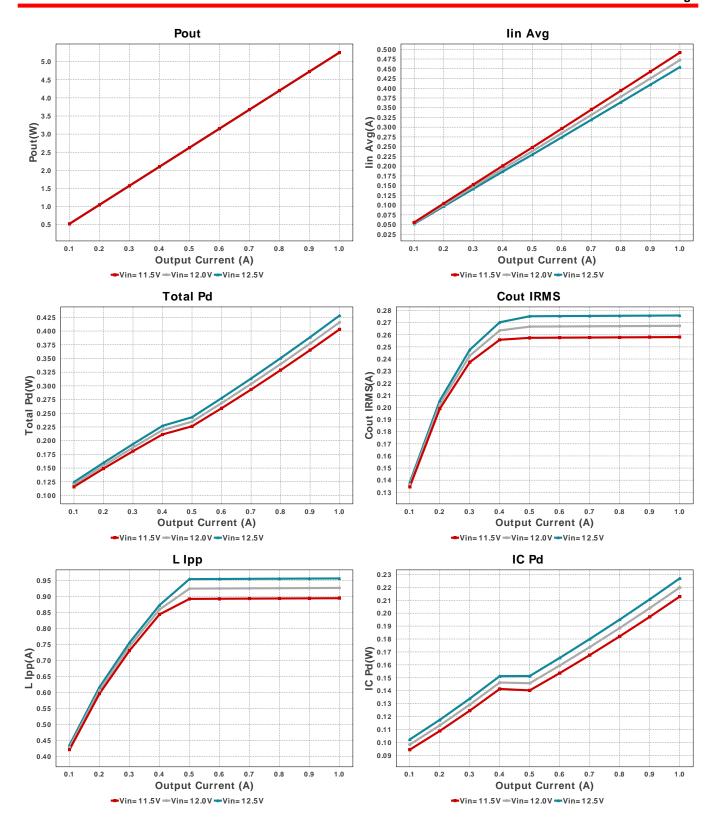
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cboot	MuRata	GRM155R71A104KA01D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	\$0.01	0402 3 mm <sup>2</sup>
Ccomp	TDK	CGA4C2C0G1H392J060AA Series= C0G/NP0	Cap= 3.9 nF VDC= 50.0 V IRMS= 0.0 A	1	\$0.04	0805 7 mm <sup>2</sup>
Ccomp2	Samsung Electro- Mechanics	CL21C100JBANNNC Series= C0G/NP0	Cap= 10.0 pF VDC= 50.0 V IRMS= 0.0 A	1	\$0.01	0805 7 mm <sup>2</sup>
Cin	MuRata	GRM32ER61E226KE15L Series= X5R	Cap= 22.0 uF ESR= 2.0 mOhm VDC= 25.0 V IRMS= 3.67 A	1	\$0.65	1210 15 mm <sup>2</sup>
Cout	Kemet	C0805C106K8PACTU Series= X5R	Cap= 10.0 uF ESR= 3.0 mOhm VDC= 10.0 V IRMS= 11.43 A	2	\$0.03	0805 7 mm <sup>2</sup>
Css	MuRata	GRM155R71C153KA01D Series= X7R	Cap= 15.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	\$0.01	0402 3 mm <sup>2</sup>
D1	ON Semiconductor	MBRS340T3G	VF@Io= 525.0 mV VRRM= 40.0 V	1	\$0.13	SMC 83 mm <sup>2</sup>
L1	Bourns	SRR7032-3R3M	L= 3.3 μH 27.0 mOhm	1	\$0.32	SRR7032 81 mm <sup>2</sup>
Rcomp	Yageo	RC0603FR-0710KL Series= ?	Res= 10.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm <sup>2</sup>
RenB	Yageo	RC0603FR-0768KL Series= ?	Res= 68.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm <sup>2</sup>
RenT	Yageo	RC0603FR-07330KL Series=?	Res= 330.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm <sup>2</sup>

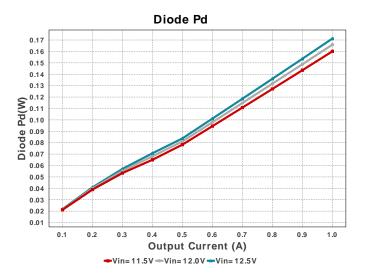
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Rfbb	Yageo	RC0603FR-071K8L Series= ?	Res= 1.8 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm <sup>2</sup>
Rfbt	Yageo	RC0603FR-0710KL Series=?	Res= 10.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm <sup>2</sup>
U1	Texas Instruments	TPS54332DDAR	Switcher	1	\$0.57	

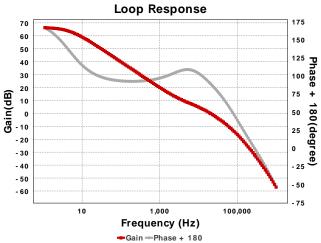












## **Operating Values**

#	Name	Value	Category	Description
1.	BOM Count	15		Total Design BOM count
2.	Total BOM	\$1.852		Total BOM Cost
3.	Cin IRMS	479.263 mA	Capacitor	Input capacitor RMS ripple current
4.	Cin Pd	459.39 μW	Capacitor	Input capacitor power dissipation
5.	Cout IRMS	275.912 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	114.19 μW	Capacitor	Output capacitor power dissipation
7.	D1 Tj	67.337 degC	Diode	D1 junction temperature
8.	Diode Pd	171.28 mW	Diode	Diode power dissipation
9.	IC lpk	1.478 A	IC	Peak switch current in IC
10.	IC Pd	226.87 mW	IC	IC power dissipation
11.		51.049 degC	IC	IC junction temperature
12.	ICThetaJA	48.7 degC/W	IC	IC junction-to-ambient thermal resistance
13.	lin Avg	454.27 mA	IC	Average input current
	L lpp	955.788 mA	Inductor	Peak-to-peak inductor ripple current
	L Pd	29.7 mW	Inductor	Inductor power dissipation
	M Irms	659.582 mA	Mosfet	MOSFET RMS ripple current
17.		38.657 mV	Mosfet	Voltage drop across the MosFET
18.		459.39 μW	Power	Input capacitor power dissipation
	Cout Pd	114.19 μW	Power	Output capacitor power dissipation
	Diode Pd	171.28 mW	Power	Diode power dissipation
	IC Pd	226.87 mW		·
			Power	IC power dissipation
	L Pd	29.7 mW	Power	Inductor power dissipation
	Total Pd	428.433 mW	Power	Total Power Dissipation
24.	Cross Freq	20.219 kHz	System Information	Bode plot crossover frequency
25.	Duty Cycle	43.505 %	System Information	Duty cycle
26.	Efficiency	92.455 %	System	Steady state efficiency
27	FootDrint	201.2	Information	Total Fact Drint Area of DOM components
27.	FootPrint	291.0 mm²	System Information	Total Foot Print Area of BOM components
28.	Frequency	1000.0 kHz	System Information	Switching frequency
29.	Gain Marg	-32.313 dB	System Information	Bode Plot Gain Margin
30.	lout	1.0 A	System	lout operating point
			Information	
31.	Low Freq Gain	66.233 dB	System	Gain at 1Hz
٠	_5	00.200 db	Information	
32.	Mode	CCM	System	Conduction Mode
JZ.	IVIOUE	CCIVI	Information	Conduction wode
22	Phasa Mara	90 654 400		Rada Plat Phasa Marain
33.	Phase Marg	89.654 deg	System	Bode Plot Phase Margin
	<b>5</b> .	5.05.147	Information	T. 1
34.	Pout	5.25 W	System	Total output power
			Information	
35.	Vin	12.5 V	System	Vin operating point
			Information	
36.	Vout	5.25 V	System	Operational Output Voltage
			Information	
37.	Vout Actual	5.244 V	System Information	Vout Actual calculated based on selected voltage divider resistors

#	Name	Value	Category	Description
38.	Vout Tolerance	5.272 %	System	Vout Tolerance based on IC Tolerance (no load) and voltage divider
			Information	resistors if applicable
39.	Vout p-p	9.484 mV	System	Peak-to-peak output ripple voltage
			Information	

# **Design Inputs**

Name	Value	Description	
lout	1.0	Maximum Output Current	
SoftStart	6.0 ms	Soft Start Time (ms)	
VinMax	12.5	Maximum input voltage	
VinMin	11.5	Minimum input voltage	
Vout	5.25	Output Voltage	
base_pn	TPS54332	Base Product Number	
source	DC	Input Source Type	
Та	40.0	Ambient temperature	

# WEBENCH® Assembly

#### Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

#### Soldering Component to Board

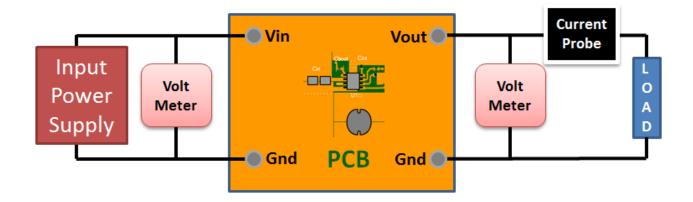
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

#### Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 11.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum lout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

#### Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

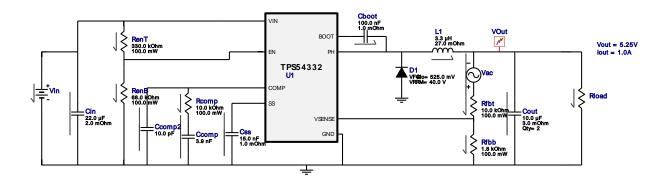


# WEBENCH® Electrical Simulation Report

Design Id = 1

sim\_id = 1

Simulation Type = Bode Plot



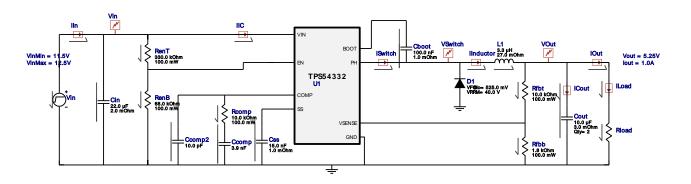
### Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cout	IC	no description	no values
2.	Cinj	С	Injection Capacitance	10000000 F
3.	Linj	L	Injection Inductance	10000000 H
4.	Vinj	AC	AC Signal	1
5.	Rload	R	Load Resistance	5.25 ohm



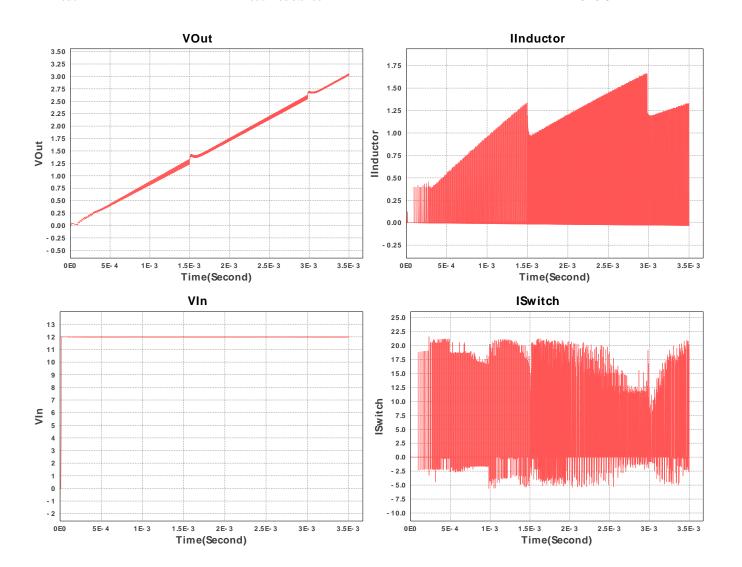
Design Id = 1 sim\_id = 2

Simulation Type = Startup



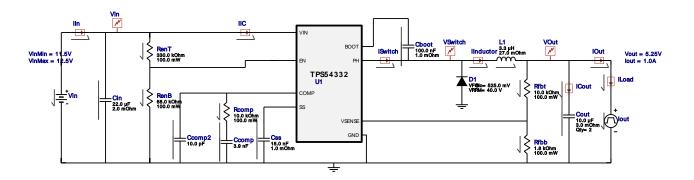
### Simulation Parameters

# Name	Parameter Name	Description	Values
1. Rload	R	Load Resistance	5.25 Ohm



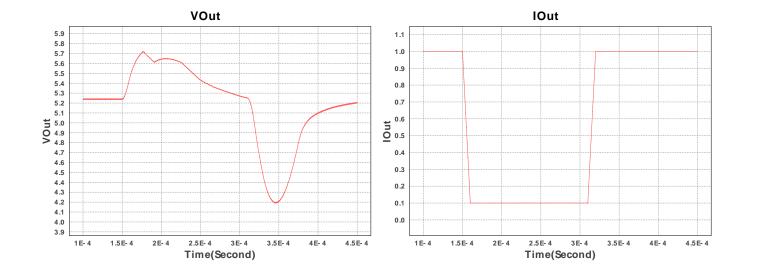
Design Id = 1 sim\_id = 3

Simulation Type = Load Transient



# Simulation Parameters

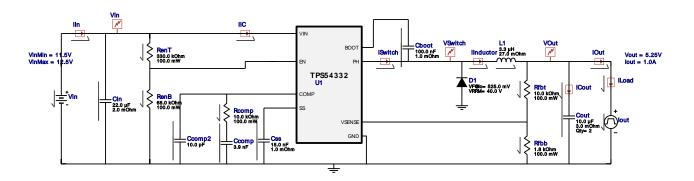
#	Name	Parameter Name	Description	Values
1.	Cboot	IC	Initial Voltage	12.0 V
2.	L1	IC	Initial Current	1.0 A
3.	lout	signal_type I1	Signal Type Initial Load Current	PULSE 1.0 A
		l2 Td	Minimum Load Current Initial Time Delay	0.1 A 150u s
		Tf Tr	Fall Time Rise Time	10u s 10u s
		Pw	Pulse Width	150u s



Design Id = 1

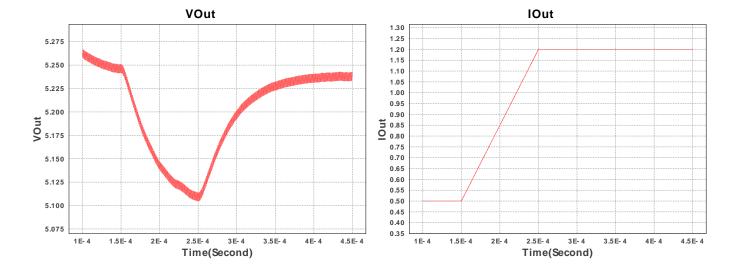
 $sim_id = 4$ 

Simulation Type = Load Transient



#### Simulation Parameters

		Values
1. Cboot IC	Initial Voltage	12.0 V
2. L1 IC	Initial Current	1.0 A
3. lout signal_type I1 I2 Td Tf Tr Pw	Signal Type Initial Load Current Minimum Load Current Initial Time Delay Fall Time Rise Time Pulse Width	PULSE 0.5 A 1.2 A 1.5E-4 s 1.0E-4 s 1.0E-5 s 7.5E-4 s



## Design Assistance

- 1. Master key : D402FA6FE69D6C85[v1]
- 2. TPS54332 Product Folder: http://www.ti.com/product/TPS54332: contains the data sheet and other resources.

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