

Q1^{a)} atomicity was violated : some sub-operations were applied while the overall logical transaction did not complete (no confirmed booking shown)

Durability may also be violated if the server crash occurred before changes were flushed to stable storage committed state might be lost

b) They system performed multiple related writes across components without a single atomic transaction spanning them

The application didn't use a transactional mechanism (e.g., database transaction with begin/commit) then a crash between partial writes leaves the system in inconsistent state

c) Server begin Transaction
driver accepted ride Customer wallet balance was deducted server crashed DBMS sees transactions that ended without commit, it will roll back

d) loss of customer, financial loss, damage to brand

P2

(a) Let initial quantity be Q . Let sold units in T_1 be s and returned units in T_2 be r

- A common problematic interleaving is

$$r_1(Q), r_2(Q), w_1(Q := Q - s), w_2(Q := Q + r)$$

(read by T_1 , read by T_2 , then T_1 writes, then T_2 writes)

(b) Conflicts occur when two diff transactions access the same item and atleast one access is a write
Examining the interleaving:

1) $r_1(Q)$ then $r_2(Q)$ - read/read: no conflict

2) $r_1(Q)$ then $w_1(Q)$ - same transaction ignore

3) $r_1(Q)$ then $w_2(Q)$ - Read by T_1 before write by T_2 :
Conflict $T_1 \rightarrow T_2$

4) $r_2(Q)$ then $w_1(Q)$ - read by T_2 before write by T_1 :
Conflict $T_2 \rightarrow T_1$

5) $w_1(Q)$ then $w_2(Q)$ - write/write conflict $\Rightarrow T_1 \rightarrow T_2$
already present

Graph  cycle

(c) has a cycle the schedule is not conflict serializable option 2 T_2 then T_1 :

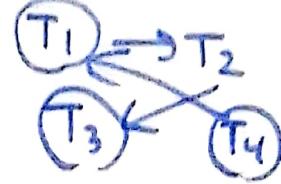
$$r_2(Q), w_2(Q := Q + r), r_1(Q), w_1(Q := Q - s) \Rightarrow \text{final } Q + r - s$$

(d) option 1 T_1 then T_2 : $\rightarrow r_1(Q), w_1(Q := Q - s), r_2(Q), w_2(Q := Q + r)$
final quantity becomes $Q - s + r$

(e) Incorrect inventory Customer dissatisfaction, Revenue loss



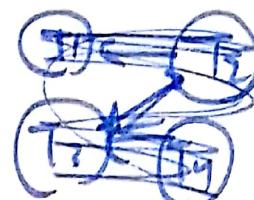
Q3



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S₁: preendene edges $T_1 \rightarrow T_2 \rightarrow T_3, T_3 \rightarrow T_4, T_4 \rightarrow T_1$
 \rightarrow cycle \rightarrow not serializable

S₂: preendene edges $T_4 \rightarrow T_3, T_2 \rightarrow T_3, T_2 \rightarrow T_1, T_4 \rightarrow T_1 \rightarrow$
 acyclic \rightarrow serializable



Example equivalent serial serial schedules

$T_2 \rightarrow T_4 \rightarrow T_3 \rightarrow T_1 \sim T_4 \rightarrow T_2 \rightarrow T_3 \rightarrow T_1$ (both valid as they respect the edges)

Q4

1) lost update (write-write) anomaly : both T_1 and T_2 reads the same initial value (2000) and compute update independently. T_1 writes 1700 then T_2 overwrites that with 2800 - T_1 update is effectively lost
 Non-serializable interleaving: The interleaving does not correspond to any serial execution of inconsistent outcome

2) 2800 (T_2 's write overwrote T_1 's write)

3) If t1 then T_2

$$\text{After } T_1: 2000 - 300 = 1700$$

$$\text{then } T_2 \text{ adds } 800: 1700 + 800 = 2500$$

If b then T_1

$$\text{After } = 2800$$

Then T_1 applies discount: $2800 - 300 = 2500$
 final 2500



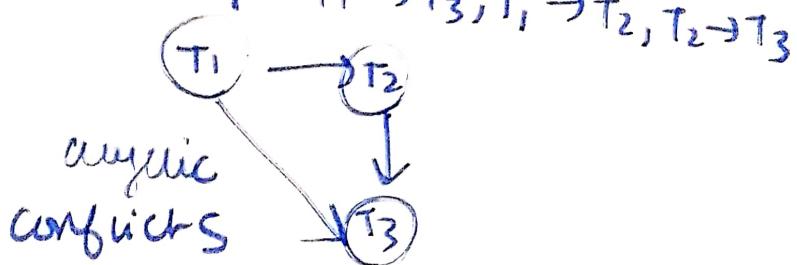
~~Q5~~

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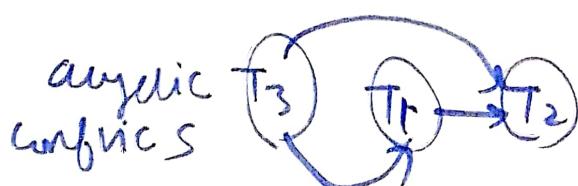
- (a) Serializable e.g. S : $T_1 \rightarrow T_2 \rightarrow T_3$
 (b) Serializable e.g. S : $T_3 \rightarrow T_1 \rightarrow T_2$
 (c) Serializable e.g. S : $T_2 \rightarrow T_3 \rightarrow T_1$
 (d) not conflict-serializable (cycle b/w T_1 and T_3)

(a) schedule $r_1(x); w_1(x); r_3(x); r_2(x); w_3(x)$

Conflict edges $T_1 \rightarrow T_3, T_1 \rightarrow T_2, T_2 \rightarrow T_3$



(b) edges from conflict $T_3 \rightarrow T_1, T_3 \rightarrow T_2, T_1 \rightarrow T_2$



(c) Edges from conflict $T_2 \rightarrow T_3, T_3 \rightarrow T_1$



(d) edges from conflict $T_2 \rightarrow T_3, T_1 \rightarrow T_3, T_3 \rightarrow T_1$



Cycle b/w T_1 and T_3 not conflict serializable.