

FSK Receiver

ECE 432 Microwave Circuit Design II

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Abstract—This report documents the successful completion of the Spring 2013 ECE 432 FSK design project. Topics covered are the design, simulation, and testing of microwave circuits suitable for operation between 2GHz to 3GHz. Specific circuits discussed include a 10+dB gain block, a Wilkenson power divider, high Q bandpass filters, and diode detectors. These elements were combined and tested to demonstrate that two microwave frequencies separated by only 200MHz could accurately be differentiated from each other by comparing the output voltage of the diode detectors. The target frequencies of 2.4GHz and 2.6GHz had to be shifted down by 100MHz due to inconsistencies in the filters used. However, when adjusted for this issue, the FSK receiver functioned as desired and successfully differentiated between 2.3GHz and 2.5GHz inputs.

I. FSK RECEIVER BACKGROUND

II. FSK RECEIVER DESIGN

The following sections describe the design and building procedures for each part of the FSK receiver. At the end, the results are documented and analyzed.

III. LNA DESIGN

The gain block used in this design used a PSA4-5043+ MMIC with an input matching network and bias T's. This is a microwave amplifier IC with realizable gain of 10 to 11 dB at 2.4GHz. It is also internally biased so only a single supply voltage needs to be provided. For both simulation and testing, 5 volts was applied to the drain through an external bias T consisting of a 22nH inductor isolating the supply and a 33pF capacitor isolating the load. The input used a single 33pF capacitor to AC couple to the source. FR4 substrate was used with a height of 59mil and 1/2oz copper on both sides. The test board was created using a simple mechanical circuit router.

IV. LNA SIMULATION

Simulation of the gain block was done using Agilent's Advanced Design System (ADS) software suite and the provided characterization files for the PSA4-5043+ amplifier. The scattering matrix for the amplifier showed that S11 could be decreased by adding an input matching network. The unmatched S11 is shown in Figure 1. Given that the intention for this circuit is for it to be driven by an antenna, we decided to attempt to preform this matching. Using the Smith chart tool in ADS, a series/stub combination was calculated and used for simulaiton. This was then tuned to provide the minimal S11 at 2.5GHz. This can be seen in Figure 2. With input matching the

simulation of the LNA showed a projection of 12 to 11.5 dB of gain over the frequency range of interest as can be seen in Figure 3. The completed simulated circuit schematic is shown in Figure ??.

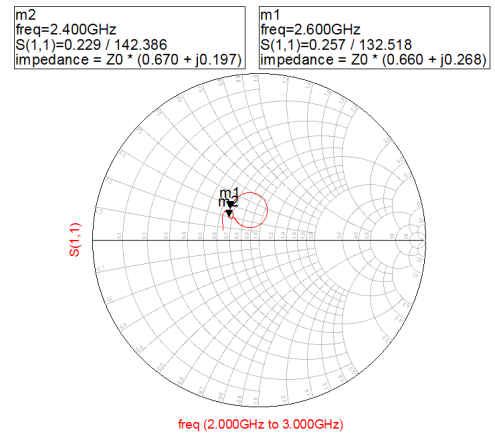


Fig. 1. Simulation results for LNA with matching.

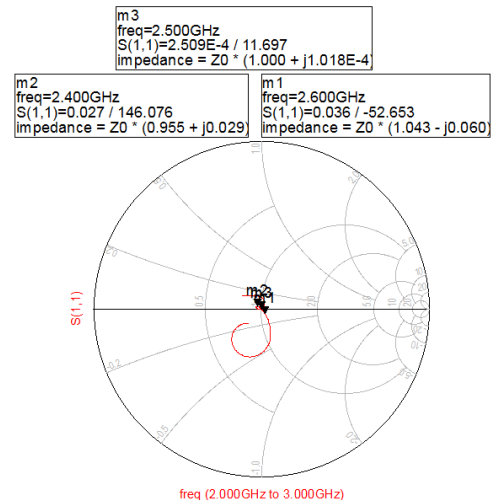


Fig. 2. Simulation results for LNA with matching.

V. LNA LAB RESULTS

The test board layout was generated using ADS and footprints for connectors were added. This layout was then routed using a mechanical circuit router on 59mil thick FR4

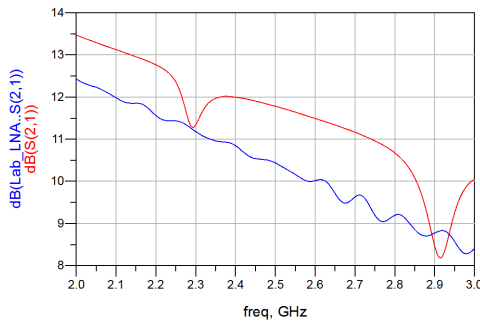


Fig. 3. Simulation gain projection.

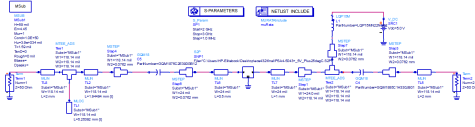


Fig. 4. LNA schematic.

with 1/2oz copper on both sides. Vias to the ground plain were created by drilling 0.35mm holes and then pressing 30AWG bare copper wire through them. These were then soldered to ensure constant electrical connectivity. Murata microwave components were used for the AC coupling capacitors and DC bias inductor. Total board size with connector footprints was approx. 1in x 2in. As the blue line in Figure 3 shows, this board was found to produce gain of approximately 11dB at 2.4GHz and 10dB at 2.6GHz. This was less than predicted by simulation but sufficient for the application's targets.

VI. WILKINSON DIVIDER DESIGN

The design of the Wilkinson power divider was done with the aid of ADS's built in Wilkinson divider coupler tool¹. The result can be seen in Figure 5. Transmission line was added on the outputs to be able to connect the bandpass filters. The simulation results, shown in Figure 6, gives close to a -3-dB insertion loss for both 2.4 GHz and 2.6 GHz as expected. Figure 7 shows the layout used when manufacturing the board in the EPL.

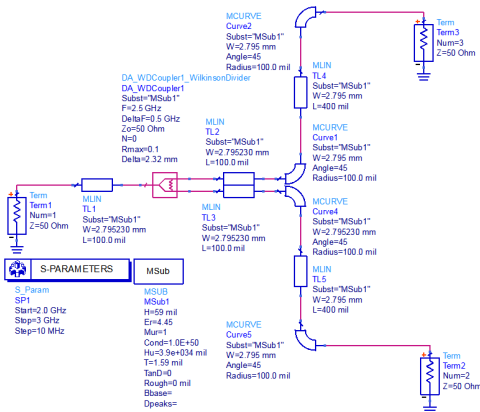


Fig. 5. Wilkinson power divider schematic.

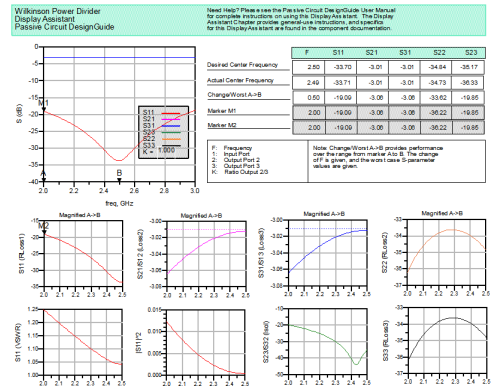


Fig. 6. Simulation results for the Wilkinson power divider.

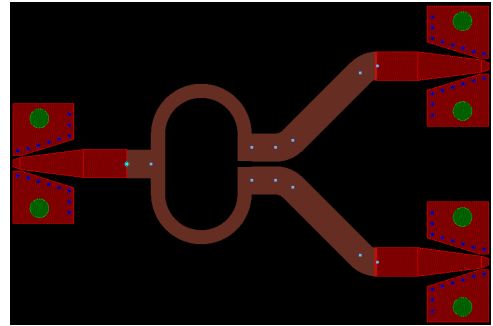


Fig. 7. Wilkinson power divider layout.

VII. BANDPASS FILTER LAB RESULTS

The 2.4 GHz and 2.6 GHz bandpass filters were designed by our TA Lunan Zhang[3]. The results for the 2.4 GHz and 2.6 GHz bandpass filter are shown in Figure 8 and Figure 9, respectively. The filters were off by about 100 MHz and will have an impact on the overall FSK receiver design.

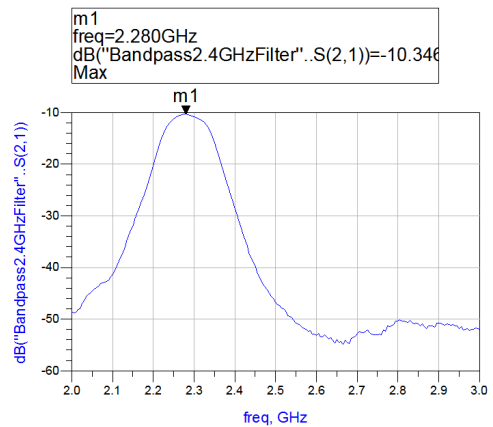


Fig. 8. Lab result for the 2.4 GHz bandpass filter.

VIII. DIODE DETECTOR BACKGROUND

Diode detectors are used to detect if a signal is present. Matching circuits are often required to detect a specific frequency.

¹It is available in the DesignGuide -> Passive Circuit menu.

the two circuits in the EPL will be very difficult due to manufacturing variations. Thus, it is anticipated that the the center frequency will not be near 2.4 GHz and 2.6 GHz.

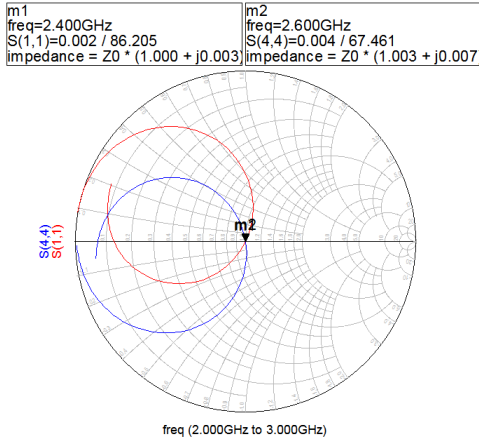


Fig. 15. Smith chart plot of complete diode detector circuit with properly matched input.

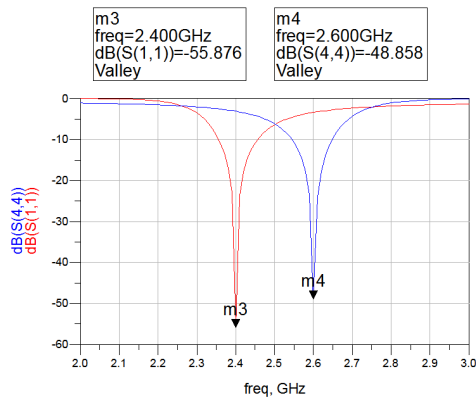


Fig. 16. S11 plot of complete diode detector circuit with properly matched input.

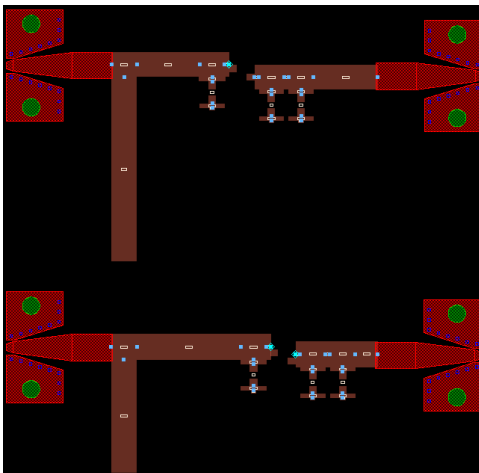


Fig. 17. Layout of complete diode detector circuit with properly matched input (2.4 GHz detector above and 2.6 GHz detector below).

XI. DIODE DETECTOR LAB RESULTS

Figure 17 shows the diode detector layout. The circuit was fabricated using the LPKF in the EPL.

A. 2.4 GHz Diode Detector

Figure 18 shows a comparison between the simulation and the actual measurements in the lab. The match did not work and will have significant signal loss. This will be verified by looking at the S11 magnitude. Figure 19 shows the S11 comparison. The poor result from the lab will have a negative impact on the overall FSK receiver.

B. 2.6 GHz Diode Detector

Figure 20 shows a comparison between the simulation and the actual measurements in the lab. The match is fairly close but the frequency sweep travels in a different direction than what ADS predicts. This may prove to be a worthwhile and interesting point to explore. Figure 21 shows the S11 comparison. The lab results are not as impressive as the simulation but still show that the circuit works well and is matched very close to 2.6 GHz.

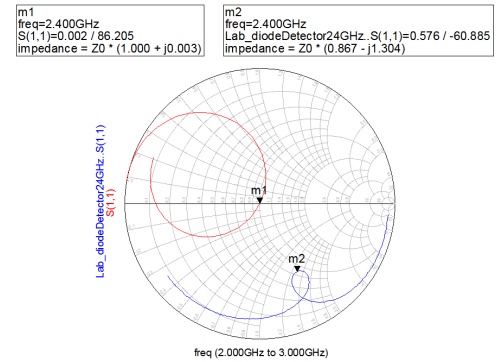


Fig. 18. Smith chart comparison between simulation and in-lab results for 2.4 GHz diode detector.

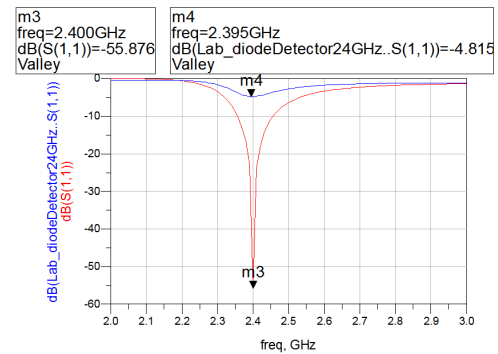


Fig. 19. S11 plot comparison between simulation and in-lab results for 2.4 GHz diode detector.

XII. FSK RECEVEIVER DESIGN

The FSK receiver was built using the results from above and connecting the subcircuits together². Figure 22 shows the final FSK receiver.

²Due to the lack of components, the entire FSK receiver was not built on a single PCB.

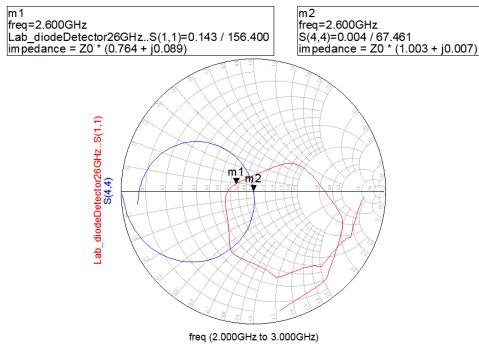


Fig. 20. Smith chart comparison between simulation and in-lab results for 2.6 GHz diode detector.

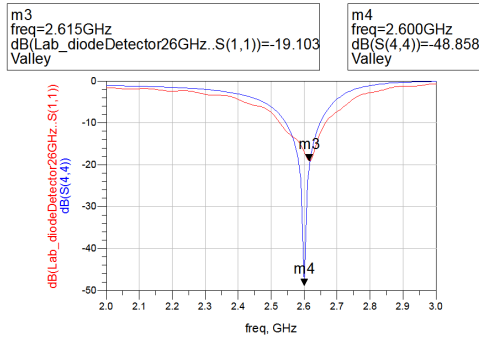


Fig. 21. S11 plot comparison between simulation and in-lab results for 2.6 GHz diode detector.

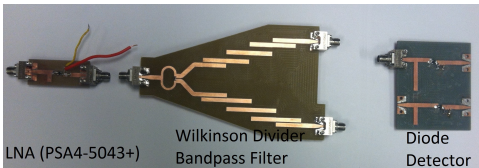


Fig. 22. FSK receiver.

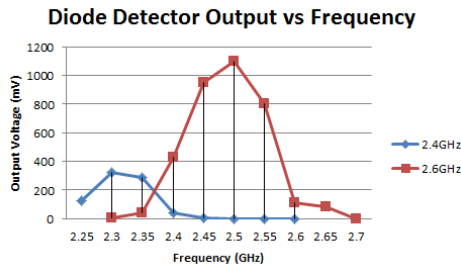


Fig. 23. FSK output voltage vs. frequency for each detector.

XIII. FSK RECEVEIVER LAB RESULTS

Table II and Table III show the measured results obtained from the FSK receiver. The main problems in the design stem from the bandpass filter being off by 100 MHz as well as the mismatch on the diode detector. Improving these two circuits will yield better results. When displayed graphically, as in Figure ??, it is clear that even with the large S11 of the 2.4GHz diode detector that differentiating between the two frequencies is still possible. These results were acheived with an input

TABLE II. FSK RECEIVER 2.4 GHZ FREQUENCY SWEEP

Frequency Sweep (GHz)	Output Signal at 0 dBm (mV)
2.25	124
2.30	320
2.35	290
2.40	40
2.45	4
2.50	0.56
2.55	0.08
2.60	1.2

TABLE III. FSK RECEIVER 2.6 GHZ FREQUENCY SWEEP

Frequency Sweep (GHz)	Output Signal at 0 dBm (mV)
2.30	4
2.35	44
2.40	430
2.45	950
2.50	1100
2.55	800
2.60	110
2.65	80
2.70	1.3

power of 0dBm which is much larger than would be likely in a real world application. Much of the gain acheived in the gain block, if not all, was lost in the splitter and filters. While the 3dB loss from the splitter may well be acceptable, the roughly 7dB loss from the filters is quite unacceptable. Future revisions to this design should focus primarily on finding a more efficient filters and properly tuning them to the desired frequencies. After the filtering loss, the next area of improvement for this design would be the the inconsitent S11 measurement of the 2.4GHz diode detector. Acheiving an S11 measurement of closer to -20dB would produce approximately 800mV of margin at the target frequency alone. This margin would allow for additional reduction in input power required for achieving a differentiable output voltage.

REFERENCES

- [1] Avago Application Note 1124
- [2] K. Payne, "Practical RF Amplifier Design Using the Available Gain Procedure and the Advanced Design System EM/Circuit Co-Simulation Capability," Agilent Technologies (5990-3356EN), 2008.
- [3] Zhang, Lunan, ECE 532/432 Microwave Circuit Design II Lab TA