Week 4 Report
ECE 432 Microwave Circuit Design II

Jackson Pugh
Portland State University
Portland, OR 97207
Email: japugh@pdx.edu

Michael Woodruff
Portland State University
Portland, OR 97207
Email: michael.woodruff@pdx.edu

I. Introduction

Goal of this session is to explore simulation tools (ADS) usage in design for stability, noise and gain. We will use SAV-541+ transistor and you should have its S2P parameters stored somewhere thats easily accessible. We will follow the first 30 pages or so from reference[1]. Basic idea is to apply the same techniques explained in there but to our own transistor. For our overall FSK receiver project your design has to cover 2.4 2.6 GHz range with at least 10dB of gain. Noise figure should be minimized but it is not of primary importance, i.e. it can be sacrificed for gain.

II. Questions & Answers

1. Design a bias network for SAV-541+ transistor with VDS=3V and IDS=60 mA. Present schematic and result for your design. You can use any of the several designs in various application notes but you may want to start with a simple resistive design.

a. Investigate and comment on sensitivity of your bias to variations of component values.
b. Comment on how well your design will integrate with future matching network that you will design (i.e. think about this as you design your bias circuit).

Figure 1 shows the DC bias network for the SAV-541+ transistor. It was determined from the SAV-541+ I-V curves that the gate voltage applied to the MOSFET transistor needed to be 0.5 V (V_{GS}) to obtain a 60 mA I_{DS} current, thus the resistor divider was chosen to give a close match (however, some additional tweaking was required to get the current closer). The BJT current mirror also acts to bias/force IDS to be 60 mA. The supply power was chosen to be 3.7 V (instead of 3.3 V) due to the 0.7 V drop from the BJT current mirror. An additional resistor was required (R6) to produce the 3 V drain to source voltage. Figure 2 shows the screenshot result from the DC simulation in ADS. The results from the bias network are accurate. There are several critical components that determine the biasing of the transistor. These include the voltage divider at the gate and the resistor that determines the current being drawn at the current mirror.

2. Do a "quick" comparison between S-parameters given by the manufacturer and S-parameters you get from a model that was distributed. Report back if you find any significant discrepancies, in particular in |S21|.

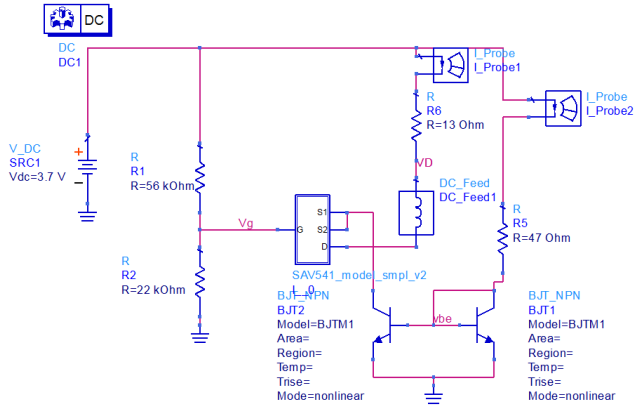

Fig. 1. DC bias network for the SAV-541+ transistor.

freq	I_Probe1.i	Vg	VD	I_Probe2.i	vbe
0.0000 Hz	60.87 mA	620.4 mV	2.909 V	62.54 mA	760.4 mV

Fig. 2. Current and voltage parameters from the DC bias network for the SAV-541+ transistor.

Figure 3 shows the S-Parameter biased network transistor circuit. Figure 4 shows the S-Parameters comparison between the untuned bias network circuit and the manufacturer S2P data. The bias network shows little discrepency.

3. Using ADS design guide for amplifiers, reproduce figure 13 from[1]. In your report comment on the amount of gain and stability. Limit your frequency range to 0.1 6 GHz. Do you anticipate any problems based on these results?

Figure 5 shows various information provided by the ADS amplifier design guide tool. The circuit is potentially

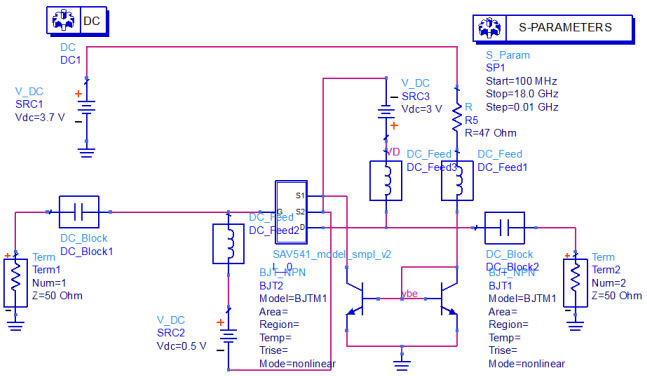

Fig. 3. S-Parameter bias network for the SAV-541+ transistor.

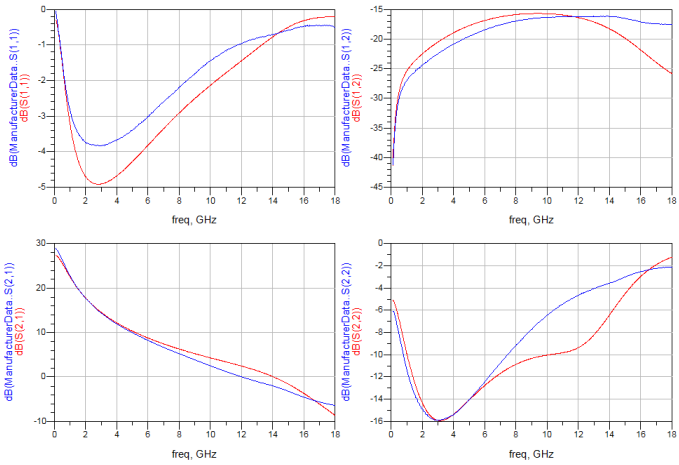

Fig. 4. S-Parameter simulation result comparison between the bias network and the manufacturer S2P data file.

unstable below around 4 GHz. Thus, stabilizing resistors will be necessary in order to make the transistor unconditionally stable between 2.4 - 2.6 GHz (the intended frequency range).

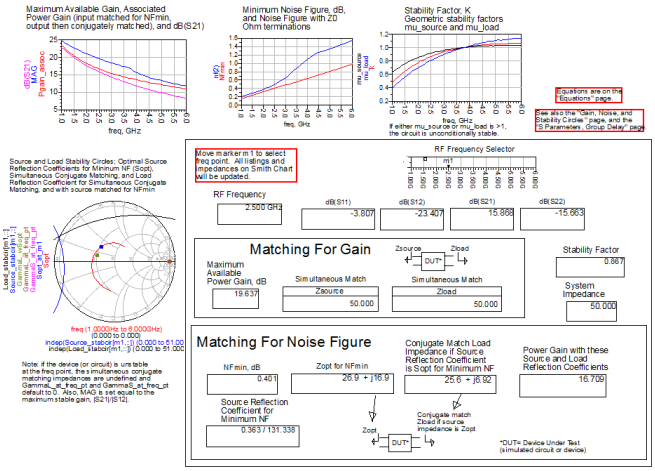

Fig. 5. Amplifier design guide generated in ADS for the bias network for the SAV-541+ transistor.

REFERENCES

[1] K. Payne, "Practical RF Amplifier Design Using the Available Gain Procedure and the Advanced Design System EM/Circuit Co-Simulation Capability," Agilent Technologies (5990-3356EN), 2008.