International Journal of Electrical and Electronics
Engineering Research (IJEEER)
ISSN 2250-155X
Vol. 3 Issue 1 Mar 2013 1- 10

TRANS STELLAR
•Journal Publications •Research Consultancy

A CIRCUIT LEVEL IMPLEMENTATION OF A CDMA BASED DPU USING 90 NM CMOS TECHNOLOGY

SHAMIMA KHATOON[1], RAVI MOHAN[2] & SUMIT SHARMA[3]

[1]Research Scholar, Shri Ram Institute of Technology, Jabalpur, Madhya- Pradesh, India

[2,3]Assistant Professors in Department of Electronics & Communication Engg, (VLSI) Shri Ram Institute of Technology, Jabalpur, Madhya- Pradesh, India

ABSTRACT

In this Paper an area efficient design for highly compact, low power digital processing unit of a receiver is presented. The proposed DPU is based on hybrid CMOS design style using 90nm CMOS process technology. The design consists of 4 modules – a detector, a correlator (Synchronization circuit) an integrator and decision or display unit. Three of them are carefully implemented upto circuit level with the proper W/L ratio and the fourth one is left for the researchers for future work. Reduced area is one of the most required features of the modern electronic system designed for low cost and high yield, on the other hand, low power dissipation results in high performance and portable applications. The tradeoff between cost and performance is fundamental to aim of the proposed design. The implemented design consumes less area, offers less delay and power dissipation without trading of driving capabilities and reliabilities. The design is based on the algorithm that enhances the security of the system to which it is attached. This unique design successfully operates at low voltage upto 1.2 V and wide operating frequency range between 2MHz to 20GHz with excellent linearity, signal integrity and driving capability. The layout designing is done manually using an educational tool called Micro wind 3.1.Simulation of layout and parametric analysis is performed and results are discussed. It can be concluded that the proposed DPU is more reliable in terms of Area, Power dissipation, speed and security.

KEYWORDS: Area Efficient, Digital Processing Unit (DPU), Subunits (Sus), CDMA, 3T (Three Transistors), Transceiver

INTRODUCTION

Recently, the RFID tag system is paid attention to as an identification source. Each RFID tag is attached to some object, whose is information needed at the user end. With the unique ID of RFID tag, a user identifies the object provided with the RFID tag and derives information about the object. One of the important applications of RFID technology is in estimating the presence of an object within its communication range. The hundreds of diversifying applications of RFID technology have fuelled much research into new and more power efficient methods of radio communication. RFID tags can also be fitted to the persons working in the company, for identifying them for security purpose So that no other than the company employee can enter the company. Such applications can reduces the risk of endangers and terrorist attacks in any organization.

But, unfortunately, it has not gone so far, as most wireless devices require batteries which typically contain elements of high atomic mass number that would scatter radiation and may harm the person to which the RFID tag is attached. Also, passive RFID tags with no batteries are not suitable, as they rely on the power transmitted by the receiver. Such tags increase the receiver complexity as well as require the supporting handshaking mechanism between the RFID tag and receiver, which further increases power consumption at the receiver side. Thus, this paper focuses on the efficient

utilization of a battery less, active, self powered RFID tag, to identify the person to which the tag is attached. This system would eliminate the need of harmful batteries and would open a host of applications in situations where power grid access is often unavailable, such as extended link expenditions or military missions.

So, highly compact, Low power and fast circuits are the basic requirement of such applications. Increasing demand of such circuits have fuelled much research into the different styles of VLSI design which can be addressed at different design levels, such as the architectural, circuit, layout, and process technology level. At the circuit design level, by means of proper choice of logic style and process technology considerable effort can be made in the field of these areas. The absence of compact design techniques leads to increased circuit cost because the die cost is a strong function of die area. High power dissipation from a certain application can result in short battery life, while cooling and packing them would be very difficult and thus leading to an unavoidable increase in the cost of the product. The use more number of slow PMOS also reduces the speed. Conclusively, area efficiency as well as energy efficiency both are significant.

OVERVIEW OF THE TRANSCEIVER ARCHITECTURE

Our wireless application system prototype consists of two subsystem, namely- an RFID Transmitter (Tag) and an RFID Receiver (Reader), along with the wireless communication path, that is truly the air medium.

RFID Transmitter

A battery less, active self-powered RFID Tag, can transmit N bit wireless identification code to the receiver, enabling the user to transmit their identity automatically to the Reader, as the user walks. A complete block diagram of the Tag along with the power supply is shown in fig 1. Its main blocks are- Piezo-electric transducer, Power conditioning electronic circuit, Serial ID digital encoder (or microcontroller), ASK/OOK/BPSK serial transmitter fitted to the antenna. An average person spends a significant part of the day on foot, dissipating abundant energy into the insole of the shoe, thus a piezoelectric element, a PZT unimorph, is inserted into a soft sports sneaker, can be the most attractive to be the source of self-powering, of the transmitter.

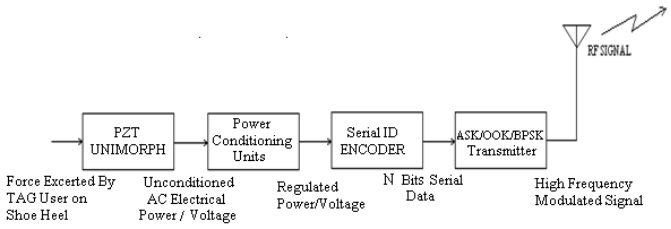


Figure 1: Block Diagram of the RFID Tag

RFID Receiver/Reader

At the reader side, the energy detection receiver [17], has been identified as the most feasible solution which is treated in the following paragraphs. A System Model of the Energy Detection Scheme is shown in figure 2 that can be apply for the detection of N no. of Tags with proper circuit implementation.

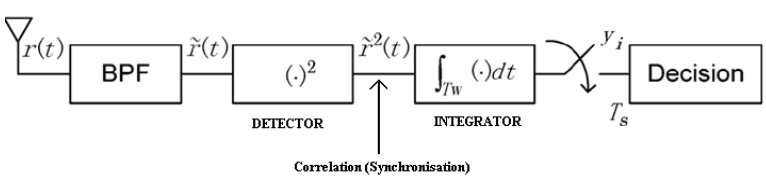


Figure 2: Block Diagram of Receiver

The model can be applied to the multiple Tags that are transmitting their unique identification code at different assigned modulation frequencies, but at the same time. The RFID Reader or receiver architecture can be divided into two namely, an analog front end (AFE) and a Digital Processing Unit(DPU). The detailed block diagrams of these two receiver blocks are shown below, where figure 3(a) shows the Analog Processing Block and figure 3(b) shows the Digital Processing Block.

The present work includes the realization and analysis of the Digital Processing Unit only, leaving the AFE as a part for the other researchers for future works. The security greatly increases as the communication will include Hybrid styles of multiplexing i.e. FDM as well as CDM. The analog processing block demodulates different frequency signals, where as digital processing block will despreads the different codes in respective parallel processing blocks (PPB).The no. of PPB are equal to the no. of Tag users.

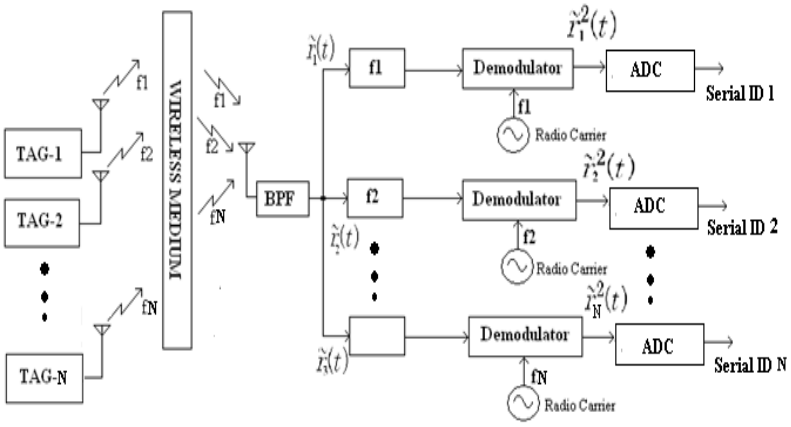


Figure 3(a): Block Diagram of RF/Analog Front end (AFE) Block of the Reader

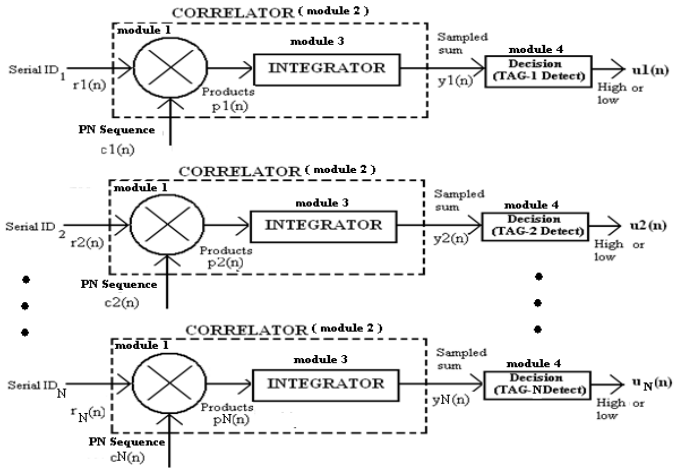


Figure 3(b): Block Diagram of Digital Processing Block/Unit (DPU) of the Reader

BASIC OPERATING PRINCIPLE OF THE RECEIVER

The concept of the reader (the receiver) is presented in figure 3(a) and figure 3(b). The basic working reveals the Direct Sequence Spread Spectrum Based CDMA receiver[13], but here instead of xoring, xnoring is used for despreading the received ID in DPU. The received signal is filtered, amplified, and converted to baseband in the Analog front end block. The baseband signal is then sampled with a chip frequency ($f_c = N/T_B$) in the analog-to-digital converter (ADC) and

it is carried to the input of the digital processing block which is responsible for the detection process. The matched filters separate the receiver into N independent, parallel processing channels. Such a structure allows reception of the signals from different tags that overlap in time, which is possible due to good cross-correlation properties of the used PN-sequence(N bit Serial ID).

Consider the kth channel of the receiver

$P_k(n) = r_k(n) * c_k(n)$ --- bit-wise xnor with the same id code

First the first resulting $u_k(n)$ bit encodes the sign

and the second bit $u_k(n)$ encodes the amplitude of the sample

$u_k(n) = 1$, when $y_k(n) = D$

0, when $y_k(n) < D$

Where D is the threshold, which is equal to the number of bits in the transmitted data.

PROPOSED WORK

The block diagram of the Digital Processing unit shown in figure 3(b) can be divided into four functional sub units or module. The present research work is focused on the circuit level implementation of the DPU of the Receiver.

Module 1

The incoming signal to the module 1 is assumed to be demodulated filtered signal from the AFE shown in figure 3(a). This is a N bit serial ID coming from the tag end. Module 1 act as a detector which provides a high output when the Tag Serial ID, r1(n)is matched bitwise with the stored receiver PN Sequence,c1(n). For this a three transistor(3T) Pass Transistor Logic Based XNOR circuit [7] is used that is shown in figure 4.

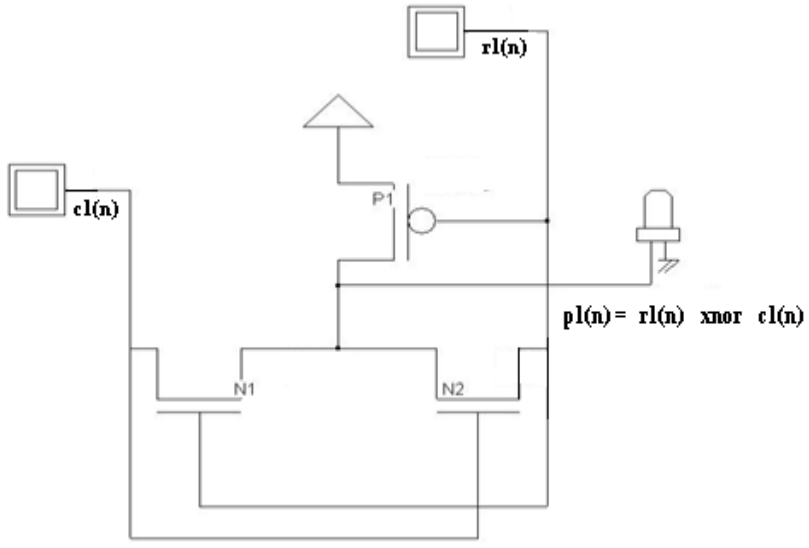


Figure 4: Schematic of PTL 3T XNOR Gate

For 90nm process, the length of the channel, L=0.100 µm, channel width of N1,WN_1 = 0.250 µm, channel width of N2, WN_2 = 0.750 µm, and channel width of P1,WP_1 = 0.500 µm.

Table 1: Analysis of Proposed PTL Based 3T XNOR Gate

INPUTS		MOSFETS LOGIC STATE			COMBINED OUTPUT	COMBINED OUTPUT With $WN_2 = 3 \times WP_1$
p1(n)	c1(n)	P1	N1	N2	p1(n) XNOR c1(n)	p1(n) XNOR c1(n)
0	0	ON	OFF	OFF	1	1
0	1	ON	OFF	ON	**X**	**0**
1	0	OFF	ON	OFF	0	0
1	1	OFF	ON	ON	1	1

Module 2

Module 2 is an N bit serial-in-parellel-out buffer which is implemented using N d type negative edge sensitive registors or flip-flops. The circuit implementation of flip-flop is shown in figure 5.

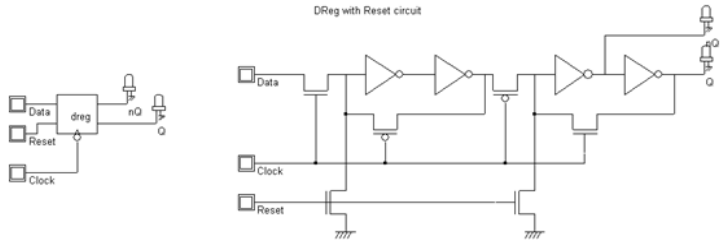


Figure 5: Schematic Representation of a Negative Edge Sensitive Flip-Flop

Module 3

It is an integrator circuit, which takes N bits from the SIPO, logical AND the bits and produces a logic '1' or high when all the inputs are high, i.e., when r1(n) matches with c1(n),indicating the presence of the Tag in the local environment. It is implemented as an N bit CMOS AND gate in which the width of each NMOS is 4 times the width of PMOS, i.e. if WP = 0.500 µm, then WN = 2.000 µm. This approach greatly increases the speed[1] [4].

PROPOSED DPU REALIZATION

The number of flip-flops in the SIPO and the CMOS AND gate inputs are equal, and in accordance with the number of bits in the received serial ID from the AFE. The number of bits in the serial ID defines the system capacity, i.e. the number of tag users. These relations are clearly shown in the table below.

Table 2: Analysis of DPU Capacity

No. of Bits in the SERIAL ID	No. of Flip-flops in the SIPO	No. of Inputs of CMOS AND Gate	Maximum No. of Tag Users
4	4	4	16
8	8	8	64
12	12	12	144
36	36	36	1296
64	64	64	4096
N	**N**	**N**	**2^N**

With the view of above relations , we conclude that $2^N \geq$ No. of Tag users. For the present work we are designing the DPU for system capacity upto 64 users, so our DPU is capable of identifying a single tag user upto 64 users. With the

knowledge of the no. of users, the no. of bits in the serial ID can be easily identified and thus the no. of flip-flops and inputs of AND gate. For present work we design the DPU for recognition of 8 bit serial ID.

Complete schematic of 8 bits, 64 user capacity DPU is shown in figure 6.

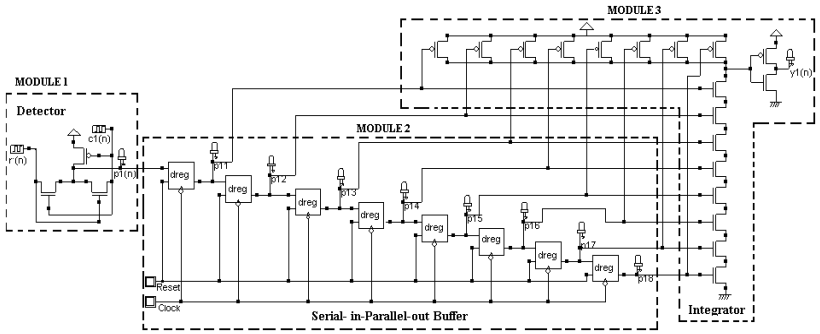


Figure 6: Schematic Realisation of Proposed DPU

LAYOUT DESIGNING OF THE PROPOSED DPU

The Layout is carefully designed manually using Microwind 3.1 EDA tool, [14] according to the design rules and selecting the desired foundry from the file menu. The layout is designed that is shown in figure 7 as per the schematics shown in figures. For present work the selected foundry is 90nm.The layout can be verified using Design Rule Checker(DRC). The design rule checker (DRC) scans all the design and verifies that all the minimum design rules are respected. Click on the icon or on **Analysis ->Design Rule Checker** to run the DRC. The errors are highlighted in the display window, with an appropriate message giving the nature of the error. Details about the position and type of the errors appear on the screen.

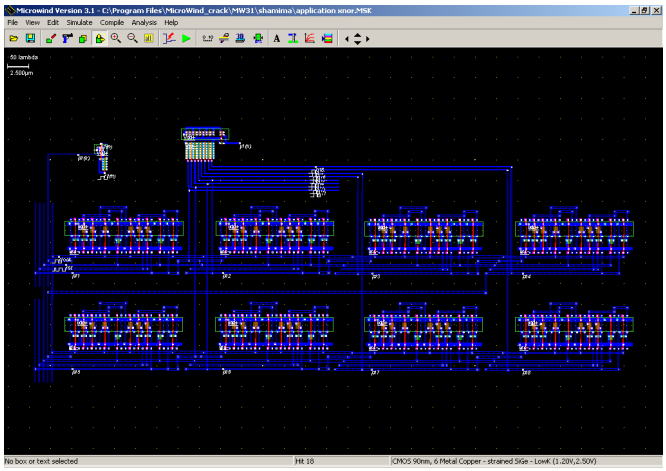


Figure 7: Layout Representation of the Proposed DPU Using 90nm CMOS Process

SIMULATION METHODOLOGY

The software used for the simulation of proposed Microwind version 3.1. Microwind program allows designing and simulation of integrated circuit at the physical description level up to various nano lambda technologies. The package contains a library of common logic and analog ICs to view and simulate. The software allows circuit simulation by pressing a single key and analog simulation produces voltage and current curves immediately.

The simulation steps refer to the Microwind user manual [14]. First of all manually design the layout of proposed full adder schematic shown in figure 3, using the Microwind 3.1.The layout should strictly follow the design rules of the respective foundry. The software can handle various technologies right from 1.2 µm till 22nm, that can be selected from the file menu. The process parameters are stored in files with appendix '.RUL'. The selected foundries for the present work are 6- metal 90nm [13], stored in the technology files Cmos90n.rul.The foundry can also be manually created by editing the default.rul technology file in the '.RUL' directory. The channel width can be adjusted by the MOS generator option located in the palette. Second step is to verify the layout in terms of design rules, by clicking on Design rule check (DRC) in the analysis menu. Errors are notified in the layout if it violates the design rules otherwise a message 'No Error' is displayed. If the circuit passes the DRC then the third step is to choose the input frequency (t=0.05ns, i.e approx. 20GHz)simulation model (level 3 or BSIM 4), then simulate the layouts to get the waveform shown in figure 8. Fourth step is to go to the analysis menu then click on the parametric analysis and then the output node carry, then choosing the voltage variations (for present work it is from 0.35V to 1.2V).Finally click on the parameter which needs to be calculated e.g. power dissipation(mw),maximum current Idd(ma),rise time, tr(ns), and fall time, tf(ns) from A to carry, for chosen model and get the results as shown in figure 9 and 10.

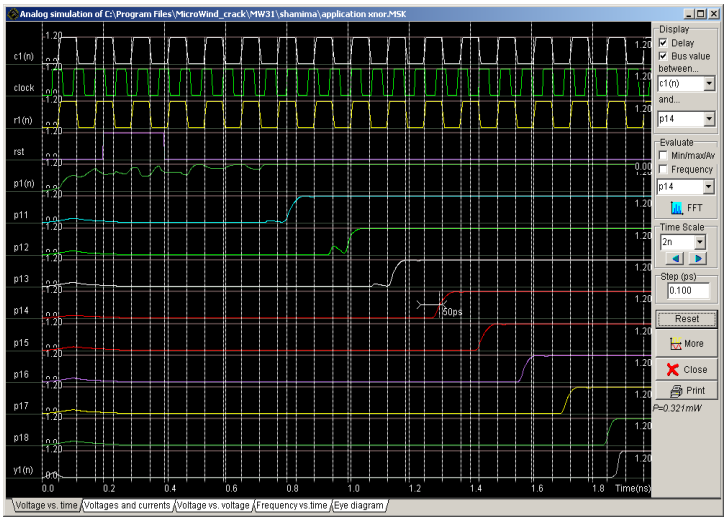
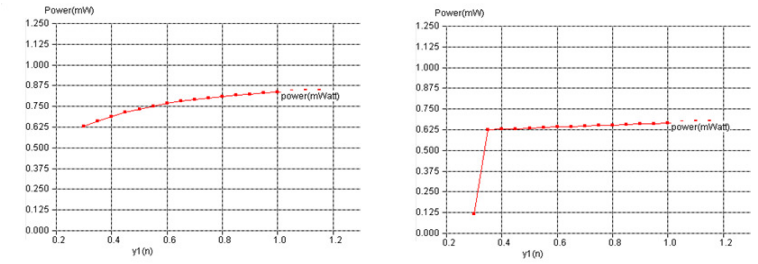


Figure 8: Simulated Waveform of Proposed DPU

The simulation waveforms clearly depicts the situation when serial ID, r1(n) matches with the stored PN sequence, c1(n).Suppose ,the output of the detector, p1(n) is high when the bits are matched. After reset p1(n) gets passed on to the SIPO, which takes the bits from detector serially as 11111111, and produces the same sequence i.e. 11111111,but in a time division manner, i.e. in parallel fashion. When one by one all the outputs of SIPO from p11 to p18 are high (this means that the bits are matched),the integrator output simultaneously become high just after the entry of p18. On the contrary if any one bit from p11 to p18 is low showing mismatching, the output of the integrator remains low, thus indicating the absence of the tag user or this tag user is not the part of the organization, so it will not be allowed to enter.

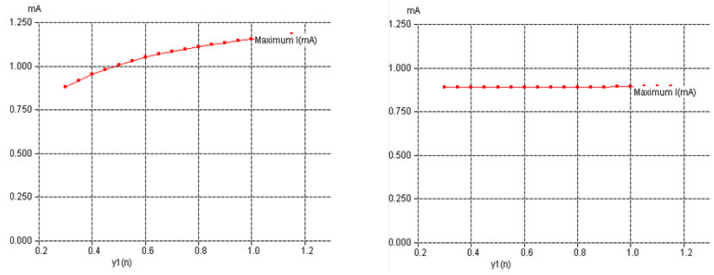
Parametric Analysis

Another step is to go to the analysis menu then click on the parametric analysis and then the output node carry, then choosing the voltage variations (for present work it is from 0.35V to 1.2V).Finally click on the parameter which needs to be calculated e.g. power dissipation(mw),maximum current Idd(ma),rise time, tr(ns), and fall time, tf(ns) from A to carry, for chosen model and get the results as shown in figure 10



(a) (b)

Figure 9: Power Dissipation Using Model (a) BSIM 4 and (b) Level 1



(a) (b)

Figure 10: Maximum Current Using Model (a) BSIM 4 and (b) Level 1

Table 3: Simulation Results of Full Adders

DPU		Supply	Avg Power Diss. in mW		Maximum Current Idd mA	
Technology	AREA in µm2	Voltage(V)	LEVEL-1	BSIM-4	LEVEL-1	BSIM-4
		0.35	0.625	0.637	0.900	0.916
3T XNOR	2195.7µm2	0.60	0.630	0.756	0.900	1.083
BASED		0.80	0.635	0.756	0.900	1.125
90nm		1.20	0.640	0.870	0.900	1.170

FUTURE WORK

The circuit can be analysed on the basis of area and power dissipation by using different set of W/L ratio and CMOS design styles, to conclude the best way of implementation. Designer can take the help of advanced EDA tools such s CADENCE and Tainer[15] for further researches. The proposed paper only detects the presence of the tag, as it meant for the short range communication with security codes, this application can be further extended upto the location tracing of the tag along with proper display unit as module 4 for the receiver.

CONCLUSIONS

The simulation shows that the area required for the DPU is only, 9.5µm2 using 90nm foundry which shows a drastic improvement in saving the area to large extent without compromising with the performance. This proves that the proposed DPU is area efficient. The circuit works efficiently with voltage supply of 1.2V, and can operates at a wide input frequency range between 2MHz to 20 GHz. However, circuit performance greatly improves in the frequency range from 50MHz to 200MHz. So, the power dissipation can be further reduced with selective frequency and supply voltage. The average delay for the proposed adder totally depends on the input frequency and remains fairly constant upto 50ps (worst case). The power dissipation and maximmun Idd current also seems to be almost constant in the given range of the voltage,

giving better results for the empirical model 1.

Such circuits are highly applicable in the design approaches in the areas of less availability of power supply such as extended military missions, or in the areas where high security is required such as company campus, educational institute, commercial banks, administrative offices, etc. for security purpose where all the employees or personnels can where shoes containing a chip that generates unique serial code or ID and can only be allowed to enter the institute after the reader identifies them. These codes are embedded in the chip of the transmitter and receiver and nobody knows them so the checking in highly secure which reduces the occurrence of terrorist attack, forgery and theft giving a fear free safe environment. This paper is just an approach towards wearable security system, further researches can be forced to improve the circuit level implementation of it.

ACKNOWLEDGEMENTS

The Authors acknowledge the support of the Shri Ram Institute of Technology, Jabalpur, M.P. (INDIA).She also like to specially thank Prof. Ravi Mohan, HOD (M-TECH),and Prof. Summit Sharma, HOD(B.E) to help her from their valuable guidance.

REFERENCES

1. N. Weste and K. Eshraghian, (2002) Principles of CMOS VLSI Design: *A System Perspective* Reading, Pearson Education, Addison –Wesley.
2. John P. Uyemura, (2002) *Introduction to VLSI circuits and systems*, Wiley John & Sons, Inc.
3. Sung-Mo Kang, Yusuf Leblebici, (2003) *CMOS Digital Integrated Circuits: Analysis and Design*, TATA Mc GRAW-HILL.
4. N. Weste and D. Harris, (2005) *CMOS VLSI Design*, Pearson Wesley.
5. J. Uyemura, (1999) CMOS Logic Circuit Design, Kluwer.
6. N. Jha and S. Gupta, (2003) Testing of Digital Systems. Cambridge, U.K.
7. Shamima Khatoon,"A Novel Design For Highly Compact Low Power Area Efficient 1-Bit Full Adders" , IJAET Sept-2012 ISSN 2231-1963 vol. 4, issue 2, pp. 464-473.
8. Candy Goyal, Ashish Kumar, "Comparative Analysis of Energy Efficient Low Power 1bit Full Addera at 120 nm technology", IJAET July-2012 ISSN 2231-1963 Vol. 3, Issue 1, pp. 501-509.
9. Mohammad Shamim Imtiaz, Md Abdul Aziz Suzon, Mahmudur Rahman, "Design of Energy-Efficient Full Adders Using Hybrid-CMOS Logic Style" IJAET Jan-2012 ISSN 2231-1963 Vol. 2, Issue 1, pp. 190-202.
10. Etienne SICARD,Syed Mahfuzul Aziz, (2010)"Introducing 32 nm technology in Microwind31" Microwind Application Note 32 Nm Technology.
11. Nilesh P. Bobade, Rajashree H. Umbarkar, Priyanka U. Badhe,Shruti V. Kohale, (2012) "Design performance of CMOS Circuits in Microwind",IJCA.
12. Ahmadreza Tabesh, Luc G. Fréchette, "A Low-Power Stand-Alone Adaptive Circuit For Harvesting Energy From A Piezoelectric Micropower Generator" , IEEE Transactions On Industrial Electronics, Vol.57, No. 3, March 2010.

13. Gustaw Mazurek, "Active RFID System With Spread-Spectrum Transmission" IEEE Transactions On Automation Science And Engineering, Vol. 6, No. 1, January 2009

14. Microwind and DSCH version 3.1, User's Manual, Copyright 1997-2007, Microwind INSA France.

15. Tanner EDA Inc. 1988, User's Manual, 2005.

16. Microwind and DSCH version 3.5, User's Manual, Copyright 1997-2010,Microwind INSA Toulouse, University of Toulouse France.

17. Zhuo Zou, David Sarmiento Mendoza, Peng Wang, Qin Zhou, Jia Mao, Fredrik Jonsson, Hannu Tenhunen, " A Low-Power and Flexible Energy Detection IR-UWB Receiver for RFID and Wireless Sensor Networks", IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 58, No. 7, JULY 2011.

AUTHORS

Shamima Khatoon received her B.E.(hons) from Shri Ram Institute of Technology, Jabalpur, M.P. in Electronics and Communication Engg and persuing her M.Tech in VLSI DESIGN from Shri Ram Institute of Technology, Jabalpur, M.P. She is in 4th Semester and engaged in completing her dissertation part 2 for the M-TECH thesis. Her research interests include Low Power and area efficient VLSI Design, VLSI design softwares such as Microwind versions 3,3.1,3.5 & DSCH versions 2.7,3,3.1,3.5, RFID technology, Self-powered microelectronics systems

Prof. Ravi Mohan, HOD-Master of Technology in Shri Ram Institute of Technology,Jabalpur, M.P. He is a known Professor of the institute and has guided various Engg. projects and Thesis. His main research areas are Digital Communication, Electronics Devices and Circuits, Communication Systems and Electro-Magnetic Theory.

Prof. Sumit Sharma, had done his PG from College of Engineering, Pune. He is HOD of Electronics and Communication branch in Shri Ram Institute of Technology, Jabalpur. His main research areas are Digital Signal Processing and Embedded systems.