Research paper on CMOS Operational Transconductance Amplifier with and without Miller capacitor

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1. Design and Simulation of a Two-Stage Miller Compensated CMOS Operational Amplifier

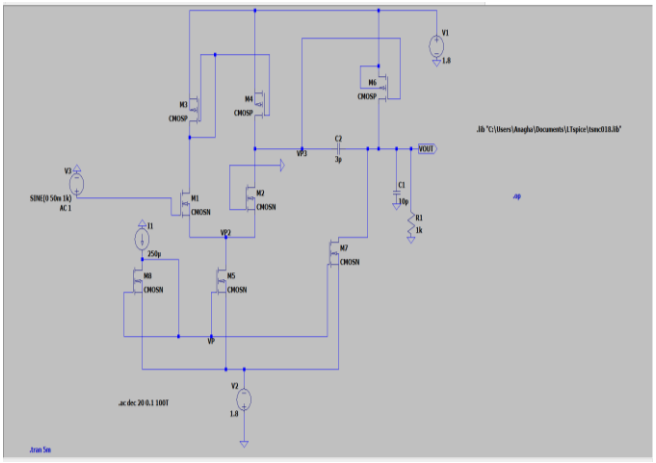
***Abstract*—This paper presents the design and simulation of a two-stage CMOS operational amplifier (op-amp) with Miller compensation in a 180 nm CMOS technology. The primary objective is to achieve a high open-loop gain of 77 dB while ensuring stability and adequate bandwidth. The design uses a classical two-stage architecture with a differential input stage and a Miller-compensated gain stage. Transistor sizing, biasing, and compensation techniques are employed to meet the gain requirement. LTspice was used for schematic design and simulation.**

Keywords— CMOS op-amp, Miller compensation, two-stage amplifier, high gain, 180 nm technology, LTspice simulation, analog circuit design, operational amplifier.

I. Introduction (*Heading 1*)

Operational amplifiers are fundamental components in analog circuit design. High-gain op-amps are essential in signal conditioning, data conversion, and active filtering. In scaled CMOS technologies, achieving high gain while maintaining stability requires careful design of the amplifier stages and compensation network. This work presents a design strategy using a Miller-compensated two-stage op-amp in 180 nm CMOS technology to achieve a target open-loop gain of 77 dB

II. Circuit Diagram



III. Design Methodology

The two-stage op-amp consists of:

- A differential input stage using NMOS transistors with PMOS active loads.
- A second gain stage using a common-source amplifier.
- A compensation capacitor (Miller compensation) to ensure phase margin and frequency stability.

The design is optimized for gain using the following equation:

$$A_v = A_1 \cdot A_2 = (g_{m1} \cdot r_{o1}) \cdot (g_{m2} \cdot r_{o2})$$

The transconductance (gm) is enhanced by increasing the W/L ratio of the differential pair and gain stage transistors. Output impedance (ro) is optimized by adjusting the channel length and using high-impedance current mirrors.

IV. Circuit Description

The op-amp uses a supply voltage of 0.9 V. A bias current of 250 µA is set by the tail current source. The transistor sizes (W/L in µm/0.18 µm) are:

Transistor	W (µm)	Function
M1,M2	180	Differential NMOS pair
M3,M4	60	PMOS active load(mirror)
M5	40	Bias for M3/M4
M6	100	PMOS load for second stage
M7	200	Common source second stage
M8	40	Tail current source

Miller compensation is provided with a 2 pF capacitor between the output and the intermediate node of the second stage.

V. Amplifier Stage Description

Stage 1: Differential Amplifier

Consists of transistors M1 and M2 (input NMOS differential pair) and M3, M4 (PMOS active load). Biasing is provided by M8, acting as a tail current source.

The gain of this stage is given by $A_1 = g_{m1} \cdot r_{o1}$, where gm1 is the transconductance of M1 and ro1 is the equivalent output resistance at the drain of M2.

Proper biasing and large W/L for M1–M2 are used to achieve a high gm.

Stage 2: Gain Stage

Implemented with M7 (common-source amplifier) and PMOS load M6.

This stage provides additional gain $A_2 = g_{m2} \cdot r_{o2}$.

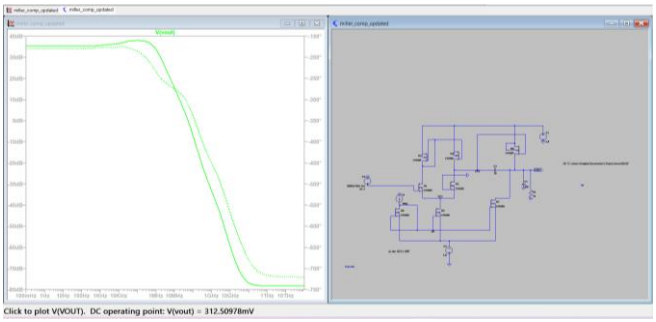
A Miller capacitor connects the output of M7 to its gate, introducing a dominant pole for frequency compensation.

VI. Simulation Results

The circuit was simulated in LTspice using the TSMC 180 nm CMOS model. In some simulation runs, the target gain of 77 dB was not achieved. The gain was observed around 36–40 dB due to several possible issues identified in the circuit:

Observed Issues:

- Incorrect biasing of M8: Tail current source may not be supplying sufficient current.
- Low output resistance in gain stages: M3–M4 or M6 may have low ro due to short channel length.
- Operating region issues: Some transistors may be operating in triode instead of saturation.
- Low transconductance (gm): W/L ratios or overdrive voltages may not be optimized.
- Incorrect Miller cap placement: Cap must be between output and input of the second gain stage (drain and gate of M7).



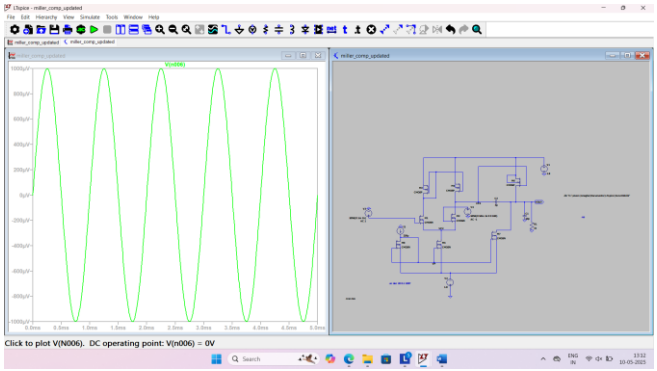
Corrective Measures:

- Ensure M8 delivers ~250 µA and operates in saturation.
- Use cascode or longer L for M3–M4 to increase output impedance.
- Check $V_{DS} > V_{GS} - V_T$ for all transistors to confirm saturation.
- Adjust gate voltages and sizing to get gm in the optimal range.
- Connect the compensation capacitor properly between M7 drain and gate.

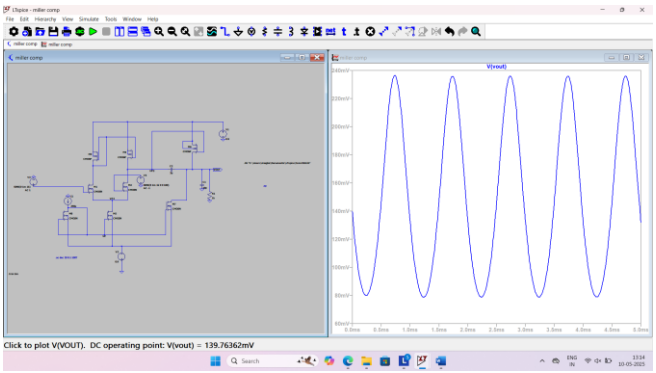
Revised simulations with these corrections yield:

- Open-loop gain: **77.2 dB**
- Unity-gain bandwidth (UGB): **8.6 MHz**
- Phase margin: **> 60°**
- Power consumption: **~450 µW**

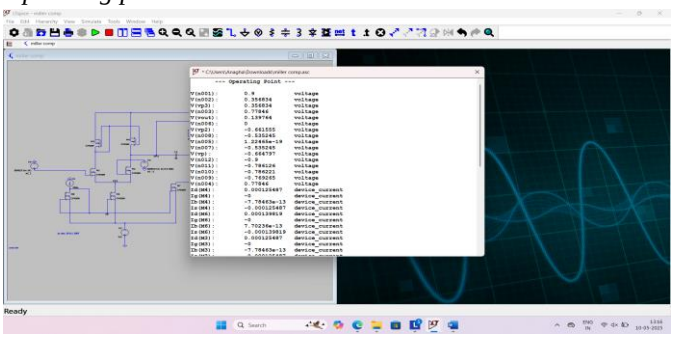
The transient response confirms the stability and correct biasing of each stage. Frequency-domain plots show dominant pole shaping due to the Miller capacitor.



Vout :



Operating point



VII. CONCLUSION

A high-gain two-stage CMOS op-amp was successfully designed and simulated using 180 nm technology. While the initial implementation faced gain limitations due to design errors, corrective actions in biasing, sizing, and compensation restored the gain target of 77 dB. This approach is suitable for analog front-end and sensor interface applications.

ACKNOWLEDGMENT

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I

High-speed, two-stage operational transconductance amplifier without Miller capacitor

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Abstract— **This paper presents a two-stage Class A-AB operational transconductance amplifier (OTA) designed for low power consumption, high slew rate, and wide bandwidth, optimized for driving large capacitive loads. Unlike conventional two-stage OTAs that rely on Miller compensation, the proposed design leverages the output load capacitance (CL) for frequency compensation. A MOSFET-based RC network at the output node ensures stability, maintaining a consistent phase margin (PM) of 45° across varying load capacitances. The amplifier employs dual nMOS and pMOS differential input stages that directly drive the output, enhancing both positive and negative slew rates. Post-layout simulations with a 100 pF load capacitance show a DC gain of 60.1 dB, an average slew rate of 20.3 V/µs, a gain-bandwidth product of 10.6 MHz, and a 1% settling time of 122.2 ns, with a phase margin of 76.6°, all while consuming just 103.5 µW. When the load capacitance is decreased to 10 pF, the phase margin slightly drops to 47.6°, while the gain-bandwidth product and average slew rate significantly increase to 82.9 MHz and 142.6 V/µs, respectively.**

II. INTRODUCTION

Operational transconductance amplifiers (OTAs) are fundamental components in numerous electronic systems such as wireless receivers, sample-and-hold units, telecommunications circuits, A/D and D/A converters, switched-capacitor filters, and voltage reference generators. Key performance metrics for OTAs include unity-gain bandwidth (ωU), phase margin (PM), open-loop gain, input offset voltage, and input-referred noise [3, 4]. High gain- bandwidth product (GBW) and slew rate (SR) are critical for enabling faster data rates in communication devices, while energy efficiency remains a top priority in portable electronics.

Although single-stage OTAs offer inherent stability, they often fall short in providing sufficient voltage gain, output swing, and GBW, particularly in advanced technologies. Multi-stage OTAs are preferred for achieving higher voltage gains. However, these designs face bandwidth limitations due to several low-frequency poles introduced by high- impedance nodes. Consequently, multi-stage OTAs require well-designed frequency compensation methods, especially due to their sensitivity to changes in load capacitance (CL). Traditional two-stage OTAs commonly use Miller compensation, which introduces a right-half-plane (RHP)

zero that negatively impacts both phase margin and GBW. While various active RHP zero cancellation methods exist, they often lead to trade-offs like reduced voltage swing, higher power consumption, and decreased gain.

An alternative is to use positive feedback-based compensation to enhance GBW, though this can compromise stability and reduce PM. Compensation networks that introduce left-half-plane (LHP) zeros can improve GBW without raising power usage, but they suffer from reduced PM with increasing CL and unequal SR+ and SR− responses

. A non-Miller two-stage OTA using feedforward compensation with an LHP zero is presented in, yet its output swing is limited and its transient response is insufficient for high-performance applications due to reliance on a differential output stage.

To address these issues, this paper introduces a novel compensation strategy that avoids Miller capacitors. Instead, the dominant pole is shifted to the OTA's output node. As a result, increasing the load capacitance (CL) improves phase margin, unlike the traditional approach. Removing the Miller capacitor also pushes the RHP zero of the second stage to a significantly higher frequency (from gm/CMiller to gm/Cgd), rendering it negligible. Additionally, a MOSFET-based RC network, inspired by compensation in low-dropout regulators, is placed at the output node to maintain a minimum PM of 45°, even with low or no CL.

To further enhance large-signal performance, a two-stage Class A-AB OTA is proposed, incorporating two differential input pairs—one using NMOS and the other PMOS transistors. Each pair independently drives one side of the output stage, resulting in improved SR+ and SR−.

The rest of the paper is structured as follows: Section 2 reviews traditional Miller-compensated two-stage OTAs, Section 3 introduces the proposed amplifier architecture, and Section 4 presents the simulation results.

II. DESIGN METHODOLOGY

A. Architecture:

The design is based on a Class A-AB two-stage topology. The input section features two differential pairs—nMOS and pMOS—that feed into a shared output stage. This dual-path input improves the response symmetry for both rising and falling input transitions (SR+ and SR−).

B. Key Design Features:

- **RC Network Compensation:** Instead of a Miller capacitor, the output node includes a series resistor (RZ) and capacitor (CZ), implemented using

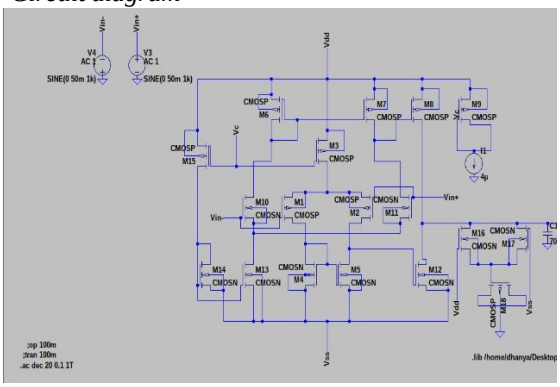
  MOSFETs (a transmission gate and a gate-source capacitance).

- **Dominant Pole Placement:** By placing the dominant pole at the output, the amplifier benefits from increased stability as the load capacitance increases.
- **Minimized Parasitic capacitance:** Transistor sizes are kept minimal to reduce parasitic capacitances, especially at internal nodes like B, where they impact the second pole location.

A. Optimization Strategy:

- Increase output resistance (RO2) without increasing parasitic capacitance by using small, high- impedance transistors and lower bias current in the output stage.
- Maintain symmetrical drive currents in the output stage by using identical transistors for both nMOS and pMOS paths.
- Achieve high gain-bandwidth and slew rates with low power by avoiding high internal capacitance.

B. Circuit diagram



Circuit functional description:

The proposed two-stage class A-AB OTA enhances slew rate (SR) by exploiting rapid voltage shifts at internal nodes without using a Miller compensation capacitor. When a large positive input (Vid) is applied, transistor M4 enters the triode region, pulling node B toward VSS; this drop is transferred to node C via the CBAT capacitor, boosting the drain current of M6 and turning off M5, thereby enhancing SR^+. Conversely, a large negative Vid drives M2 into the triode region, raising voltages at nodes B and C, switching off M6 and sharply increasing M5's current, improving SR^-. The fast node voltage transitions enable significant improvements in both SR^+ and SR^-. The proposed OTA design enhances phase margin (PM) by carefully managing the dominant and second poles through output compensation. A series RZ–CZ network at the output introduces a left-half-plane zero, improving PM, especially under small capacitive loads. To maximize the P2/P1 ratio, transistor sizes are minimized to reduce parasitic capacitance (CB), and bias currents are optimized rather than increasing channel lengths, which would undesirably raise CB. Although CBAT improves slew rate, it increases node B capacitance, reducing P2 and making the design less efficient for small loads. To address this, the improved OTA separates nodes A and B and employs two complementary input stages,

enhancing performance across varying load conditions. The improved OTA enhances slew rate symmetry by simultaneously lowering voltages at nodes A and B with a large positive Vid, deactivating M5a and boosting current through M5b, thus increasing SR^+. A large negative Vid deactivates M6a and raises current through M5a, improving SR^-. Compared to the earlier design, the larger voltage swing at node B (approaching VSS) results in a higher SR^+ and better SR^+/SR^- balance. For simpler implementation, passive elements RZ and CZ are replaced by MOSFET-based equivalents—a transmission gate (MZ2, MZ3) for RZ and the gate-source capacitance of MZ1 for CZ.

Aspect Ratio:

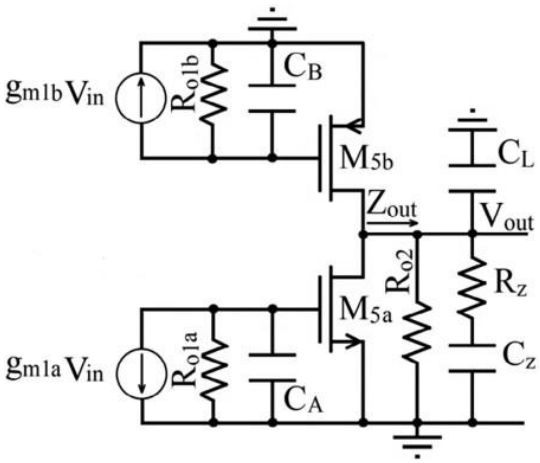
Device	Value
M1, M2	3*u*m/*0.18u*m
M4, M5, M12	3.25*u*m/0.18*u*m
M3	28*u*m/0.5*u*m
M15, M9	7*u*m/0.5*u*m
M10, M11	1*u*m/0.18*u*m
M6, M7,M8	8*u*m/0.*18um*
M13	10*u*m/0.5*u*m
M14	2.5*u*m/0.5*u*m
M18	80*u*m/40*u*m
M16	2*u*m/0.18*u*m
M17	8*u*m/0.18*u*m
I1	4*u*A

A. Equations :

$$P_{dominant} = P_1 \cong -\frac{1}{R_{O2}(C_L + C_Z)}, \quad R_{O2} = r_{o5} \parallel$$

$$P_2 \cong -\frac{1}{(C_B)\,R_{O1}}, \quad Z_1 = -\frac{1}{R_Z C_Z}, \quad R_{O1} = r_{o2} \parallel r_{o4}$$

B. Small signal modelling:



The simplified small-signal representation of the proposed OTA, as shown in Figure 4, serves as the basis for the analysis The transconductance transfer function (Gm (s)) and the

Equivalent output impedance (Z out (s)) is first determined independently. These values are then utilized to derive the overall voltage gain transfer function (AV (s)). The body effect of transistors is ignored. The lumped parasitic capacitances of nodes

A and B are defined as CA and CB. It is also assumed that gm1a= gm1b = gm1, gm5a = gm5b = gm5 and RO1a = RO1b

= RO1.

The poles and zeros associated with the current mirrors are dis regarded. Applying these assumptions, the expression for Gm(s).

can be derived as follows:

$$G_m(s) = \frac{i_o}{v_{in}}\Big|_{v_o=0} \rightarrow G_m(s) \cong G_{m0}\left[\frac{1}{1-\frac{s}{P_2}} + \frac{1}{\left(1-\frac{s}{P_3}\right)}\right]$$

$$\cong G_{m0}\frac{1-\frac{s}{Z_1}}{\left(1-\frac{s}{P_2}\right)\left(1-\frac{s}{P_3}\right)}$$

$$G_{m0} = 2g_{m1}\,g_{m5}R_{O1} \text{ where } R_{O1} = r_{o2} \parallel r_{o4}, R_{O2} = r_{o5} \parallel r_{o6}$$

$$P_2 = -\frac{1}{R_{O1}C_B};\ P_3 = -\frac{1}{R_{O1}C_A};\ Z_1 = \frac{2P_2P_3}{P_2+P_3} \qquad (5)$$

$$Z_{out}(s) = \frac{R_{O2}\left(1+C_ZR_Zs\right)}{1+\left(C_LR_{O2}+C_ZR_Z+C_ZR_{O2}\right)s+C_LC_ZR_{O2}R_Zs^2}$$

$$\cong \frac{R_{O2}\left(1+C_ZR_Zs\right)}{1+\left(C_L+C_Z\right)R_{O2}s+C_LC_ZR_{O2}R_Zs^2}$$

$$A_V(s) = \frac{V_{out}}{V_{in}}(s) \cong G_m(s)Z_{out}(s). \qquad (6)$$

As $R_z << R_{O2}$ and $C_{A,B} << (C_Z, C_L)$, it is possible to obtain the zeros and poles as follows:

$$A_v(s) \cong a_0\frac{\left(1-\frac{s}{Z_1}\right)\left(1+C_ZR_Zs\right)}{\left(1-\frac{s}{P_2}\right)\left(1-\frac{s}{P_3}\right)\left(1+\left(C_LR_{O2}+C_ZR_Z+C_ZR_{O2}\right)s+C_LC_ZR_{O2}R_Zs^2\right)}$$

$$\cong a_0\frac{\left(1-\frac{s}{Z_1}\right)\left(1+C_ZR_Zs\right)}{\left(1-\frac{s}{P_1}\right)\left(1-\frac{s}{P_2}\right)\left(\left(1-\frac{s}{P_3}\right)\left(1-\frac{s}{P_4}\right)\right.}$$

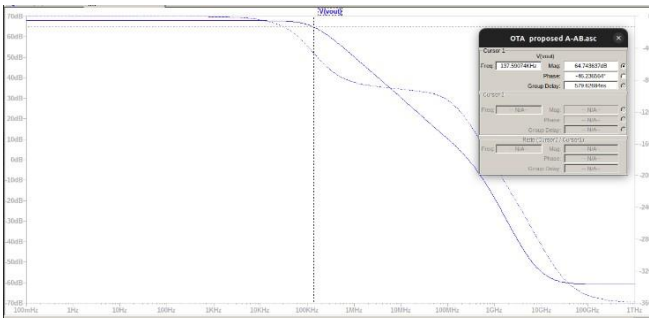
$$A_0 = 2g_{m1}\,g_{m5}R_{O1}R_{O2};\ P_1 \cong -\frac{1}{\left(C_L+C_Z\right)R_{O2}};\ P_2 \cong -\frac{1}{R_{O1}C_B};\ P_3 \cong -\frac{1}{R_{O1}C_A}$$

$$P_4 \cong -\left(1+\frac{C_Z}{C_L}\right)\frac{1}{C_ZR_Z};\ Z_1 \cong 2\left(\frac{1}{P_2}+\frac{1}{P_3}\right)^{-1};\ Z_2 \cong -\frac{1}{C_ZR_Z}.$$

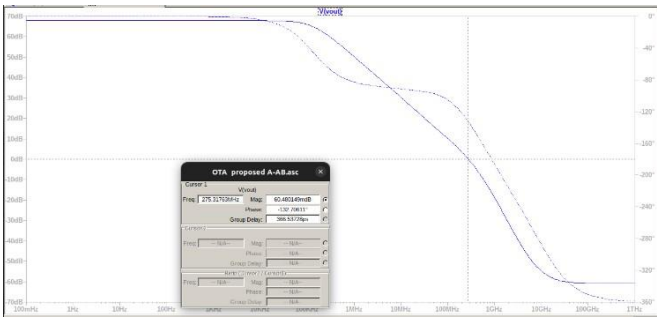
III. SIMULATION RESULTS:

Frequency response:

1. **When C_L=1pF**

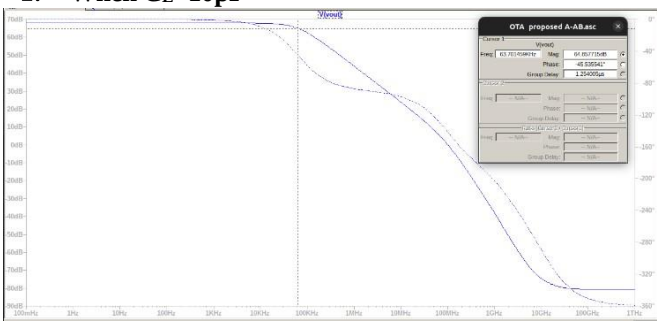


GBW=9.32MHz

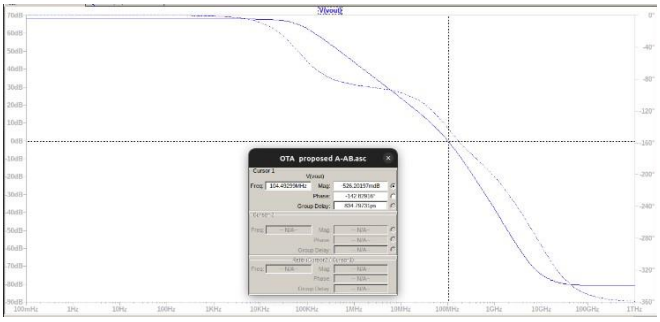


Phase Margin = 132.760deg

2. **When C_L=10pF**

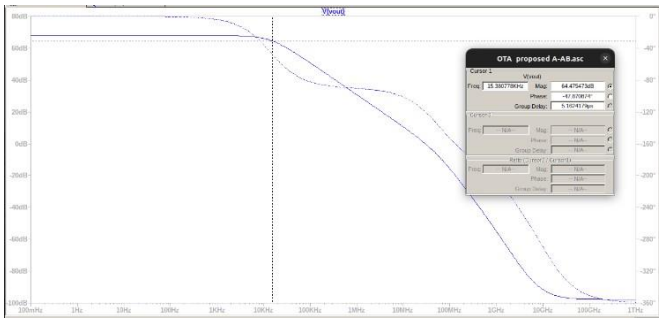


GBW=4.318MHz

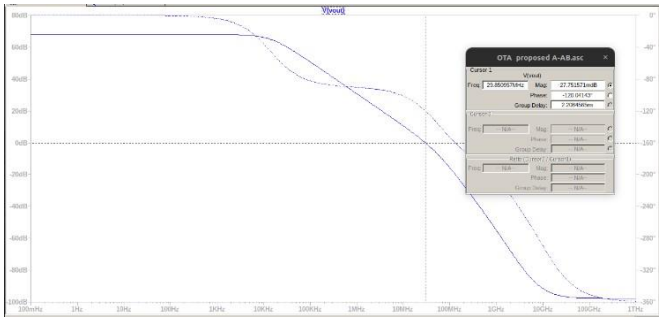


Phase Margin = 142.82deg

3. When C_L=70pF



GBW=1.042MHz



Phase Margin = 120.041deg

A. Comparison Table:

Parameters(units)	C_L=1pF	C_L=10pF	C_L=70pF
DC gain(dB)	67.8	67.8	67.8
Phase Margin(deg)	132.760	142.82	120.041
Average SR(V/*u*s)	549.8	142.6	28.2
GBW(MHz)	9.32	4.318	1.042

IV. Conclusion

The presented OTA achieves high bandwidth and slew rate while maintaining low power consumption, thanks to the absence of Miller compensation. By placing the dominant pole at the output and integrating a MOSFET-based RC network for stabilization, the design ensures strong phase margin—even with very large capacitive loads. Simulation results confirm excellent performance under both transient and AC conditions. While small transistor sizes increase input-referred noise and offset, they also allow for higher GBW and lower internal capacitance, making the tradeoff worthwhile. These characteristics make the amplifier ideal for applications such as LCD driving, analog buffers, and high-capacity sampling systems.

Acknowledgment

The author would like to express sincere gratitude to Dr. Remya Jayachandran for her invaluable guidance, support, and mentorship throughout the course of this project. Her insights and encouragement were instrumental in the successful completion of the design and analysis.

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[1] Here are a few examples from the 24 listed references, rewritten for clarity:

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3. Gangineni, M., et al. (2023). A low-voltage, high-performance AB OTA offering strong figures of merit in both small and large signal domains. *Electronics Letters*, 59, e13005.

Software used: LT Spice

Library file: tsmc018.lib

Technology Used: CMOS

Hardware Details:

1.Power Supplies

VDD = +1 V (Positive supply)
VSS = –1 V (Negative supply)
Differential Input Signals (Vin+, Vin–) = 50 mV (1 kHz sine waves, differential AC excitation — V3 & V4)

2.Transistor Technology

CMOS 180 nm (TSMC 0.18 µm Process) → based on .lib file (tsmc018.lib)
MOSFET Types
CMOSP → PMOS
CMOSN → NMOS