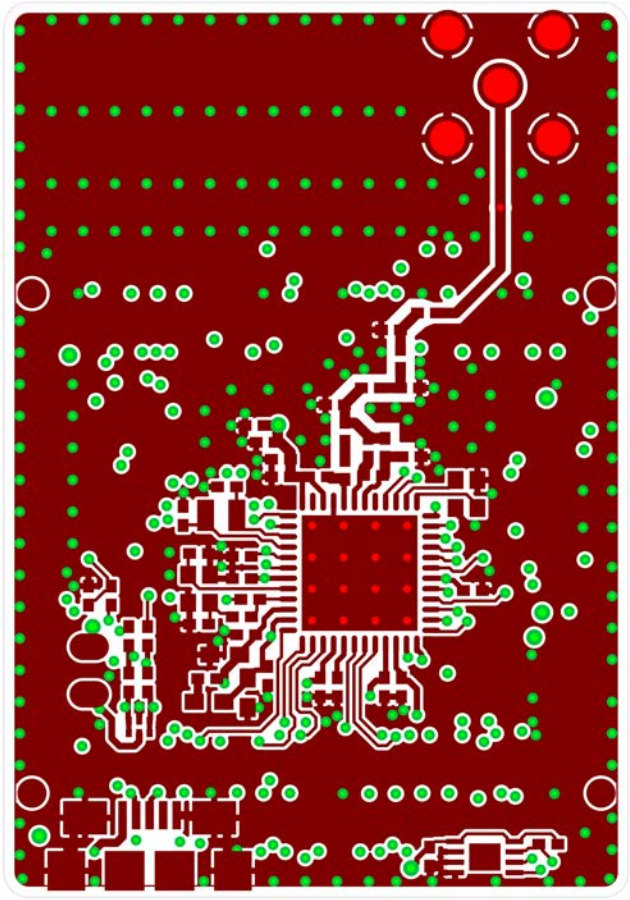
AN1005: EZR32 Layout Design Guide

The purpose of this application note is to help users design PCBs for EZR32 Wireless MCUs using best design practices that result in excellent RF performance. EZR32 wireless MCUs are based on the Si4455/Si446x radios but usually require slightly different matching network component values in order to achieve similar performance due to their different PCBs and package parasitics. The matching principles are similar to those for Si4455/Si446x devices and are described in detail in “AN693: Si4455 Low-Power PA Matching”, “AN627: Si4x6x and EZR32 Low-Power PA Matching”, and “AN648: Si4x6x and EZR32 High-Power PA Matching”.

RF performance and critical maximum peak voltage on the output pin are strongly dependant on the PCB layout as well as on the design of the matching networks. For optimal performance, Silicon Labs recommends the use of the PCB layout design hints described in this document.

KEY FEATURES

- Layout Guidelines
- Design Principles
- Summary Checklist



1. Design Recommendations for Using EZR32 Wireless MCUs

Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended that designers use the reference designs “as is” to minimize the detuning effects caused by parasitics or generated by poor component placement and PCB routing.

The compact RF part of the designs is highlighted by a blue frame, and it is strongly recommended to use the same framed RF layout in order to avoid any possibility of detuning effects. The figure below shows the framed compact RF part of the designs.

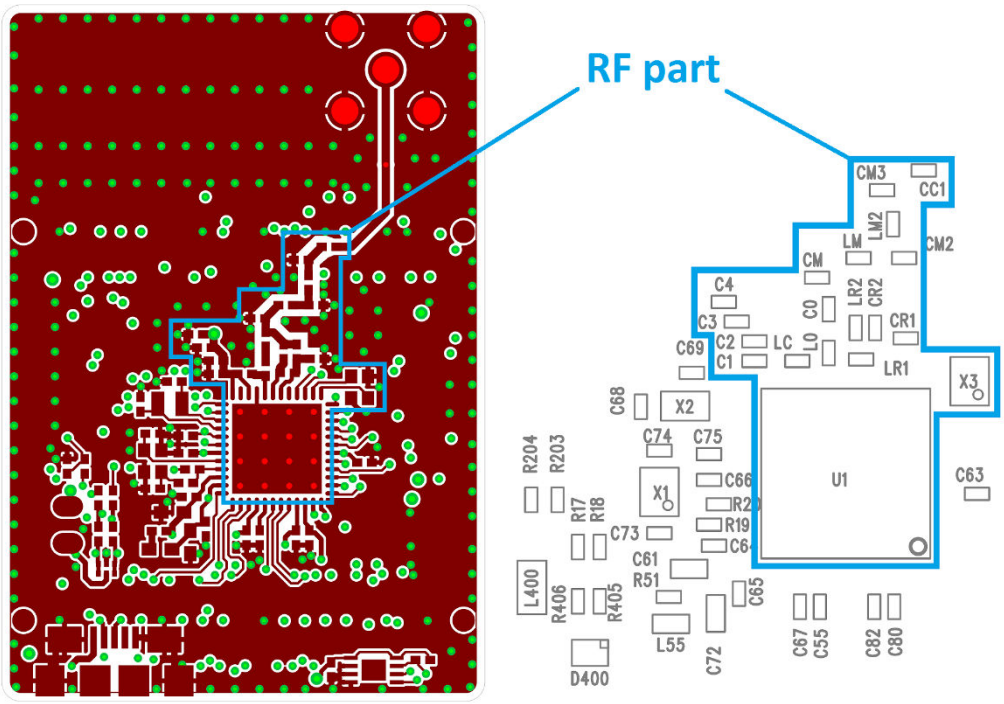


Figure 1.1. Compact RF Part of the Designs Highlighted on Top Silkscreen

The layout of the MCU VDD filtering capacitors should also be copied from the reference design as much as possible. When layouts cannot be followed as shown in the reference designs (due to PCB size and shape limitations), the layout design rules described in the following sections are recommended.

1.1 Matching Network Types and Layout Topologies for the EZR32 Wireless MCUs

The Si4455/Si446x-based EZR32 devices can use the following TX matching networks:

- **Class-E(CLE)**
- Switched-Current (SWC)
- **Square-Wave (SQW)**

From the above-listed matching network types, only the bolded ones, Class-E and Square-Wave, exist in EZR32 radio board format. Still, if one intends to use the Switched-Current match (or any other match that does not exist in the EZR32 format but does exist in the Si4455/Si446x format) with the EZR32 wireless MCU, the matching networks designed for the Si4455/Si446x can be used as a good starting point for EZR32. In most cases, fine tuning of the matching element values might be required.

The basic types of board layout configurations are as follows:

- Split TX/RX
- **Direct-tie**
- **Switched TX/RX**
- Diversity

In the Split TX/RX type, the TX and RX paths are separated, and individual SMA connectors are provided for each path. This type of board layout configuration is best suited to demonstrations of output power and sensitivity of Si4455/Si446x-based EZR32 wireless MCUs.

In the Direct-Tie type, the TX and RX paths are connected together directly, without any additional RF switch.

In the Switched TX/RX type, the boards contain a single antenna and a single-pole, double-throw (SPDT) RF switch to select between the TX and RX paths.

In the Diversity type, there are two antennas, both of which can be connected either to the TX or to the RX path by a double-pole, double-throw (DPDT) RF switch.

Of the board layout configurations listed above, only the bolded ones, Direct-tie and Switched TX/RX, exist in EZR32 radio board format. If a Split TX/RX board layout configuration is intended to be used with an EZR32 wireless MCU, the Split reference designs for the Si4455/Si446x provide a good starting point. In most cases, fine tuning of the matching element values will be required. If a Diversity solution is required for EZR32 and an EZR32 Switched TX/RX match exists for the same frequency using a radio with the same output power capability (refer to the data sheet of the radio), the Switched TX/RX matching network can be used for the Diversity application by using a DPDT switch instead of SPDT (additional harmonic filtering is necessary on both outputs of the DPDT switch).

2. Guidelines for Layout Design when Using the EZR32 Wireless MCUs

The typical power regime of the Si4461-based EZR32 wireless MCU is in the +13 to +16 dBm range, while the Si4455/60/67-based EZR32 is primarily devoted to the +10…+13 dBm applications. For these devices, the preferred matching types for the 315 to 950 MHz frequency range are CLE and the SWC. As discussed in 1.1 Matching Network Types and Layout Topologies for the EZR32 Wireless MCUs, an SWC matching network for EZR32 wireless MCUs does not exist in radio board format, but the SWC matching networks designed for the Si446x can be used as a good starting point for EZR32. The operating principles of CLE and SWC matching and the reference designs with element values are given in “AN627: Si4x6x and EZR32 Low-Power PA Matching”.

For versions of radio boards using the Si4463/68-based EZR32 wireless MCUs (for +16…20 dBm applications) with CLE Direct-tie or Switched TX/RX type matchings, general layout guidelines similar to those of the Si4455/60/61/67 based wireless MCUs (i.e., +10...+16 dBm PA) can be applied.

The layout issues of SQW matching will be discussed in this section as well. This type of matching can be used effectively when the required output power is high and the operating frequency is low (e.g. 169 MHz). The operating principles of these types and the reference designs with element values are given in “AN648: Si4x6x and EZR32 High-Power PA Matching”.

In the case of SQW type matching, it is necessary to pay closer attention to the shape and amplitude of the voltage waveform at the TX output pin of the device due to the increase in output power. Silicon Labs recommends the addition of a harmonic termination circuit (formed by the LH, CH, and RH components) placed in parallel shunt-to-GND configuration at the input of the low-pass filter. This harmonic termination circuit helps to maintain the desired voltage waveform at the TX output pin by providing a good impedance termination at very high harmonic frequencies. Refer to “AN648: Si4x6x and EZR32 High-Power PA Matching” for further details on this subject.

The following are some general rules for designing RF-related layouts for good RF performance:

- For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required.
- Use as much continuous ground plane metallization as possible. Avoid separation of the ground plane metallization.
- Use as many grounding vias (especially near the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
- Use a series of GND vias (i.e., “stitching vias”) along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than λ/10 of the 10th harmonic. This is required to reduce PCB radiation at higher harmonics caused by the fringing field of these edges.
- Avoid using long and/or thin transmission lines to connect the components. Otherwise, some detuning effects might occur due to distributed parasitic inductance.
- Try to avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
- Use tapered line between transmission lines with different widths (i.e., different impedances) to reduce internal reflections.
- Avoid using loops and long wires to obviate their resonances.
- Always ensure good VDD filtering by using bypass capacitors (especially at the range of the operating frequency).

2.1 Class-E, Direct-Tie Type Matching Network Layout Based on the BRD4542A Radio Board (Single Antenna without an RF Switch)

Examples shown in this section are based on the layout of the BRD4542A Radio Board. This board contains one antenna, while TX and RX paths are connected directly together, without the use of an RF switch.

The schematic of the CLE Direct-Tie type matching network for the Si4455/Si446x-based EZR32HG is shown in the figure below.

During TX mode operation, the built-in LNA protection circuit turns on (see “AN627: Si4x6x and EZR32 Low-Power PA Matching” for more details). In this case, the dc path from the output of the matching network to the LNA is not blocked through the RX side, so a dc blocking capacitor (CC1) is necessary.

With Direct-Tie type matching, coupling between the RX and TX sides is not critical since no harmonic leakage occurs through the coupled RX path. This is because both sides are filtered after the common connection point.

The main layout design concepts are reviewed throughout this layout to demonstrate the basic principles.

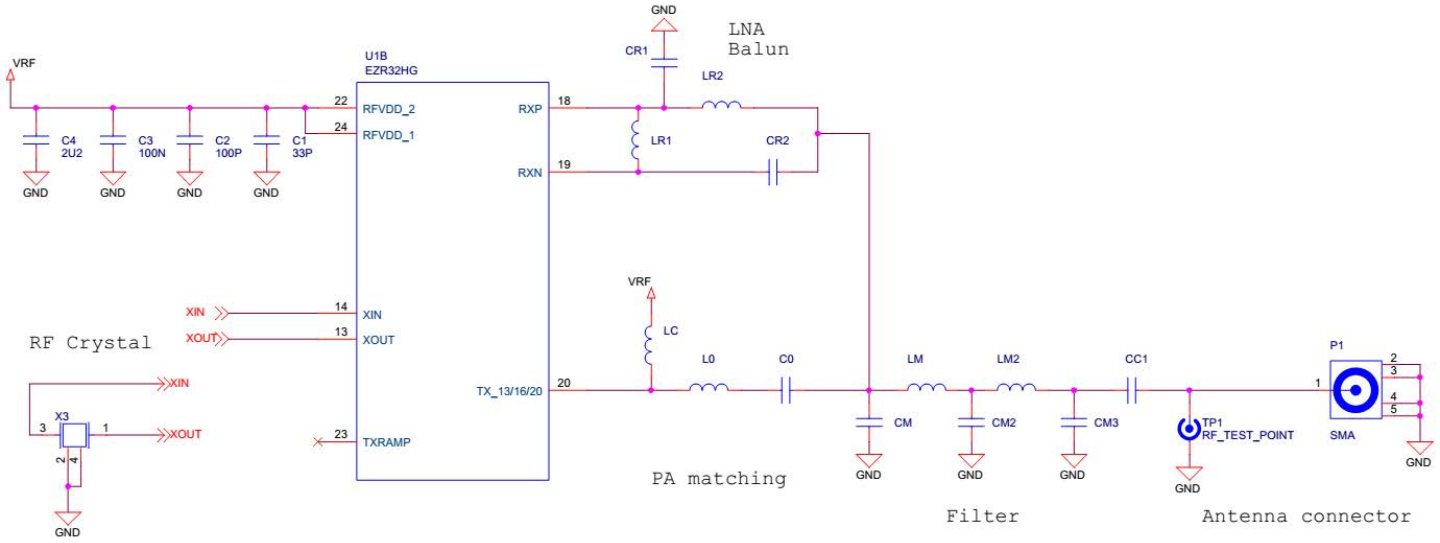


Figure 2.1. Schematic of RF Section for CLE Direct-Tie Type Matching Network for the Si4455/446x-Based EZR32HG

Note: Component values should be chosen based on radio type and frequency band. The EZR32HG has a smaller package and thus a different pinout than the EZR32LG/WG. For the correct pinout information, refer to the data sheet and reference designs.

The layout structure of the CLE Direct-Tie type matching network is shown in the figure below.

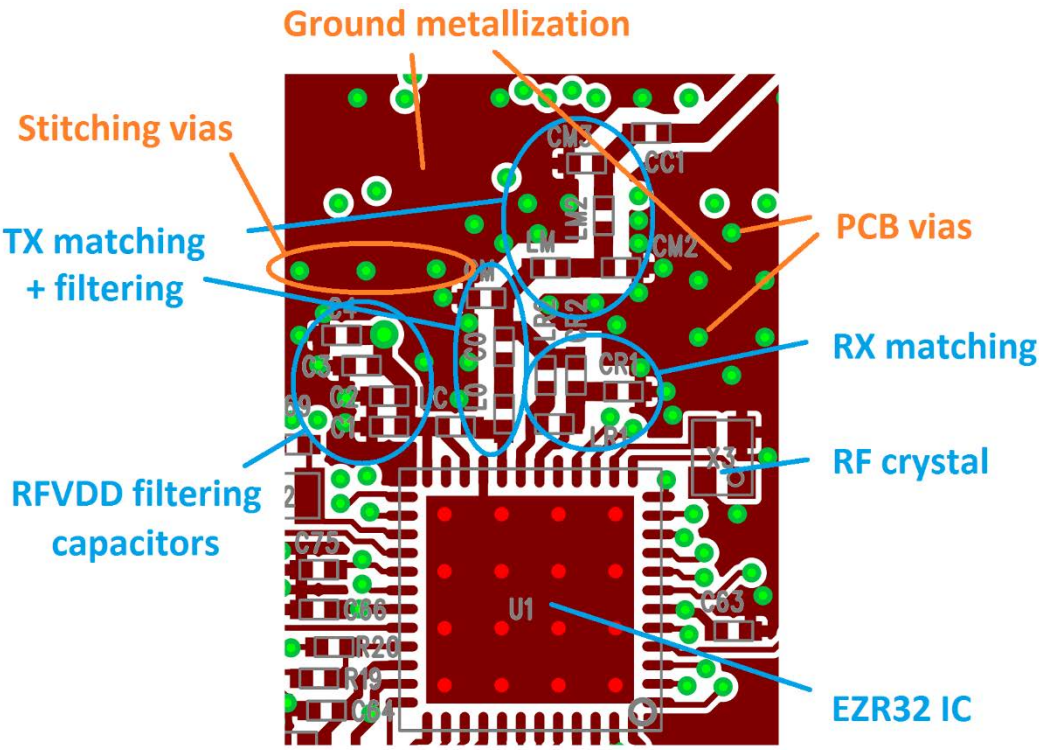


Figure 2.2. Layout of the RF Section for CLE Direct-Tie Type Matching Network for the Si4455/Si446x-Based EZR32HG

2.1.1 Layout Design Guidelines

- The L0 inductor should be placed as close to the TX pin of the EZR32 chip as possible (even if this means the RX is further away) in order to reduce the series parasitic inductance. This additional series parasitic inductance increases the voltage peak at the internal drain pin and detunes the matching network from its optimal form. The detuning of the TX matching network affects not only the TX performance but can cause significant RX sensitivity loss in Direct-tie configurations.
- The neighboring matching network components should be placed as close to each other as possible in order to minimize any PCB parasitic capacitances to ground and series parasitic inductances between components.
- The trace parasitics are critical in case of the connection of LR2, so the shortest traces possible should be used to connect LR2 to the TX side.
- Traces near the GND pins of the capacitors should be thickened to improve the grounding effect in the thermal straps. This minimizes series parasitic inductances between the ground pour and the GND pins. Additional vias placed close to the GND pins of capacitors connect them to the inner/bottom layer GND plane and serve to further reduce these effects.

The figure below demonstrates the positioning and orientation of LC, L0, and LR1 components and thermal strapping on the shunt capacitors on the BRD4542A Radio Board.

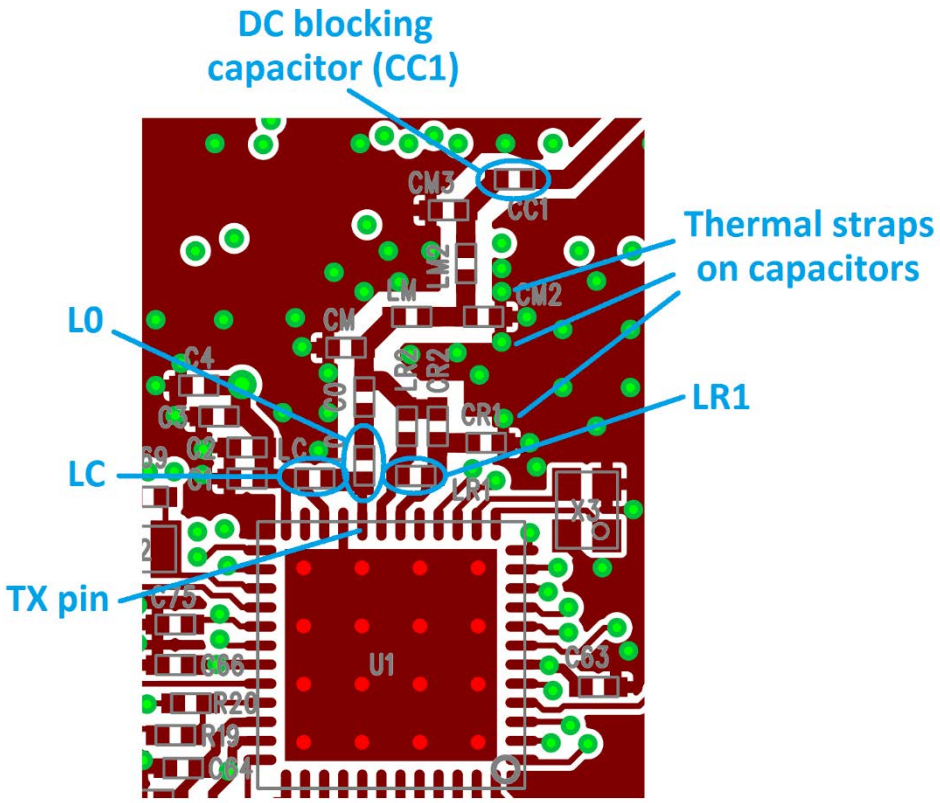


Figure 2.3. Component Orientation, Placement, and Thermal Straps

- The lower-value VDD bypass capacitors (C1 and C2) should be kept as close as possible to the RFVDD pins.
- To ensure good ground connection, all VDD filtering capacitors should use many vias close to their ground pins. It is also recommended that the GND return path between the GND vias of the VDD filtering capacitors and the GND vias of the RFIC paddle should not be blocked in any way; return currents should have a clear and unhindered pathway through the GND plane to the back of the RFIC.
- The exposed pad footprint for the paddle of the EZR32 IC should use as many vias as possible to ensure good grounding and heat sink capability. Due to the different package sizes, EZR32LG/WG reference designs use 25 exposed pad vias, while, for the EZR32HG reference layouts, 16 vias are applied.
- The crystal should be placed as close as possible to the XIN and XOUT pins of the EZR32 IC in order to minimize wire parasitic capacitances and any frequency offsets.
- Use at least 0.5 mm separation between traces/pads to the adjacent GND pour in the areas of the matching networks. This minimizes the parasitic capacitance and reduces detuning effects.
- If space allows, the nearby inductors of the matching network should be kept perpendicular to each other to reduce coupling between stages. This helps to improve filter attenuation at higher harmonic frequencies. The series filtering inductors can be placed one after another or perpendicular to each other.

- If space allows, the parallel inductor in the RX path (LR1) should be perpendicular to the nearby inductors in the TX path to reduce TX-to-RX coupling.
- Couplings through the ground can occur between nearby filtering capacitors (especially at high harmonics) and decrease the effectiveness of low-pass filtering, causing higher conducted and radiated harmonics. To avoid possible high harmonic levels, it is recommended to connect the nearby harmonic filtering capacitors to ground planes on different sides of the transmission line.

The following figure shows the grounding of the EZR32 IC, placement of the harmonic filtering capacitors, the crystal, and VDD filter capacitor positions on the BRD4542A Radio Board.

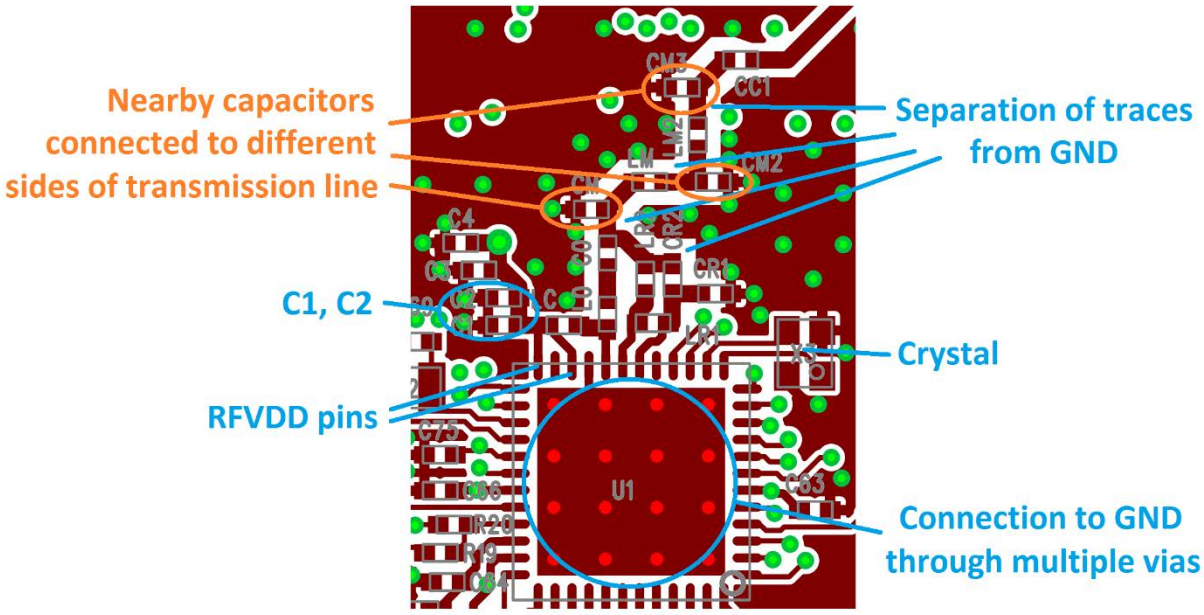


Figure 2.4. EZR32 IC GND Vias, VDD Filtering and Component Placement

- To achieve a good RF ground on the layout, it is recommended to add a large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering and provides a good ground plane for a monopole antenna. Gaps should ideally be filled with GND metal, and the resulting sections on the top, bottom, and inner layers should be connected with as many vias as possible.
- The area under the matching network (on the first inner layer) should be filled with ground metal as it will help reduce/remove radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX LPF/Match and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear unhindered pathway through the GND plane to the back of the RFIC.
- Use as many parallel grounding vias at the GND metal edges (especially at the edge of the PCB and along the VDD trace) as possible in order to reduce their harmonic radiation caused by the fringing field.
- If necessary, a shielding cap can be used to shield the harmonic radiation of the PCB; in that case, the shielding cap should cover all of the RF-related components. The shielding cap may be required based on output power level and the harmonic radiation limits of the regulatory standard that applies to the device.
- Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers (EZR32LG and EZR32WG radio boards are made on six-layer PCBs, while EZR32HG reference designs contain four PCB layers).
- Avoid placing the supply lines close to the PCB edge.

The ideal layer consistency for PCBs with more than two layers is as follows:

- Top layer: Use as much continuous solid GND metallization as possible with many vias.
- First inner layer: Use continuous, unified GND metallization beneath the RF part; wires can be routed beneath the non-RF parts if necessary.
- All other inner layers: Route as many (supply and digital) traces on these layers as possible.
- Bottom layer: This layer should be unified GND metal; route traces on this layer only if necessary.

The following figure illustrates layer consistency on the layout of the BRD4542A Radio Board.

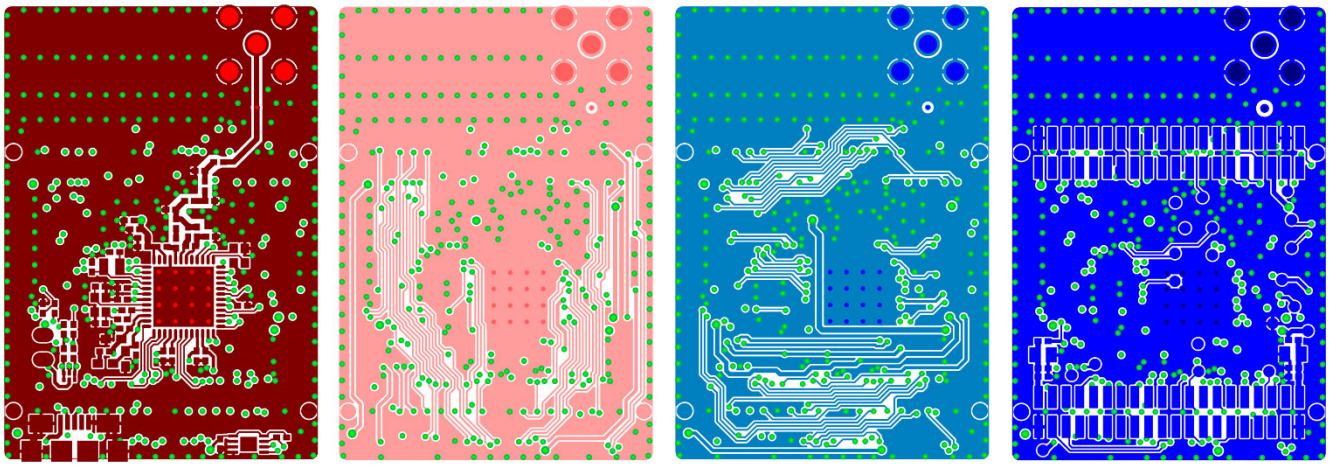


Figure 2.5. Layer Consistency on the Layout of BRD4502A Radio Board (Top, Inner 2, Inner 3, and Bottom, Respectively)

- To reduce sensitivity to PCB thickness variations, use 50 Ω grounded coplanar lines where possible for connecting the SMA connector to the matching network and/or the RF switch. This also reduces radiation and coupling effects. A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency.
- The interconnections between elements are not considered transmission lines since their lengths are much shorter than the wavelength, and, thus, their impedances are not critical. As a result, their recommended width is equal to the width of the pad of the applied components. In this way, reflections at pad-trace transitions can be prevented, and parasitic capacitances to ground can be minimized. For the BRD4542A Radio Board, the only route where a 50 Ω coplanar transmission line is used is between the output of the matching network and the SMA connector. Examples for the trace dimensions are shown in the table below.
- Use many vias near the coplanar lines in order to minimize radiation.

The following figure demonstrates the 50 Ω grounded coplanar line on the BRD4542A Radio Boards.

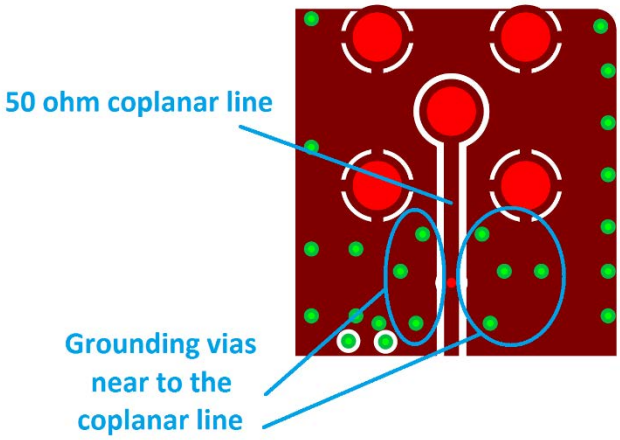


Figure 2.6. 50 Ω Grounded Coplanar Line on a 1.5 mm Thick 4-Layer Substrate

Table 2.1. Parameters for 50 Ω Grounded Coplanar Lines (4- and 6-Layers Calculation)[1]

Number of Layers	4-Layer	6-Layer
Frequency	142−1050 MHz	
T	0.018−0.035 mm	
ϵr	4.6	
H[2]	0.325 mm	0.304 mm
G	0.248 mm	0.39 mm
W	0.508 mm	0.508 mm

Note:
1. Different impedance calculators may yield slightly different results.
2. H is the distance between the top and the first inner layer.

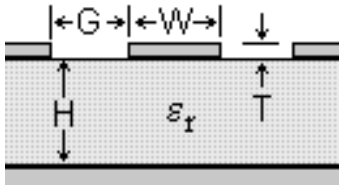


Figure 2.7. Grounded Coplanar Line Parameters

2.2 Class-E, Switched Type Matching Network Layout Based on the BRD4543A Radio Board (Single Antenna with RF Switch)

For reference, examples shown in this section are based on the layout of the BRD4543A Radio Board. This board contains a single antenna and an RF switch to select between the TX and RX paths. The schematic of the Switched type matching network for the EZR32HG is shown in the following figure.

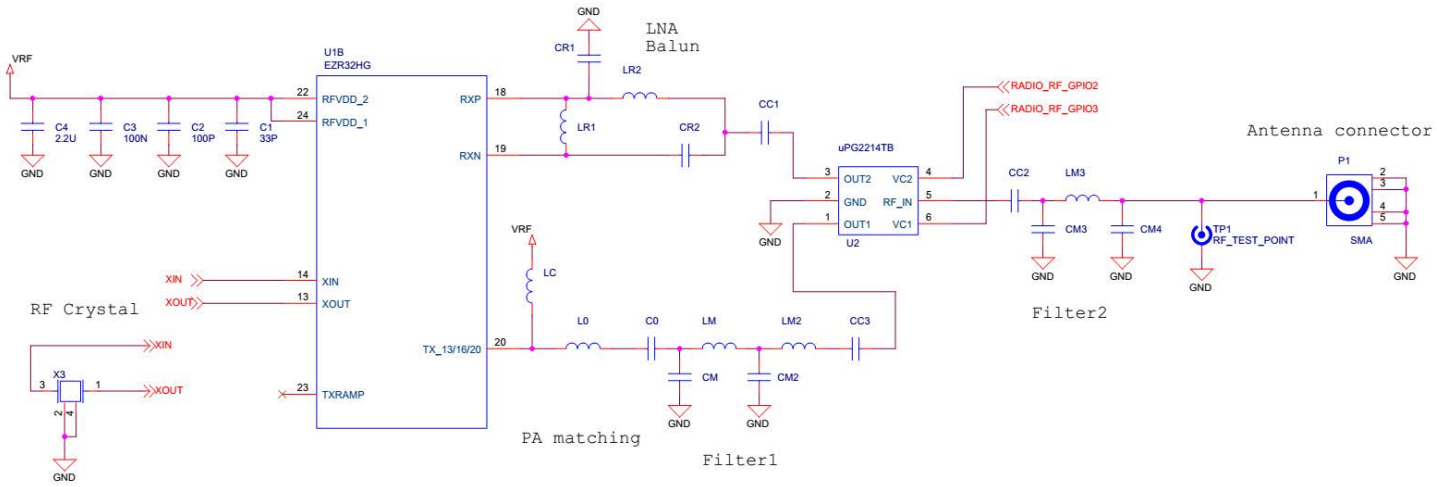


Figure 2.8. Schematic of the RF Section for CLE Switched Type Matching Network for the Si4455/Si446x-Based EZR32HG

Note: Component values should be chosen based on the radio type and frequency band. The EZR32HG has a smaller package and thus a different pinout than the EZR32LG/WG. For the correct pinout information, refer to the data sheet and reference designs.

2.2.1 Layout Design Guidelines

- When using a TX/RX switch or a switch to select antennas in an antenna diversity implementation, series capacitors may be required on all ports (e.g., TX, RX, Antenna) to block the dc path to the switch. Refer to the exact requirements and specifications of the switch used in the application.
- RF switches may behave in a slightly nonlinear fashion, resulting in some regeneration of harmonic energy, regardless of the cleanliness of the input signal to the switch. Thus, it may be necessary to move a portion of the TX low-pass filter after the RF switch (i.e., just prior to the antenna) in order to further attenuate these regenerated harmonic signals. In this way, the matching topology for the Single Antenna with RF Switch board configuration consists of two small low-pass filter sections with the RF switch embedded between them.
- If the RX side matching network is relatively far from the RF switch (the distance is more than λ/16 at the fundamental frequency), then the connecting trace should be a 50 Ω grounded coplanar line.
- It is recommended to add an isolating ground metal with many vias between the TX and RX matching.
- If one compares Figure 2.2 Layout of the RF Section for CLE Direct-Tie Type Matching Network for the Si4455/Si446x-Based EZR32HG on page 4 with the figure below, it can be seen that the choke inductor (LC) placement is different. For the Switched type layout, the choke inductor is placed between L0 and the TX pin. Although this additional pad and trace creates an extra series parasitic inductance for L0, its value (~0.3 nH) is commensurable with the component tolerance, and thus its effect on TX performance is negligible.

The following figure demonstrates the positioning and orientation of components and ground flooding on the BRD4543A Radio Board.

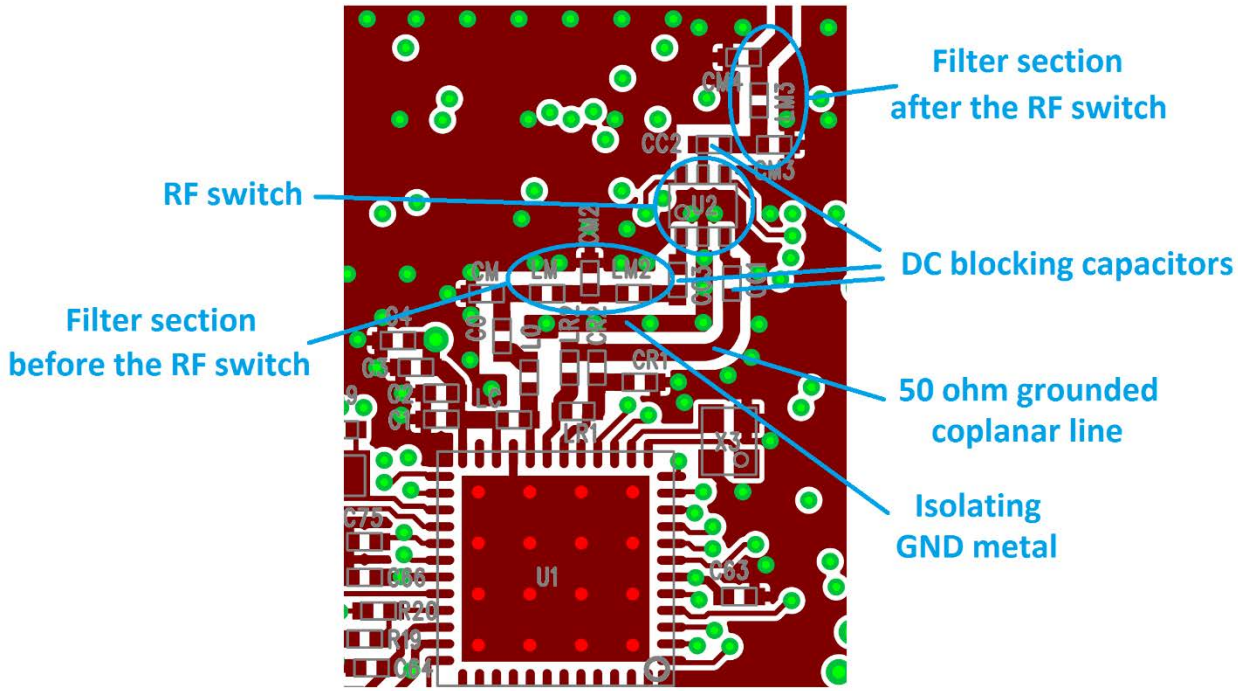


Figure 2.9. Layout of the RF Section for CLE Switched Type Matching Network for the Si4455/Si446x-Based EZR32HG

2.3 Square-Wave, Direct-Tie Type Matching Network Layout Based on the BRD4544A Radio Board (Single Antenna without RF Switch)

For reference, layout examples shown in this section are based on the layout of the BRD4544A Radio Board. This board contains one antenna, and the TX and RX paths are connected directly together without the use of an RF switch.

The schematic of the SQW Direct-Tie type matching network for the EZR32HG is shown in the figure below.

During TX mode operation, the built-in LNA protection circuit turns on (see “AN648: Si4x6x and EZR32 High-Power PA Matching” for more details). In this case, the dc path from the output of the matching network to the LNA is not blocked through the RX side, so a dc blocking capacitor (CC1) is necessary.

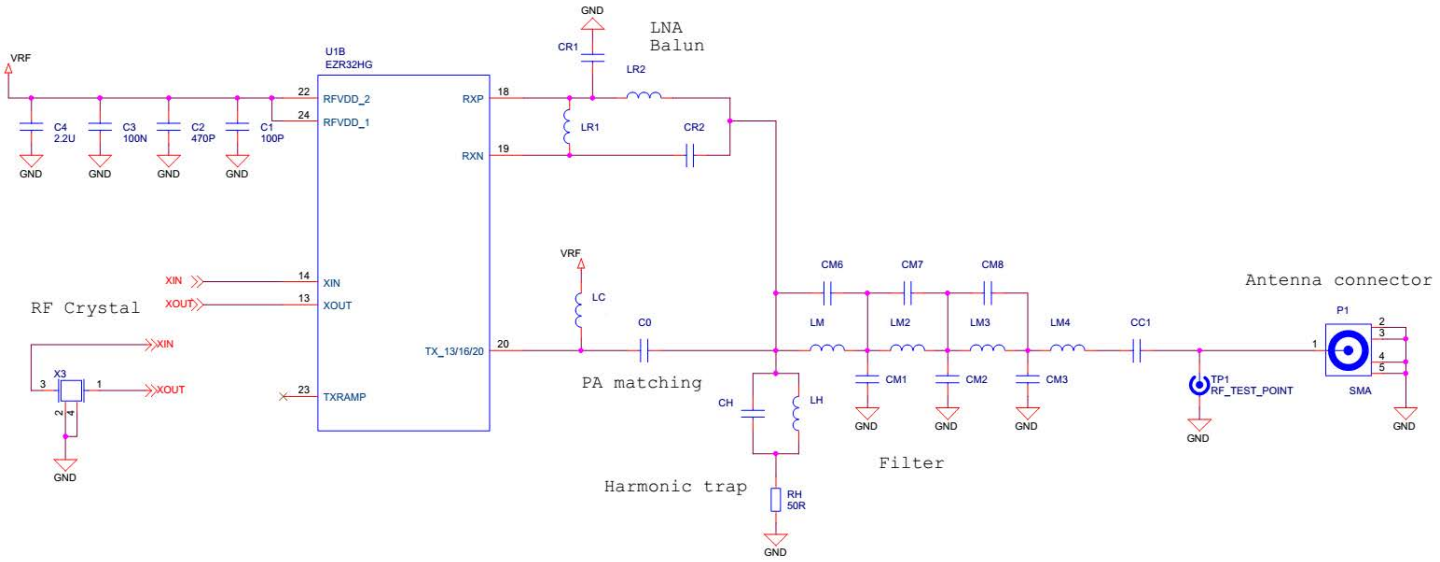


Figure 2.10. Schematic of the RF Section for SQW Direct-Tie Type Matching Network for the Si4455/Si446x-Based EZR32HG

Note: Component values should be chosen based on the frequency band. The EZR32HG has a smaller package and thus a different pinout than the EZR32LG/WG. For the correct pinout information, refer to the data sheet and reference designs.

2.3.1 Layout Design Guidelines

The following figure demonstrates the positioning and orientation of components on the BRD4544A Radio Board.

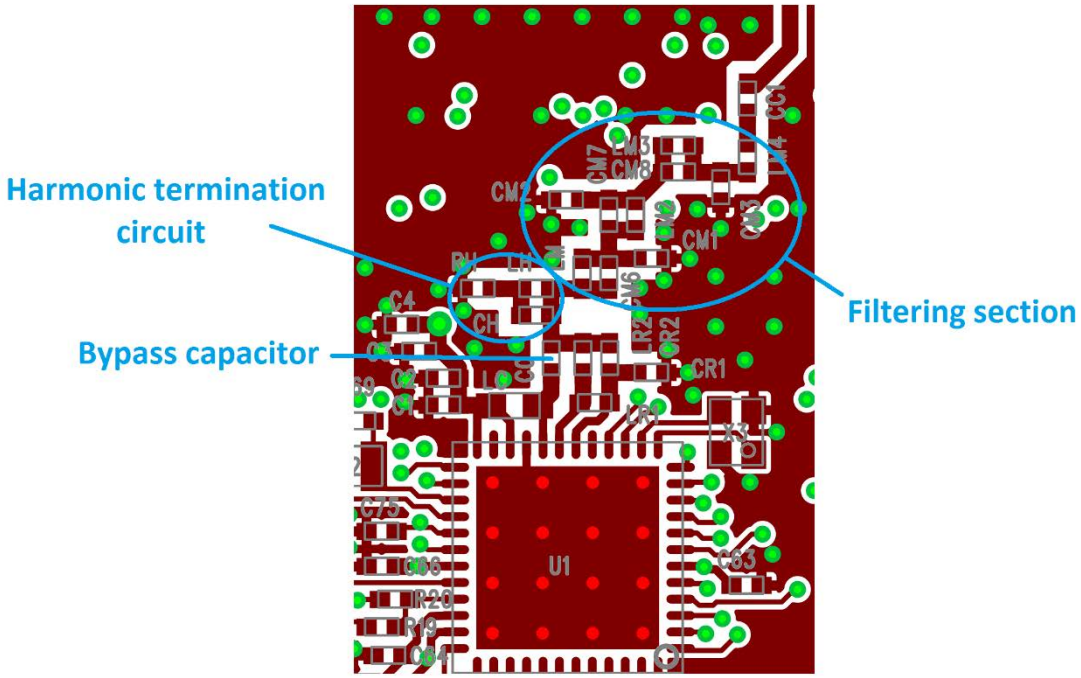


Figure 2.11. Layout of the RF Section for SQW Switched Type Matching Network for the Si4455/Si446x-Based EZR32HG

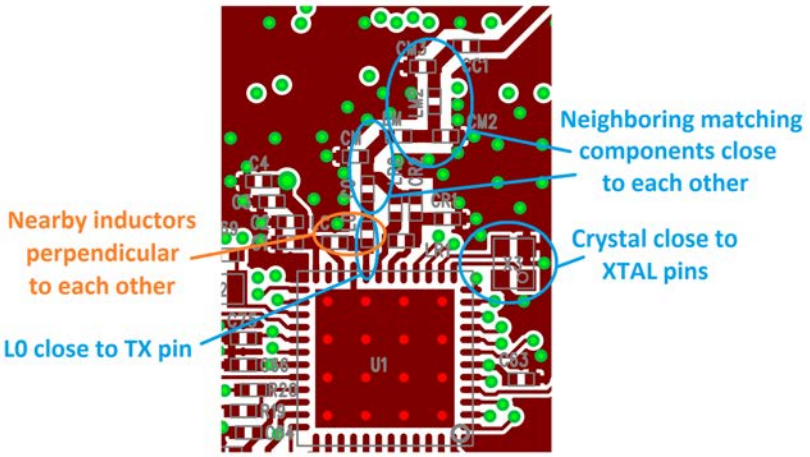
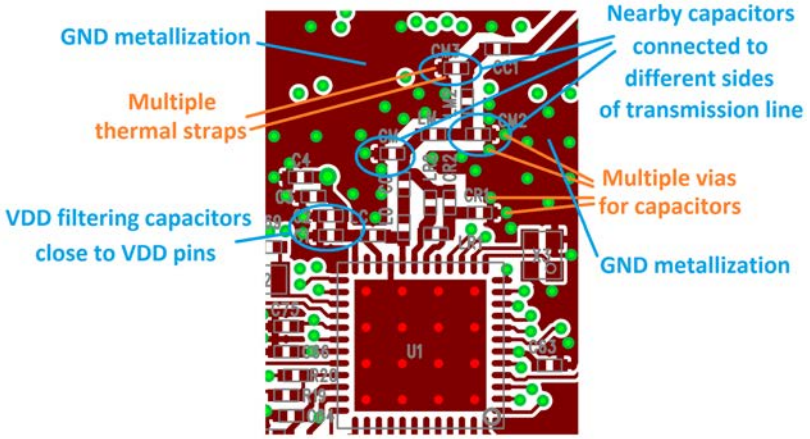
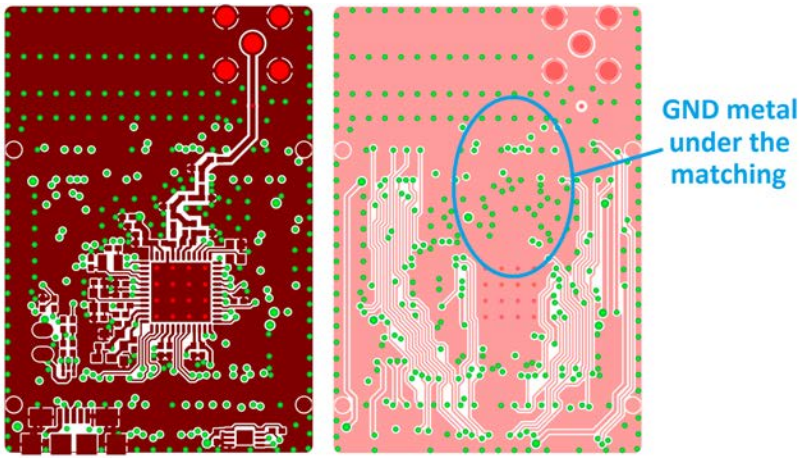
2.4 Further Design Recommendations when Using Additional RF Components

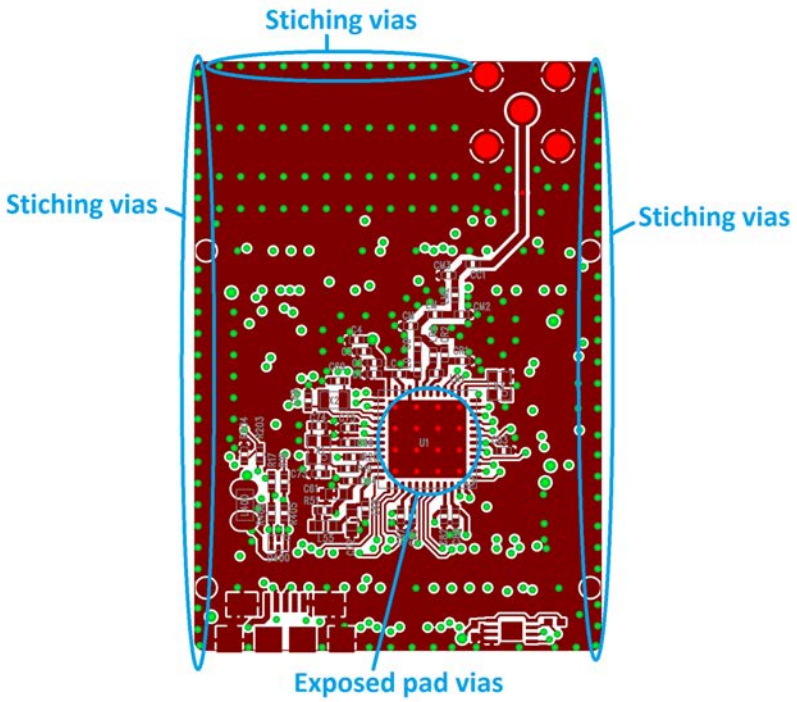
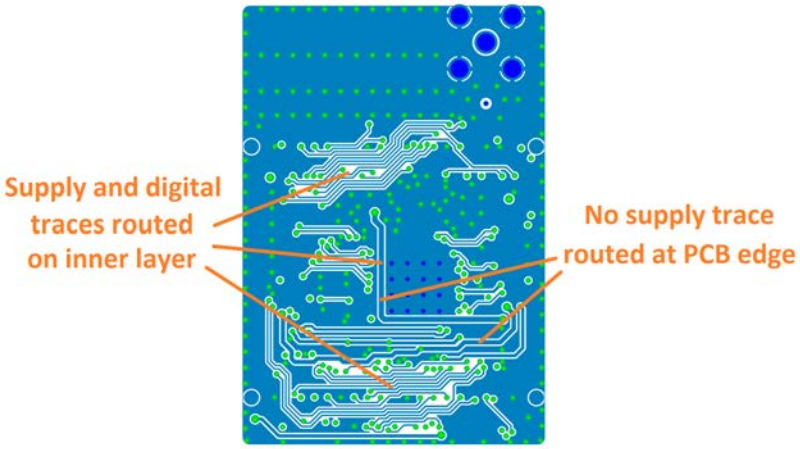
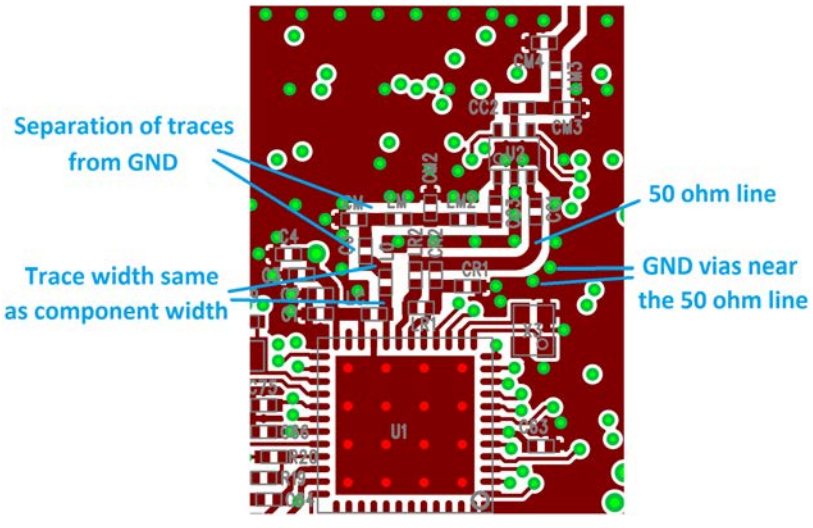
Although EZR32 radio board reference designs do not use additional components, such as FET, FEM, SAW filters, or TCXO, they can be applied in custom designs as they are for Si4455/Si446x devices. When using one of the EZRadioPro reference designs with an FET, FEM, or SAW filter for EZR32, slight modifications in the matching network component values might be necessary due to the different package parasitics and the different PCB parasitics (if the number of PCB layers differs).

In general, the extra components' data sheet includes the special layout design recommendations that should be taken into consideration in the layout design. For further layout design recommendations on FET, FEM, SAW filters, or TCXO usage (including layout design figures for Si4455/Si446x devices), please refer to Section 3.5, "Further Design Recommendations when Using Additional RF Components" in “AN629: Si4460/61/63/64/67/68 RF ICs Layout Design Guide”.

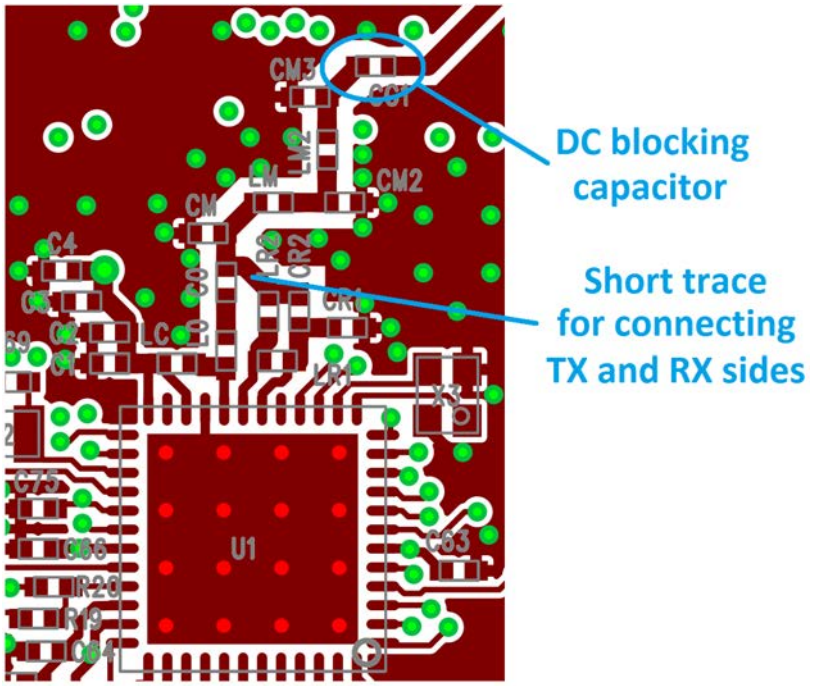
3. Checklist

3.1 Main Layout Design Principles

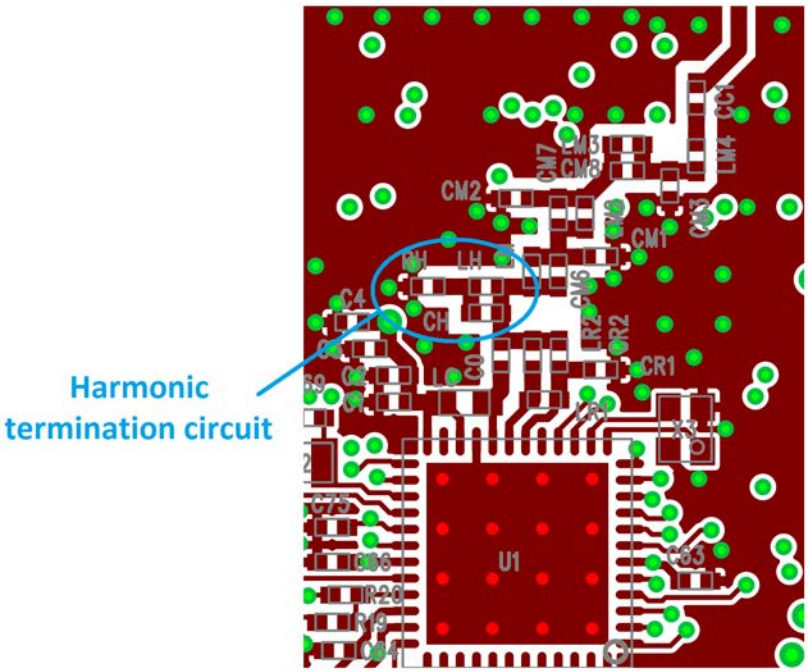
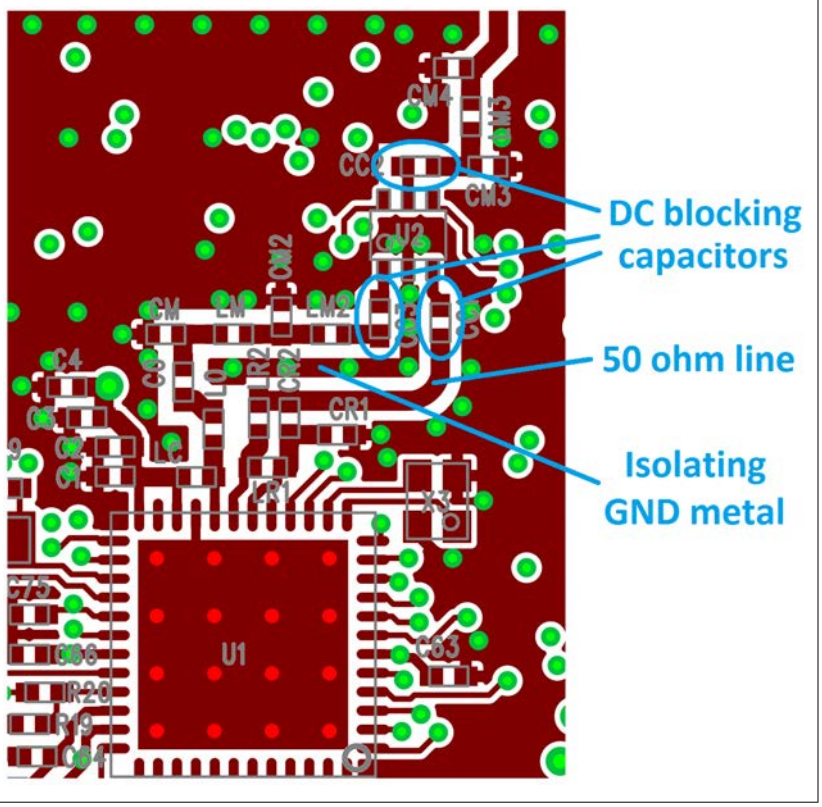
1.	☐	Is the first TX matching network component (L0) as close to the TX pin as possible?	
2.	☐	Are the neighboring matching network components as close to each other as possible?	
3.	☐	Is the crystal as close to the XTAL pins as possible?	
4.	☐	Are the nearby inductors perpendicular to each other?	
5.	☐	Are the smallest value VDD filtering capacitors kept close to the VDD pins of the EZR32 IC?	
6.	☐	Are the nearby harmonic filtering capacitors connected to ground planes on different sides of the transmission line?	
7.	☐	Are there multiple thermal straps used with shunt capacitors?	
8.	☐	Do the ground pins of the shunt capacitors use multiple vias?	
9.	☐	Is large, continuous GND metallization added to at least the RF section?	
10.	☐	Is the area on the first inner layer under the matching network filled with GND metal, and was wiring and routing avoided in this region?	

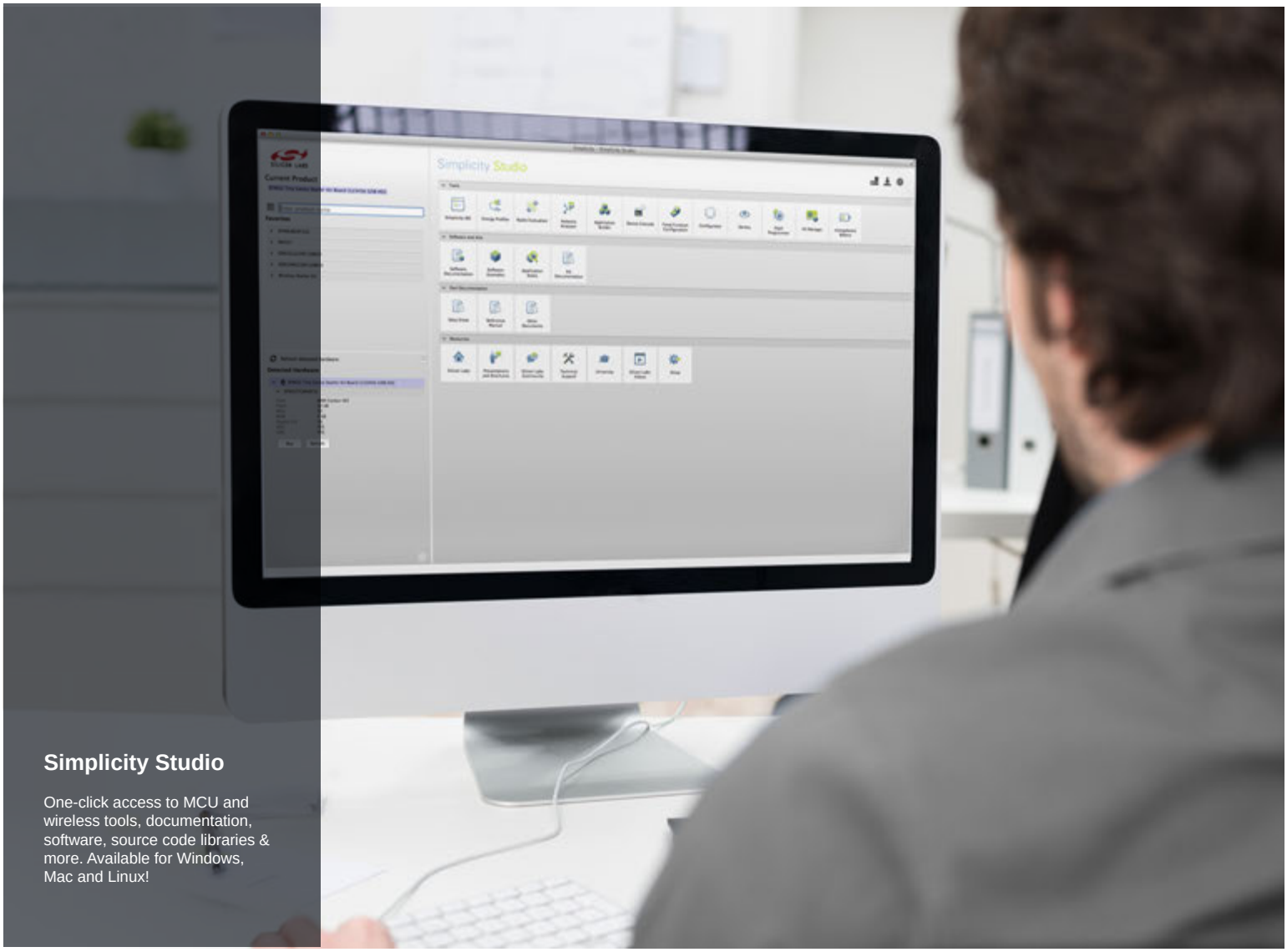
11.	☐	Does the exposed pad footprint use multiple vias?	
12.	☐	Are the GND metal edges closed by stitching vias where possible, with a via distance less than λ/10 of the highest (usually 10th) critical harmonic frequency?	
13.	☐	Is the number of PCB layers the same as in the reference design or, at a minimum, is the distance between the top and first inner layers similar?	
14.	☐	In case of PCBs with more than two layers, are supply and digital traces routed on inner layers?	
15.	☐	Is placing supply lines close to the PCB edge avoided?	
16.	☐	Is there at least 0.5 mm separation in the matching between the traces/ pads and the GND metal?	
17.	☐	Are 50 Ω grounded coplanar lines used for RF traces longer than λ/16 at the fundamental frequency?	
18.	☐	Are there vias at the ground metallization near the 50 Ω transmission lines?	
19.	☐	Is the trace width the same as pad width for connecting nearby components?	

3.2 Additional Concerns for Direct-Tie Type Matching

20.	☐	Is the length of the trace connecting the RX and TX sides minimal?	
21.	☐	Is an additional dc blocking capacitor added to the output of the matching network to block the dc path in RX mode?	

3.3 Additional Concerns for SQW and Switched Type Matching Networks

22.	☐	Is the additional harmonic termination circuit added into the TX path in case of SQW matching?	
23.	☐	Are series capacitors added to the TX/RX path to block the dc signal when a TX/RX switch (or Diversity switch) is used?	
24.	☐	Is a 50 Ω grounded coplanar line used to connect the RX side matching to the RF switch (if they are far from each other)?	
25.	☐	In case of Switched type matching, are the TX and RX separated by a ground metal on the top layer?	



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