THIS DRAWING HAD BEEN GENERATED AND IS MAINTAINED BY A CAD SYSTEM. CHANGES SHALL ONLY BE INCORPORATED AS DIRECTED BY THE GOVERNMENT DESIGN ACTIVITY

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	–			

NOTES:

1. INTERPRET DRAWING PER ASME Y14.100
2. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS VALUES ARE IN OHMS, CAPACITORS ARE MICROFARADS, INDUCTORS ARE MICROHENRIES.
3. ON & OFF SHEET CONNECTOR REPRESENT ORIGIN AND DESTINATION, NOT NECESSARILY THE DATA FLOW
4. CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY.

RED INTERFACE SCHEMATICS

INTERFACE	PAGE
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NEXT ASSY	USED ON
TTTTTTTTTT	JTT-X

APPLICATION

CONTRACT NO. TBD

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
NA NA NA

DO NOT SCALE DRAWING

MATERIAL

FINISH

DESIGN
CHECKED
DESIGN
ENGINEERING
PROJECT
QUALITY ASSURANCE
MANUFACTURING

DATE

ELECTRONIC SIGNATURES ON FILE

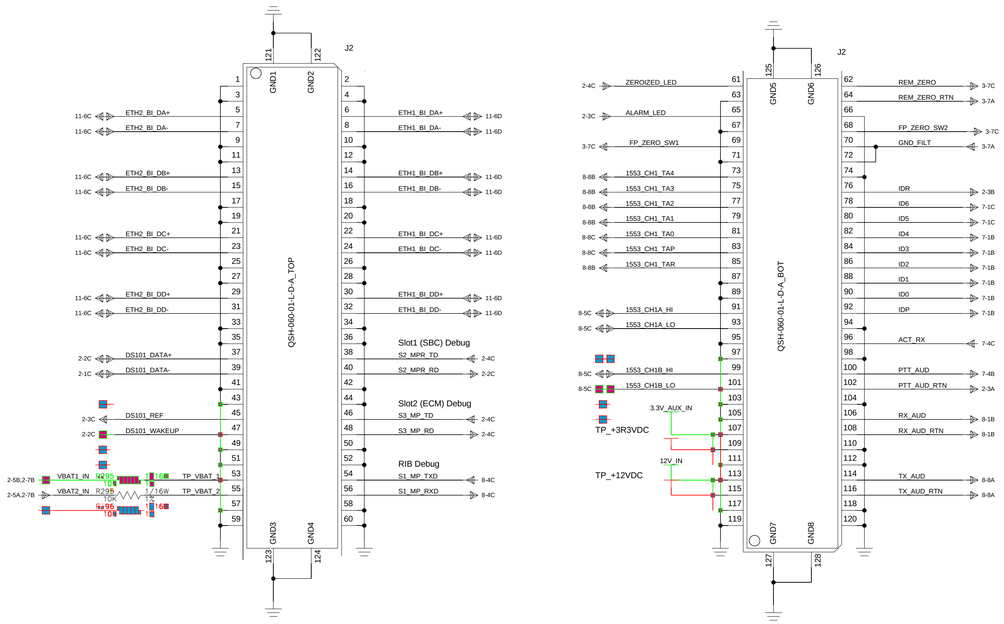
LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

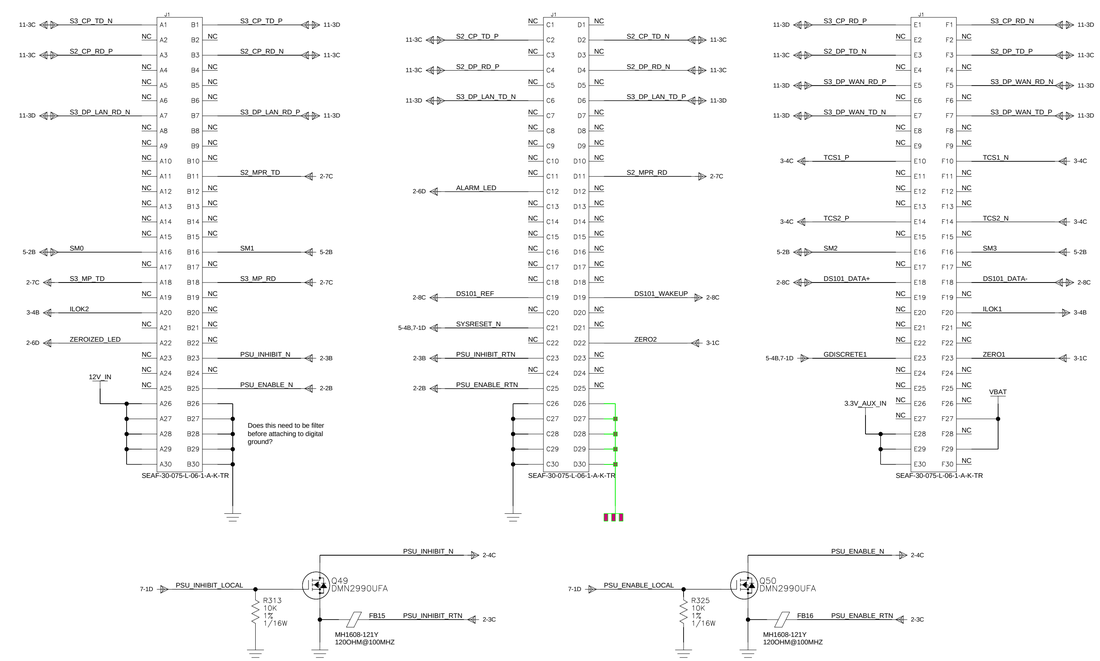
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE

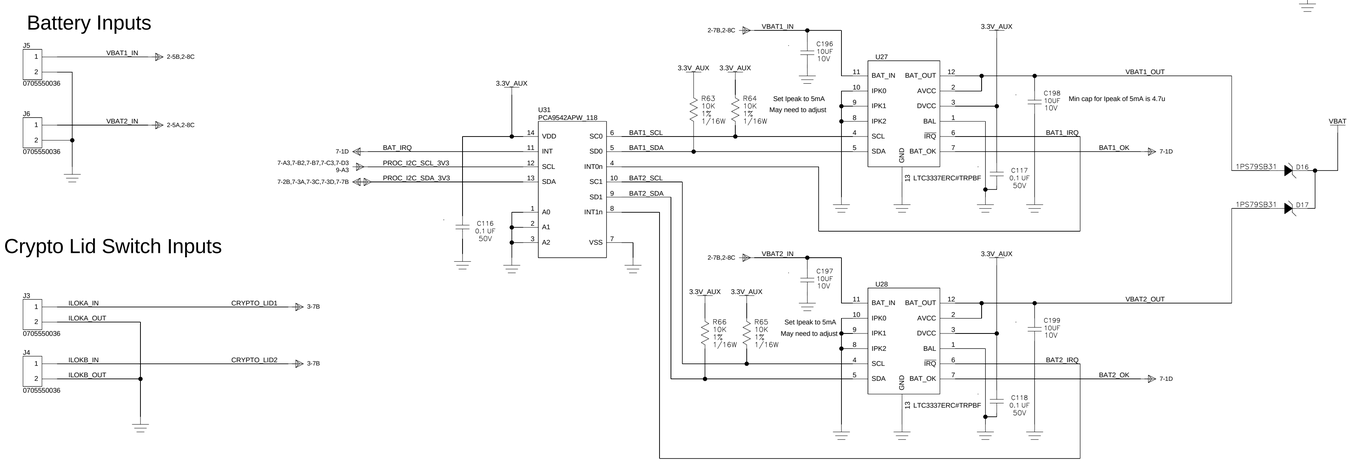
SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

FILE NAME 112302-01003 PADs 2.13 10/03/2025:09:22 SHEET 1 OF 11

PADs 2.13







IO Connectors

LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

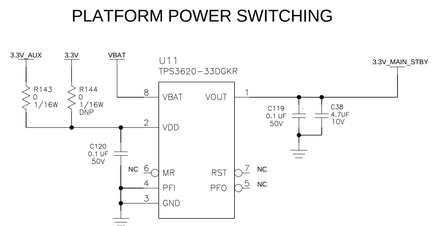
SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

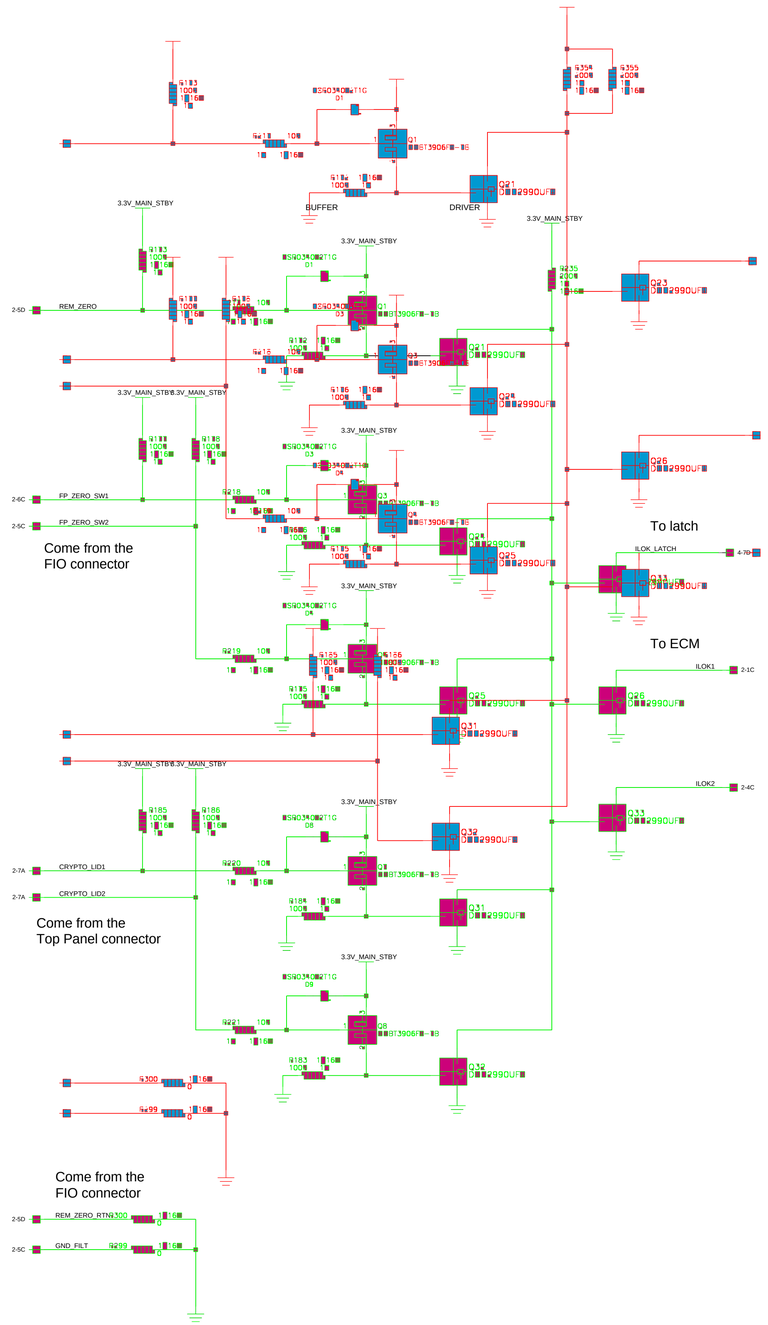
FILE NAME 112302-01003

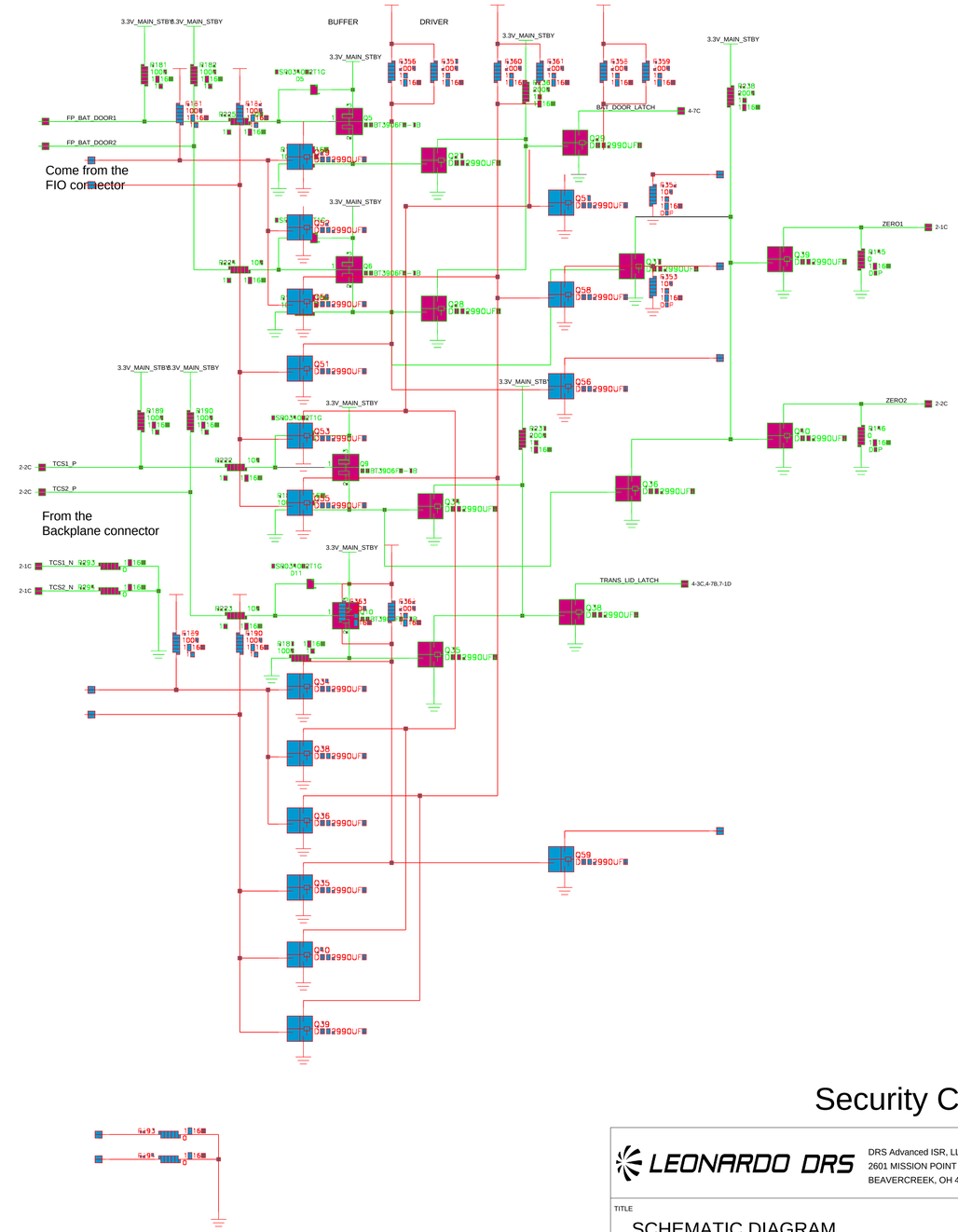
SHEET 2 OF 11

EXPORT CONTROLLED

SEE PAGE 1







Security Circuits

LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

EXPORT CONTROLLED

SEE PAGE 1

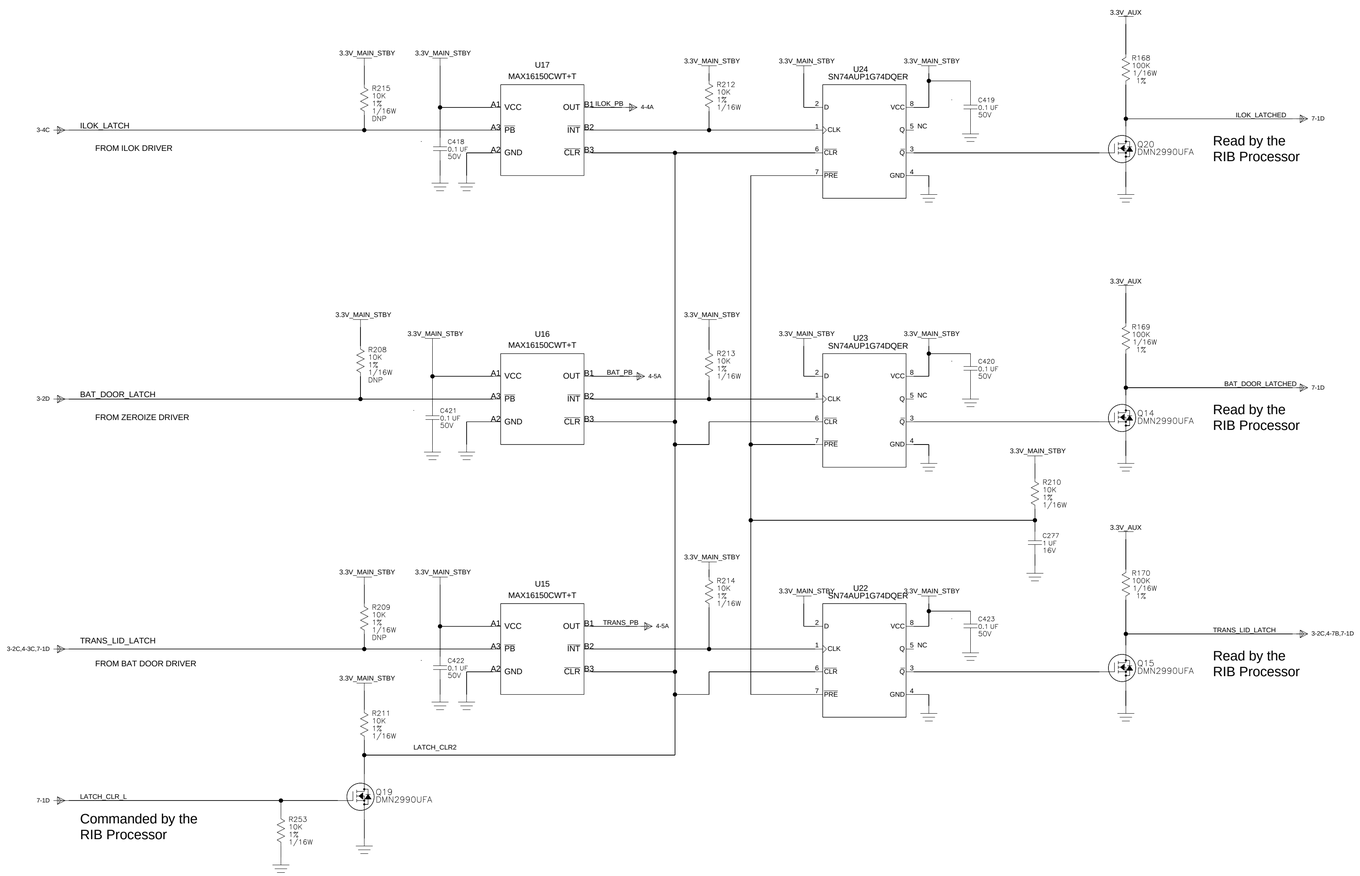
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

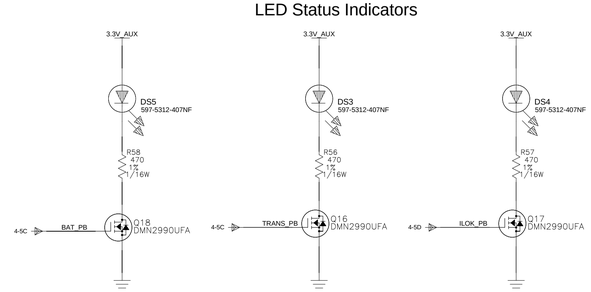
FILE NAME 112302-01003

SHEET 3 OF 11

Status Latches



LED Status Indicators



Security Latches

EXPORT CONTROLLED

SEE PAGE 1

LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

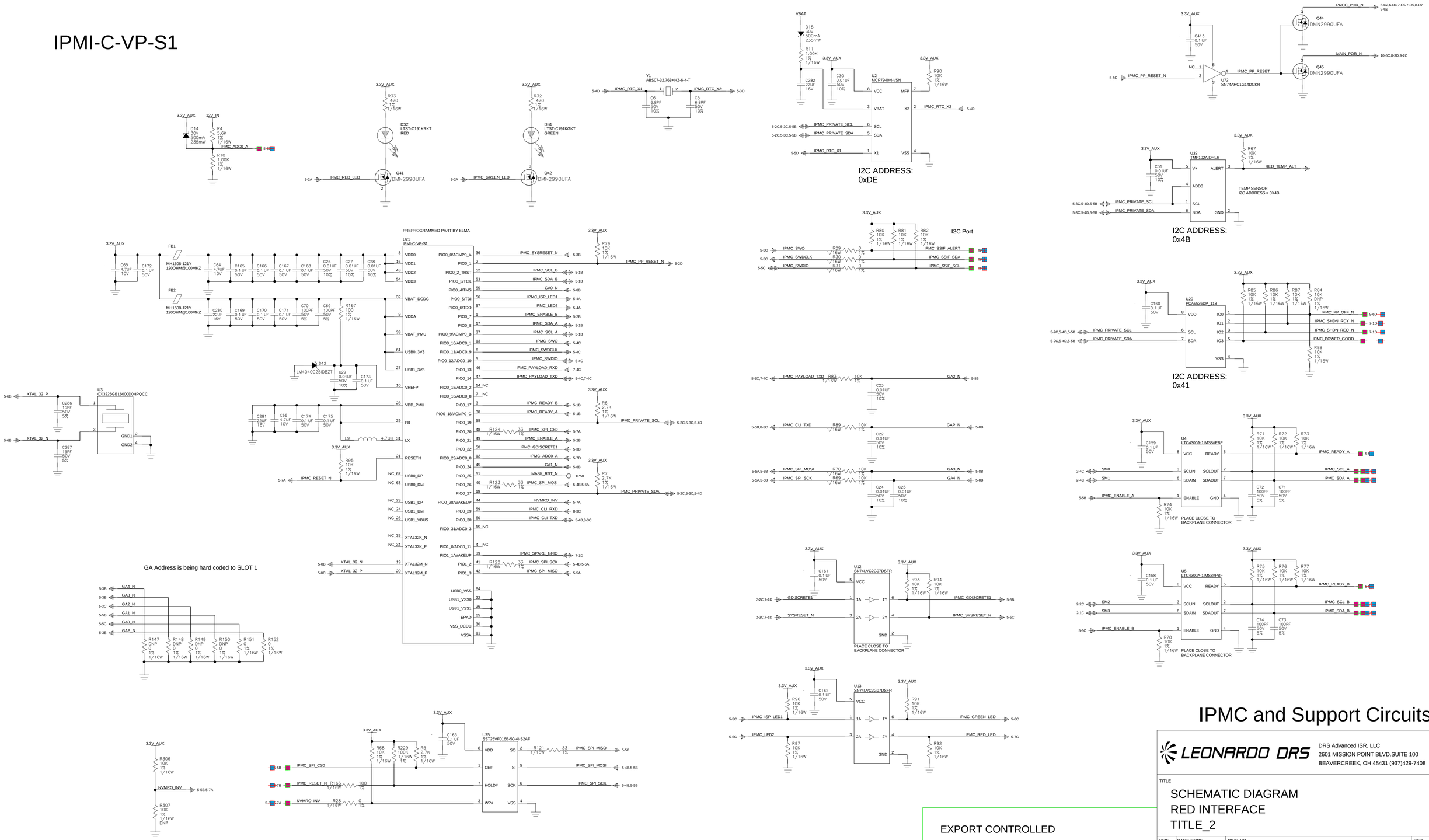
SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

FILE NAME 112302-01003

SHEET 4 OF 11

How does IPMC get programmed if it is a blank device?

IPMI-C-VP-S1



IPMC and Support Circuits

EXPORT CONTROLLED

SEE PAGE 1

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2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

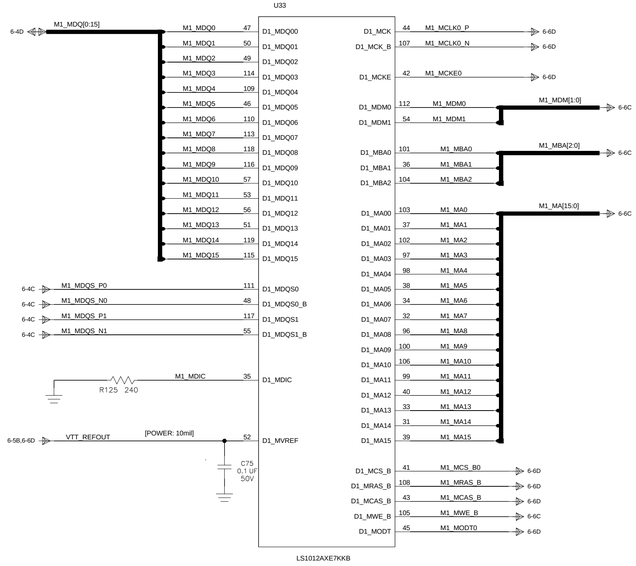
FILE NAME 112302-01003

SHEET 5 OF 11

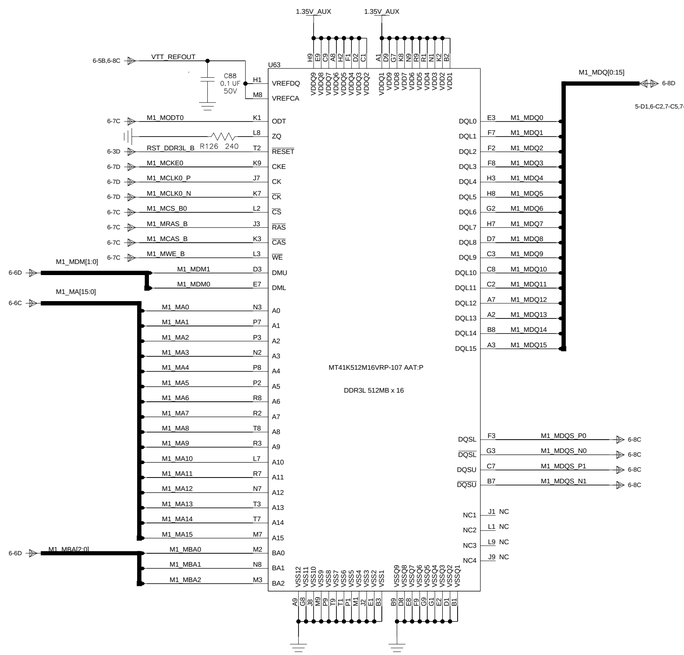
Increase this to 1G or 2G.

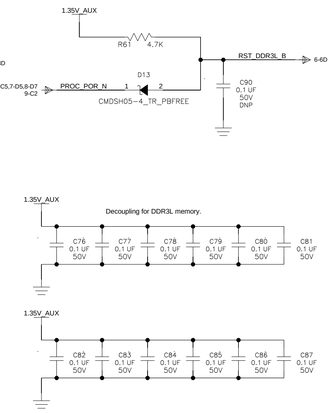
Micron MT41K512M16VRP-107 AAT:P 512Mx16 = 1G

LS1012 DDR3L CONTROLLER BLOCK

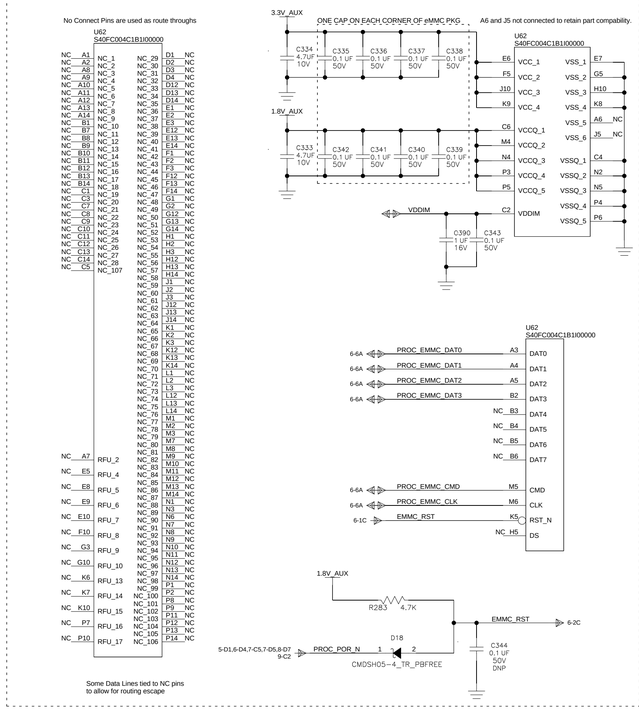


1G of DDR3L

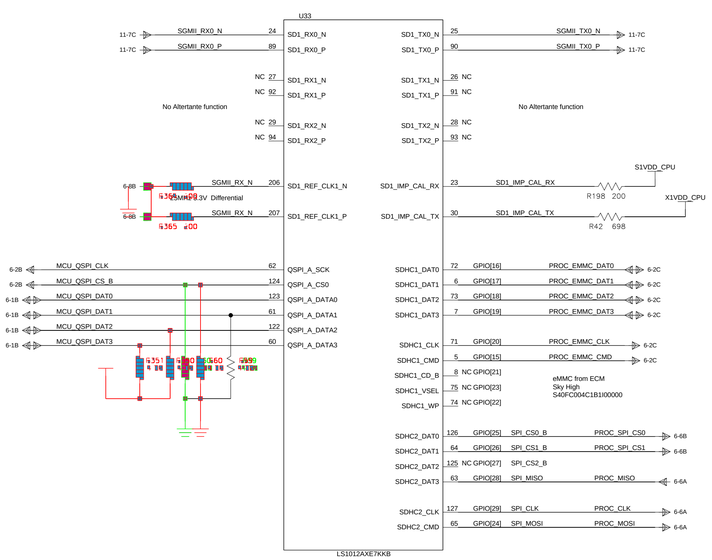


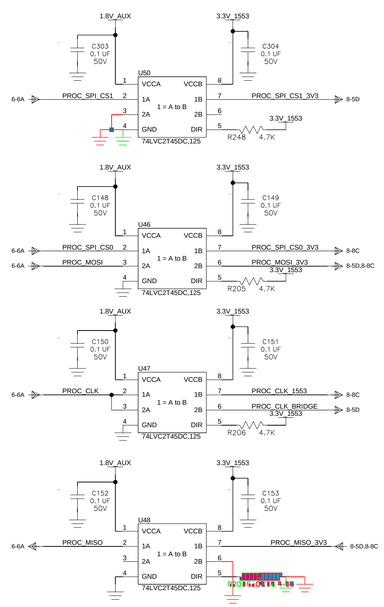


4G eMMC SLC Flash

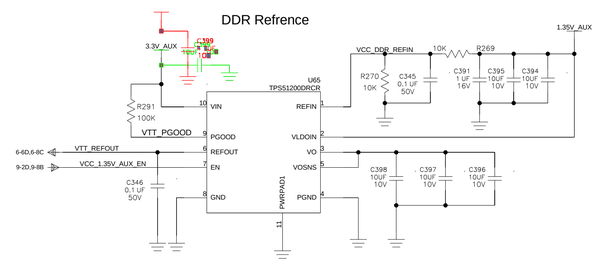


MCU SPI Level Tranlation

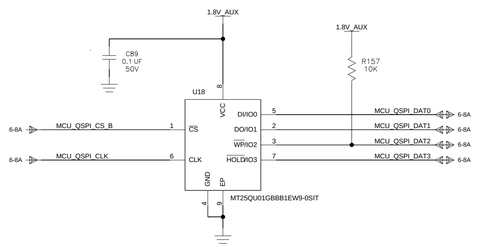




DDR Refrence



Program NOR Flash Boot Block 128MB



RIB Processor and Memories

EXPORT CONTROLLED

SEE PAGE 1

LEONARDO DRS

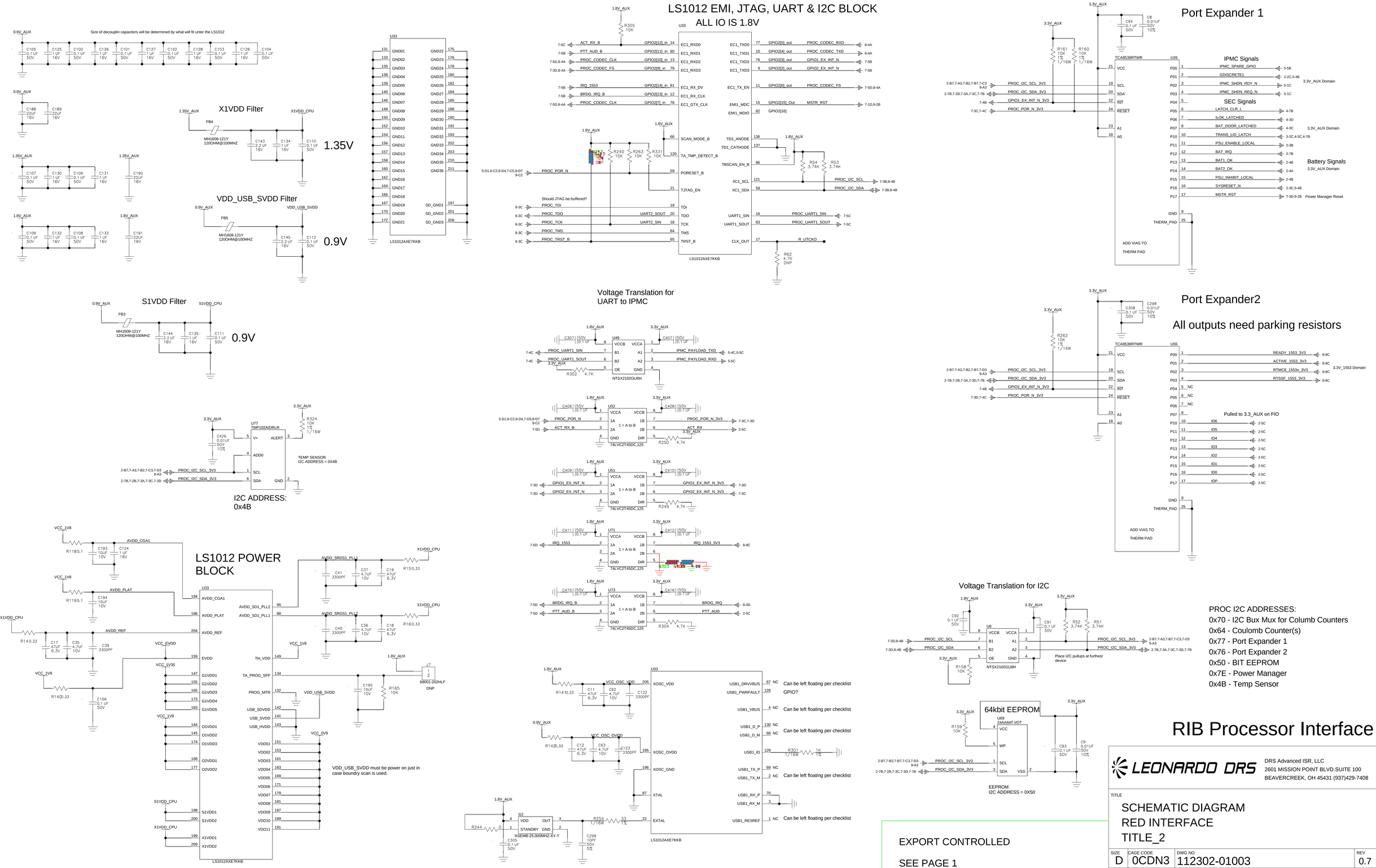
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

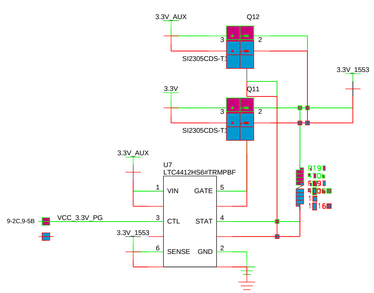
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

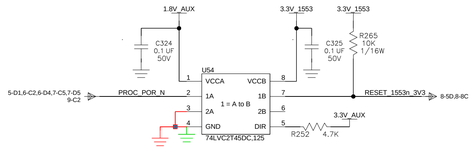
SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

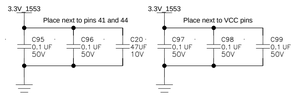
FILE NAME 112302-01003

SHEET 6 OF 11

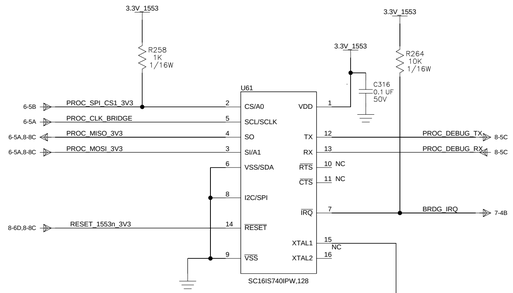

LS1012 EMI, JTAG, UART & I2C BLOCK
ALL IO IS 1.8V
Size of decouplin capacitors will be determined by what will fit unter the LS1012
X1VDD Filter
1.35V
VDD_USB_SVDD Filter
0.9V
S1VDD Filter
0.9V
Voltage Translation for UART to IPMC
Port Expander 1
IPMC Signals
SEC Signals
Battery Signals
Port Expander2
All outputs need parking resistors
Pulled to 3.3_AUX on FIO
TEMP SENSOR
I2C ADDRESS = 0x4B
LS1012 POWER BLOCK
VDD_USB_SVDD must be power on just in case boundry scan is used.
Voltage Translation for I2C
PROC I2C ADDRESSES:
0x70 - I2C Bux Mux for Columb Counters
0x64 - Coulomb Counter(s)
0x77 - Port Expander 1
0x76 - Port Expander 2
0x50 - BIT EEPROM
0x7E - Power Manager
0x4B - Temp Sensor
64kbit EEPROM
EEPROM
I2C ADDRESS = 0X50
RIB Processor Interface
EXPORT CONTROLLED
SEE PAGE 1
LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2
SIZE D
CAGE CODE 0CDN3
DWG NO 112302-01003
REV 0.7
FILE NAME 112302-01003
SHEET 7 OF 11

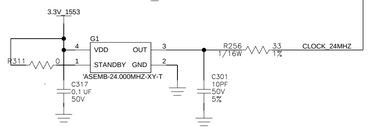


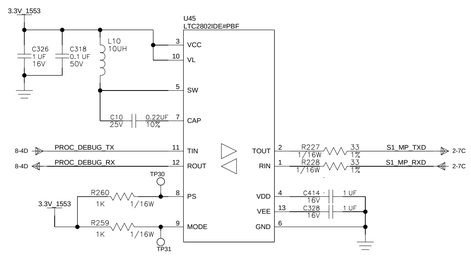




SPI to UART Bridge

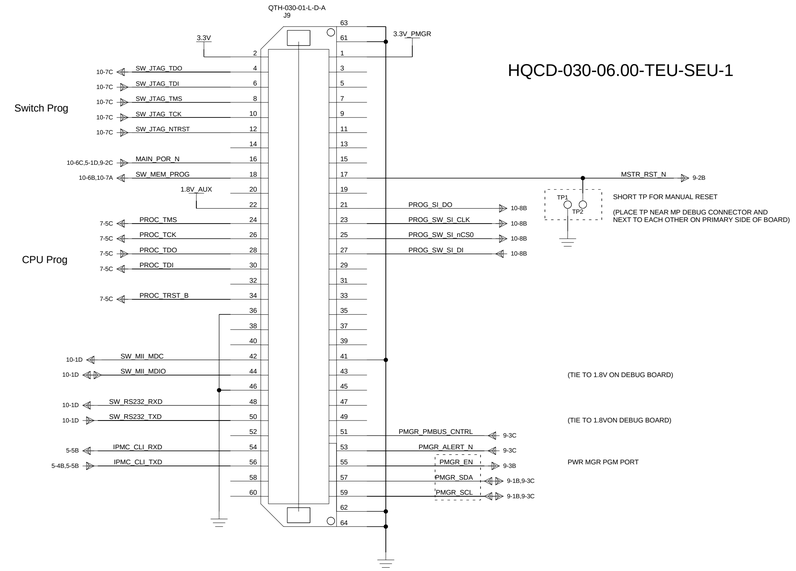




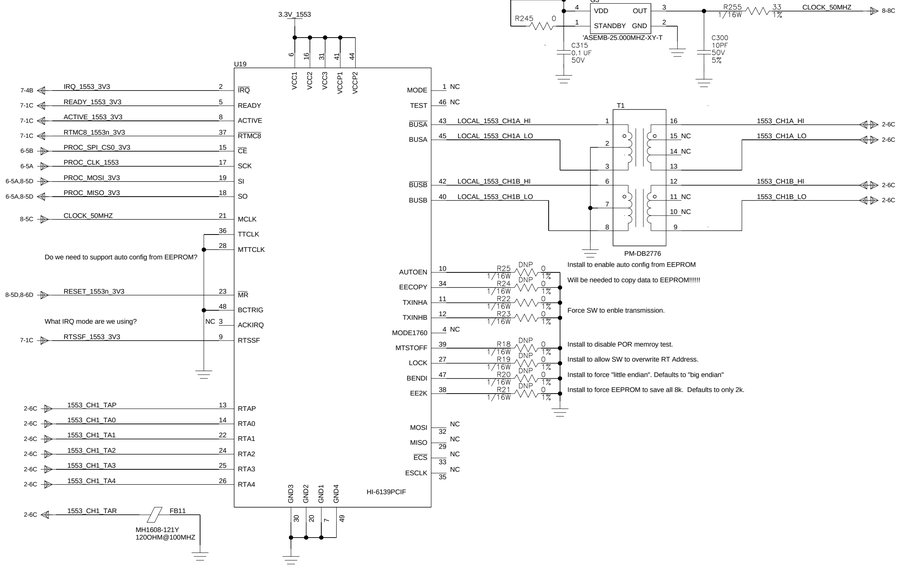


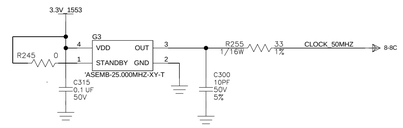
Will need GPIO if this needs to be shutdown.

MULTIPURPOSE DEBUG PORT

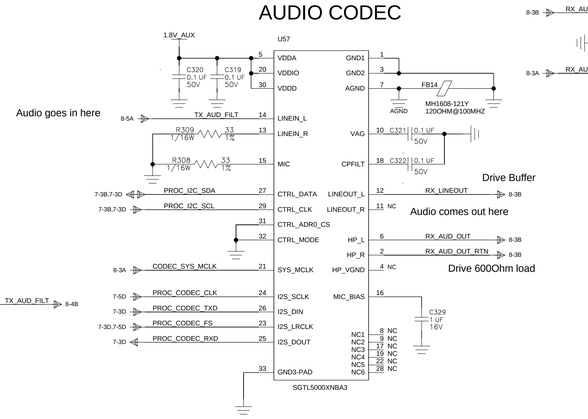


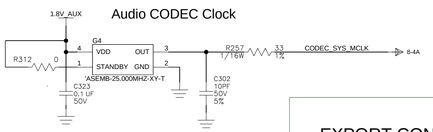
1553 Terminal

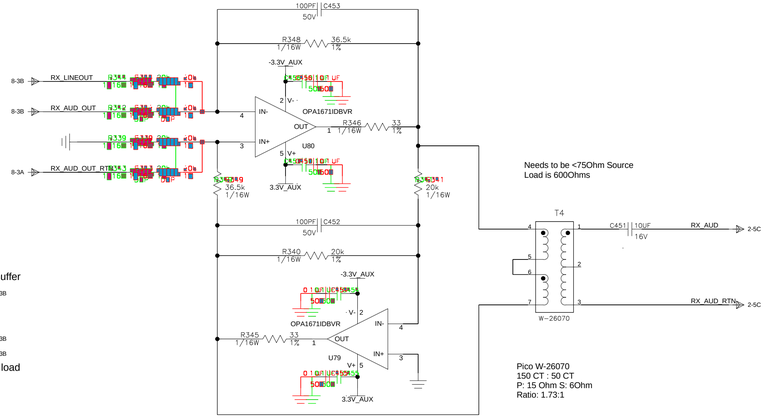




AUDIO CODEC

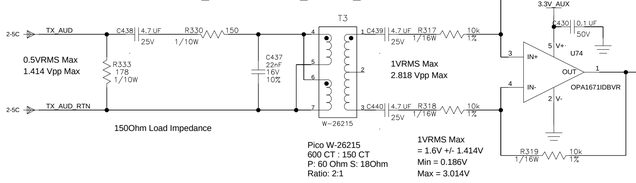




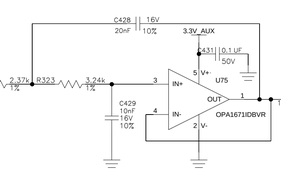


1.6V Refrence for Amp Bias

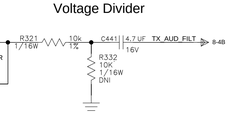
Unity Differential Amplifier



Lowpass Filter



Voltage Divider



1553, Serial Bridge and Debug

LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

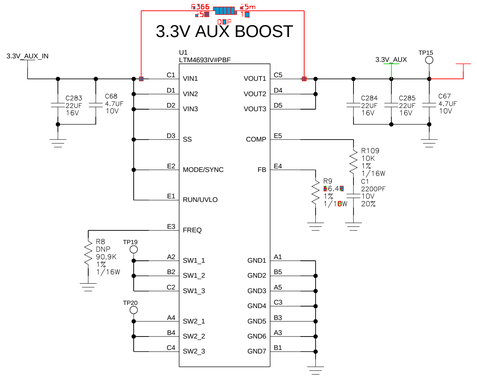
FILE NAME 112302-01003 SHEET 8 OF 11

EXPORT CONTROLLED

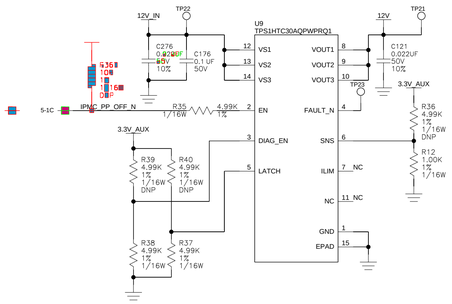
SEE PAGE 1

Audio Uncertinty Connector

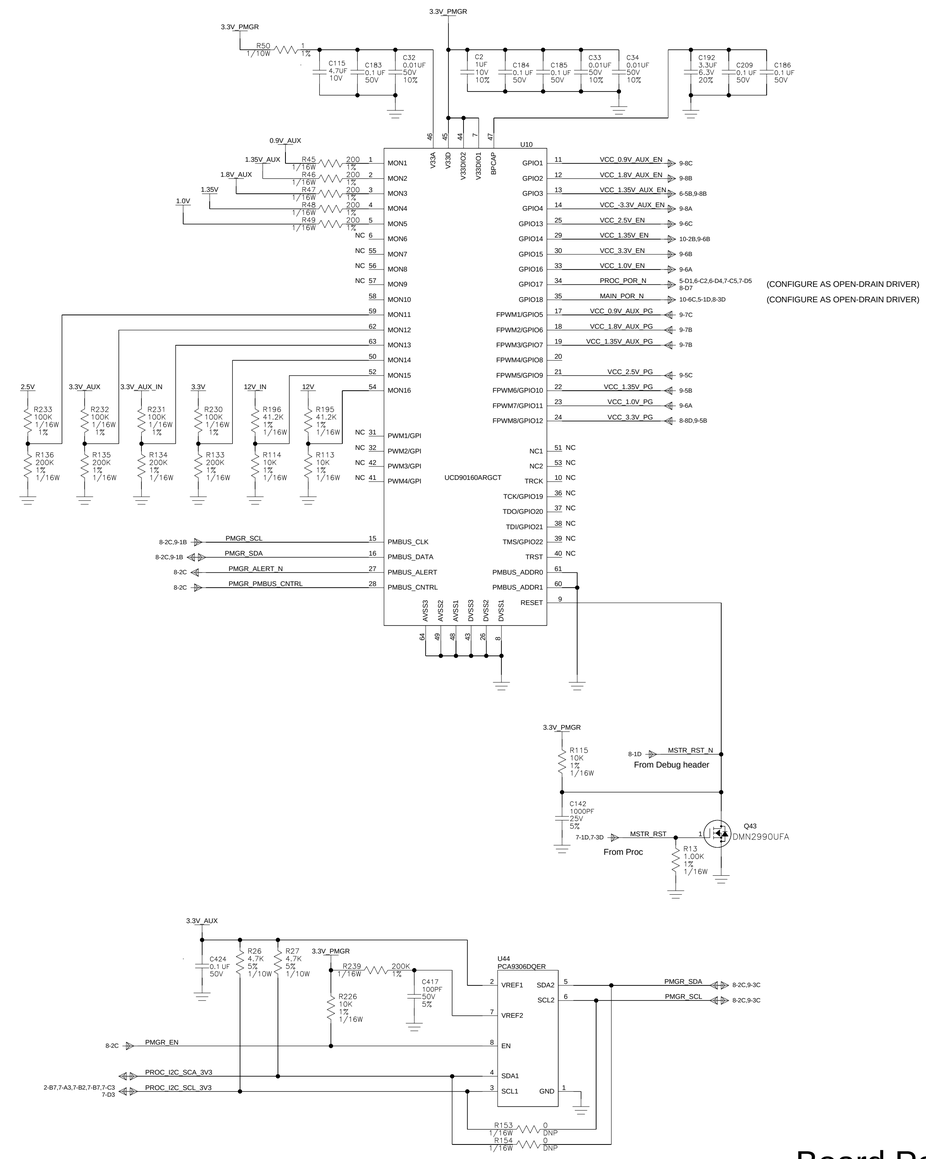
3.3V AUX BOOST



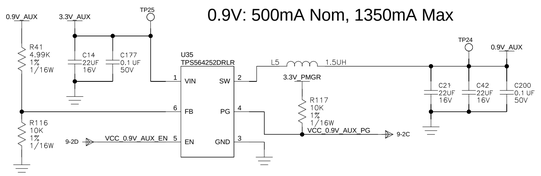
IPMC CONTROLLED 12V ON/OFF SWITCH

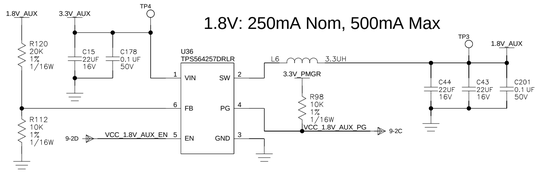


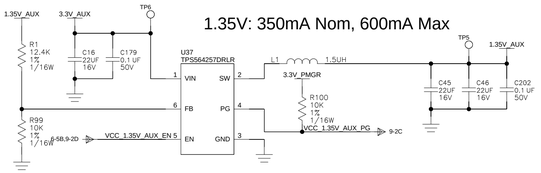
We have two power on sequences::
1) 3.3V_AUX is applied and it's rails come alive
2) IMPC releases 12V rail and remaining rails start



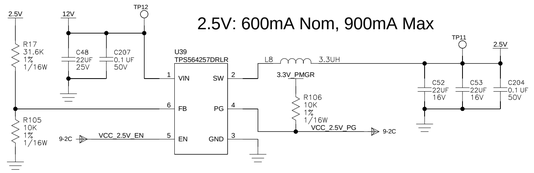
3.3V_AUX Input Regulators

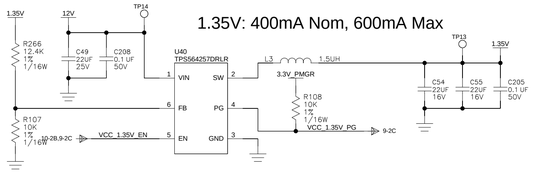


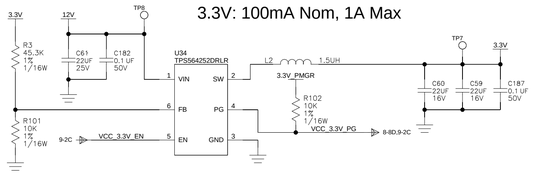


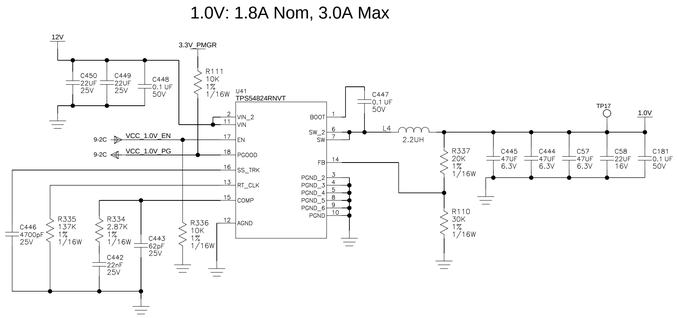


12V Input Regulators

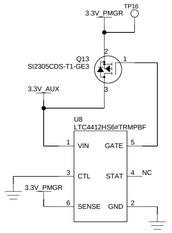


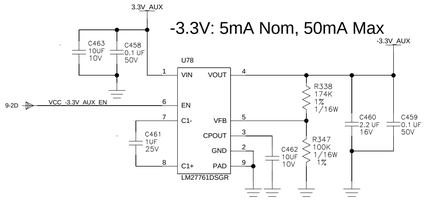






Allows the PMIC to be programmed
with primary power.
Needed?





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SEE PAGE 1

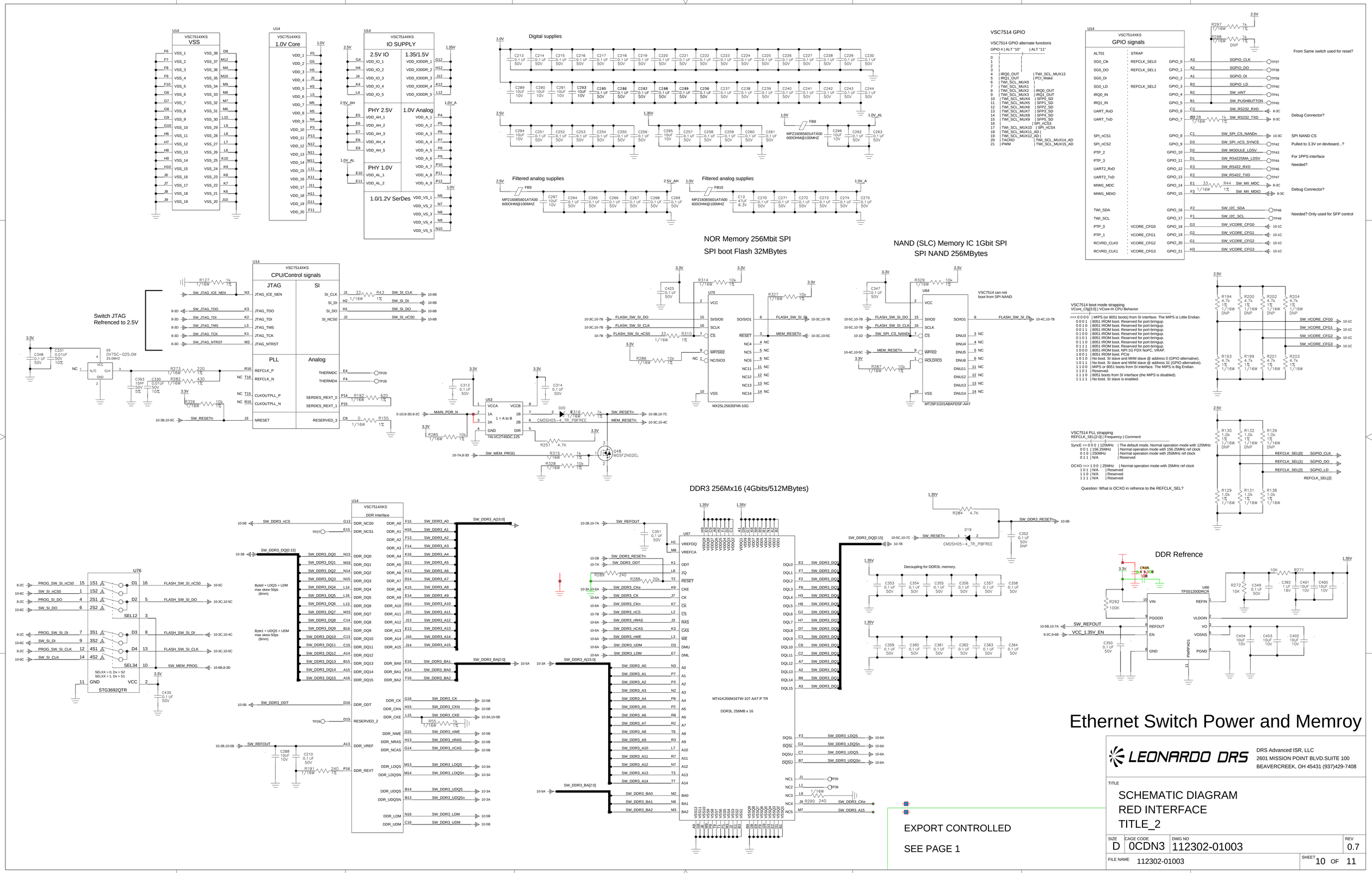
Board Power

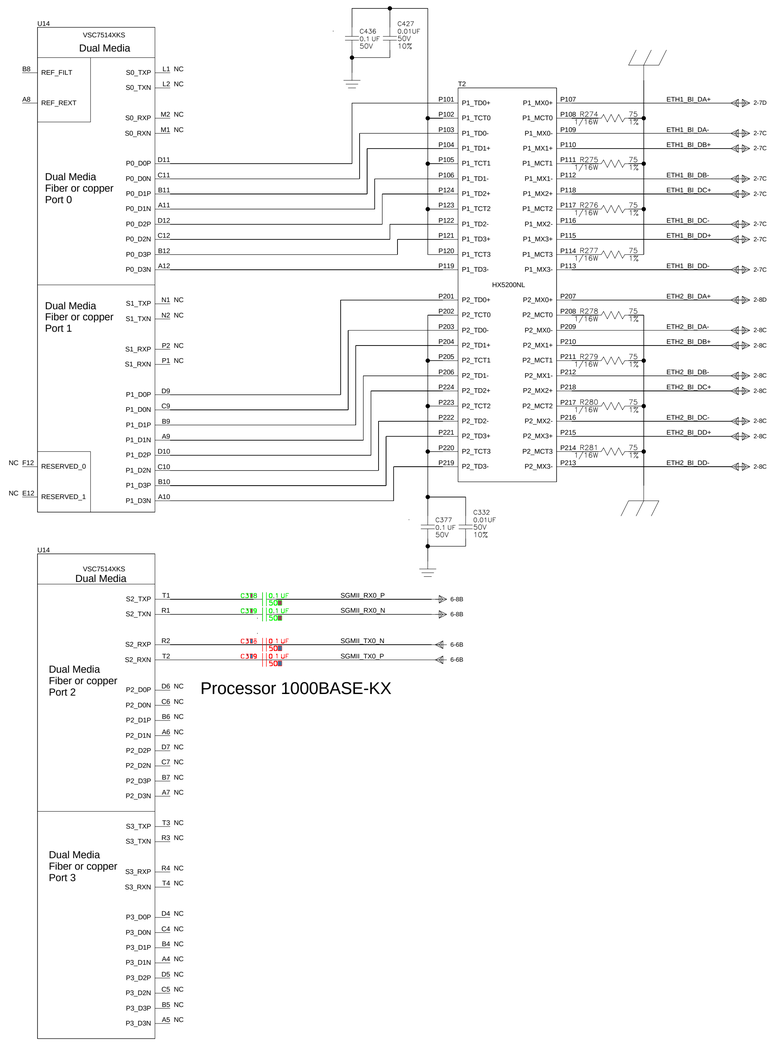
LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

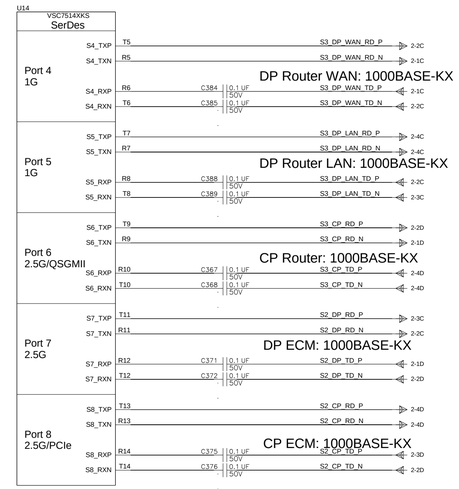
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

FILE NAME 112302-01003 SHEET 9 OF 11


VSC7514 GPIO
VSC7514 GPIO alternate functions
GPIO # | ALT "10" | ALT "11"
0 | | |
1 | | |
2 | | |
3 | | |
4 | IRQ0_OUT | TWI_SCL_MUX13
5 | IRQ1_OUT | PCI_Wake
6 | TWI_SCL_MUX0 |
7 | TWI_SCL_MUX1 |
8 | TWI_SCL_MUX2 | IRQ0_OUT
9 | TWI_SCL_MUX3 | IRQ1_OUT
10 | TWI_SCL_MUX4 | SFP0_SD
11 | TWI_SCL_MUX5 | SFP1_SD
12 | TWI_SCL_MUX6 | SFP2_SD
13 | TWI_SCL_MUX7 | SFP3_SD
14 | TWI_SCL_MUX8 | SFP4_SD
15 | TWI_SCL_MUX9 | SFP5_SD
16 | | SPI_nCS3
17 | TWI_SCL_MUX10 | SPI_nCS4
18 | TWI_SCL_MUX11_AD |
19 | TWI_SCL_MUX12_AD |
20 | TACHO | TWI_SCL_MUX14_AD
21 | PWM | TWI_SCL_MUX15_AD
U14
VSC7514XKS
GPIO signals
ALT01 | STRAP
SG0_Clk | REFCLK_SEL0 | GPIO_0 | A3 | SGPIO_CLK | TP37
SG0_DO | REFCLK_SEL1 | GPIO_1 | A2 | SGPIO_DO | TP38
SG0_DI | GPIO_2 | A1 | SGPIO_DI | TP39
SG0_LD | REFCLK_SEL2 | GPIO_3 | B3 | SGPIO_LD | TP40
IRQ0_IN | GPIO_4 | B2 | SW_nINT | TP41
IRQ1_IN | GPIO_5 | B1 | SW_PUSHBUTTON | TP45
UART_RxD | GPIO_6 | C3 | SW_RS232_RXD | 8-3C
UART_TxD | GPIO_7 | D2 | SW_RS232_TXD | 8-3C
SPI_nCS1 | GPIO_8 | C1 | SW_SPI_CS_NANDn | 10-3C
SPI_nCS2 | GPIO_9 | D3 | SW_SPI_nCS_SYNCE | TP42
PTP_2 | GPIO_10 | D2 | SW_MODULE_LDSV | TP43
PTP_3 | GPIO_11 | D1 | SW_RS4225MA_LDSV | TP44
UART2_RxD | GPIO_12 | E3 | SW_RS422_RXD | TP46
UART2_TxD | GPIO_13 | E2 | SW_RS422_TXD | TP47
MIIM1_MDC | GPIO_14 | E1 | SW_MII_MDC | 8-3C
MIIM1_MDIO | GPIO_15 | F3 | SW_MII_MDIO | 8-3C
TWI_SDA | GPIO_16 | F2 | SW_I2C_SDA | TP48
TWI_SCL | GPIO_17 | F1 | SW_I2C_SCL | TP49
PTP_0 | VCORE_CFG0 | GPIO_18 | G3 | SW_VCORE_CFG0 | 10-1C
PTP_1 | VCORE_CFG1 | GPIO_19 | G2 | SW_VCORE_CFG1 | 10-1C
RCVRD_CLK0 | VCORE_CFG2 | GPIO_20 | G1 | SW_VCORE_CFG2 | 10-1C
RCVRD_CLK1 | VCORE_CFG3 | GPIO_21 | H3 | SW_VCORE_CFG3 | 10-1C
From Same switch used for reset?
Debug Connector?
SPI NAND CS
Pulled to 3.3V on devboard...?
For 1PPS interface
Needed?
Debug Connector?
Needed? Only used for SFP control
Digital supplies
Filtered analog supplies
Filtered analog supplies
NOR Memory 256Mbit SPI
SPI boot Flash 32MBytes
NAND (SLC) Memory IC 1Gbit SPI
SPI NAND 256MBytes
VSC7514 can not boot from SPI NAND
VSC7514 boot mode strapping
VCore_Cfg[3:0] | VCore-III CPU Behavior
0 0 0 0 | MIPS (or 8051 boots) from SI interface. The MIPS is Little Endian.
0 0 0 1 | 8051 IROM boot. Reserved for port-bringup.
0 0 1 0 | 8051 IROM boot. Reserved for port-bringup.
0 0 1 1 | 8051 IROM boot. Reserved for port-bringup.
0 1 0 0 | 8051 IROM boot. Reserved for port-bringup.
0 1 0 1 | 8051 IROM boot. Reserved for port-bringup.
0 1 1 0 | 8051 IROM boot. Reserved for port-bringup.
0 1 1 1 | 8051 IROM boot. Reserved for port-bringup.
1 0 0 0 | 8051 IROM boot. NPI-1G FDX NoFC, VRAP.
1 0 0 1 | 8051 IROM boot. PCIe
1 0 1 0 | No boot, SI slave and MIIM slave @ address 0 (GPIO alternative).
1 0 1 1 | No boot, SI slave and MIIM slave @ address 31 (GPIO alternative).
1 1 0 0 | MIPS or 8051 boots from SI interface. The MIPS is Big Endian.
1 1 0 1 | Reserved.
1 1 1 0 | 8051 boots from SI interface (the MIPS is disabled).
1 1 1 1 | No boot. SI slave is enabled.
VSC7514 PLL strapping
REFCLK_SEL[2:0] | Frequency | Comment
SyncE ==> 0 0 0 | 125MHz | The default mode. Normal operation mode with 125MHz ref clock
0 0 1 | 156.25MHz | Normal operation mode with 156.25MHz ref clock
0 1 0 | 250MHz | Normal operation mode with 250MHz ref clock
0 1 1 | N/A | Reserved
OCXO ==> 1 0 0 | 25MHz | Normal operation mode with 25MHz ref clock
1 0 1 | N/A | Reserved
1 1 0 | N/A | Reserved
1 1 1 | N/A | Reserved
Question: What is OCXO in refrence to the REFCLK_SEL?
REFCLK_SEL[0] SGPIO_CLK
REFCLK_SEL[1] SGPIO_DO
REFCLK_SEL[2] SGPIO_LD
REFCLK_SEL[2]
U14
VSC7514XKS
VSS
1.0V Core
IO SUPPLY
2.5V IO
1.35/1.5V
PHY 2.5V
1.0V Analog
PHY 1.0V
1.0/1.2V SerDes
U14
VSC7514XKS
CPU/Control signals
JTAG
SI
PLL
Analog
NRESET
RESERVED_3
Switch JTAG Refrenced to 2.5V
DDR3 256Mx16 (4Gbits/512MBytes)
U14
VSC7514XKS
DDR Interface
U76
STG3692QTR
SELX0 = 0, Dx = S2
SELX0 = 1, Dx = S1
Byte0 = LDQS + LDM max skew 50ps (8mm)
Byte1 = UDQS + UDM max skew 50ps (8mm)
U67
MT41K256M16TW-107 AAT:P TR
DDR3L 256MB x 16
Decoupling for DDR3L memory.
DDR Refrence
U66
TPS51200DRCR
PMP9401
Ethernet Switch Power and Memroy
EXPORT CONTROLLED
SEE PAGE 1
LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408
TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2
SIZE D
CAGE CODE 0CDN3
DWG NO 112302-01003
REV 0.7
FILE NAME 112302-01003
SHEET 10 OF 11





Ethernet Switch Ports

EXPORT CONTROLLED

SEE PAGE 1

LEONARDO DRS
DRS Advanced ISR, LLC
2601 MISSION POINT BLVD.SUITE 100
BEAVERCREEK, OH 45431 (937)429-7408

TITLE
SCHEMATIC DIAGRAM
RED INTERFACE
TITLE_2

SIZE	CAGE CODE	DWG NO	REV
D	0CDN3	112302-01003	0.7

FILE NAME 112302-01003 SHEET 11 OF 11