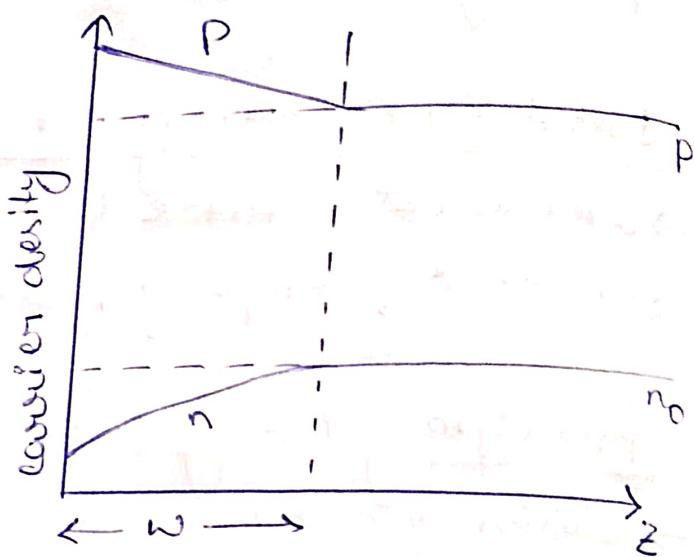
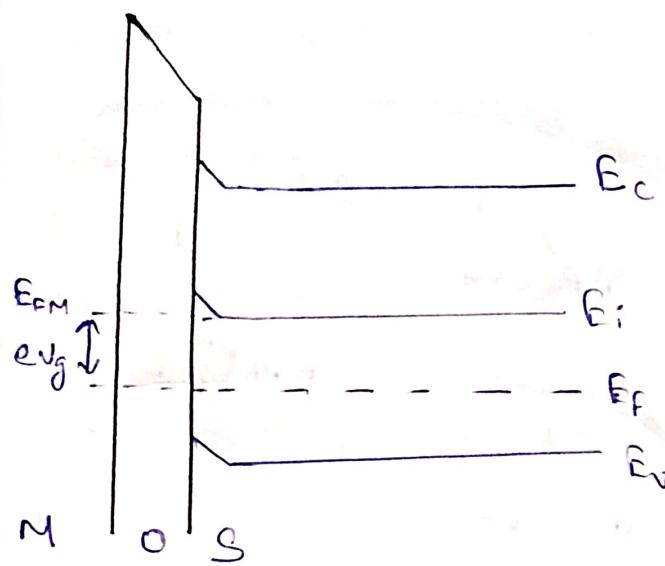
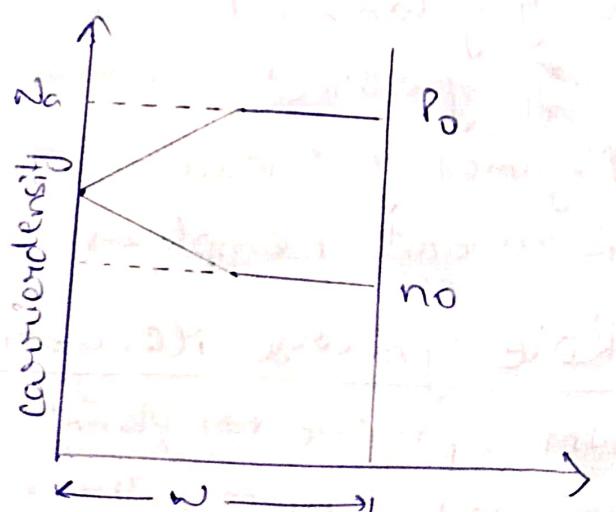
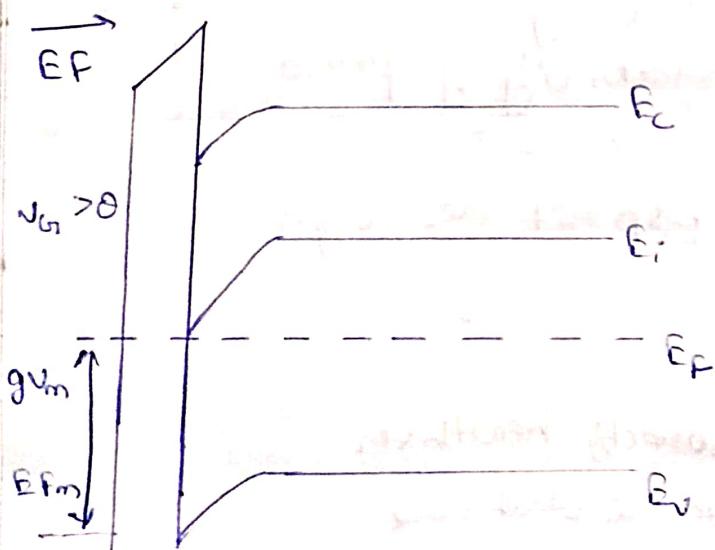


Draw well labelled diagram of the following:

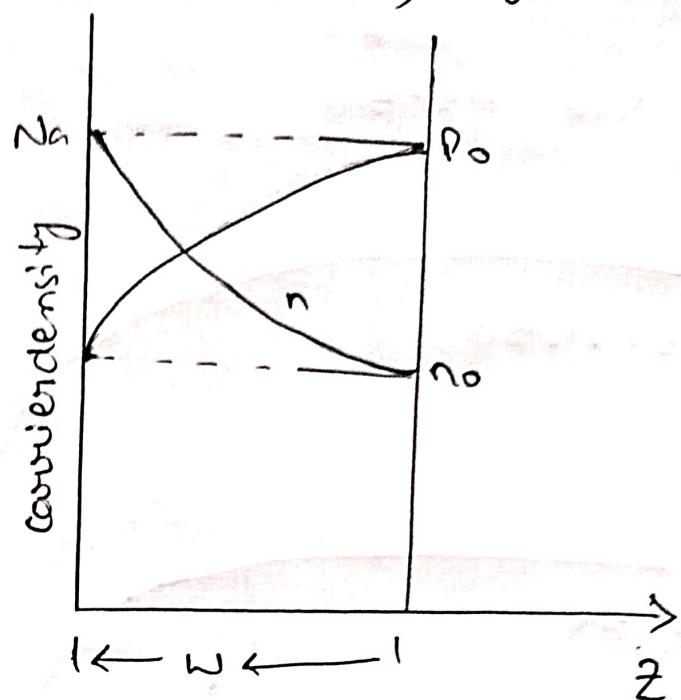
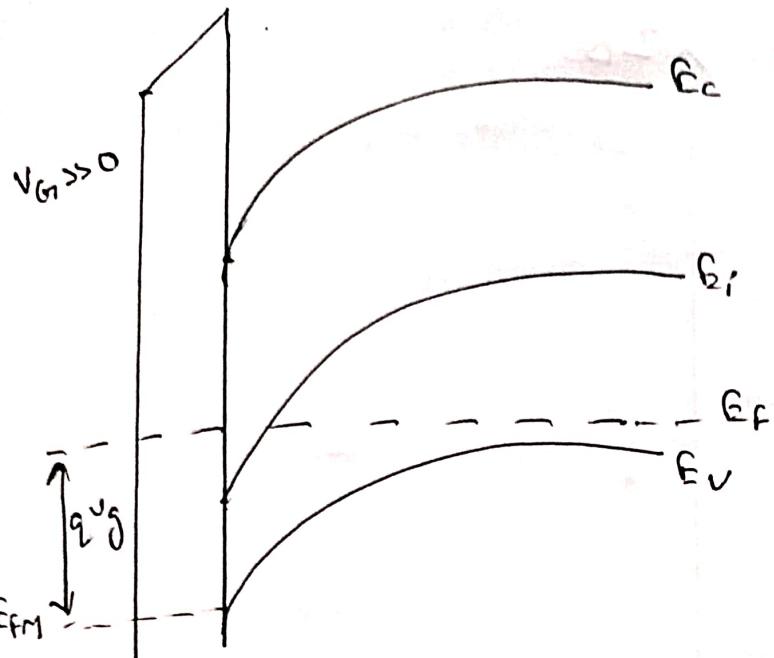
1. Energy Band in Accumulation :-



2. Energy Band in Depletion :-

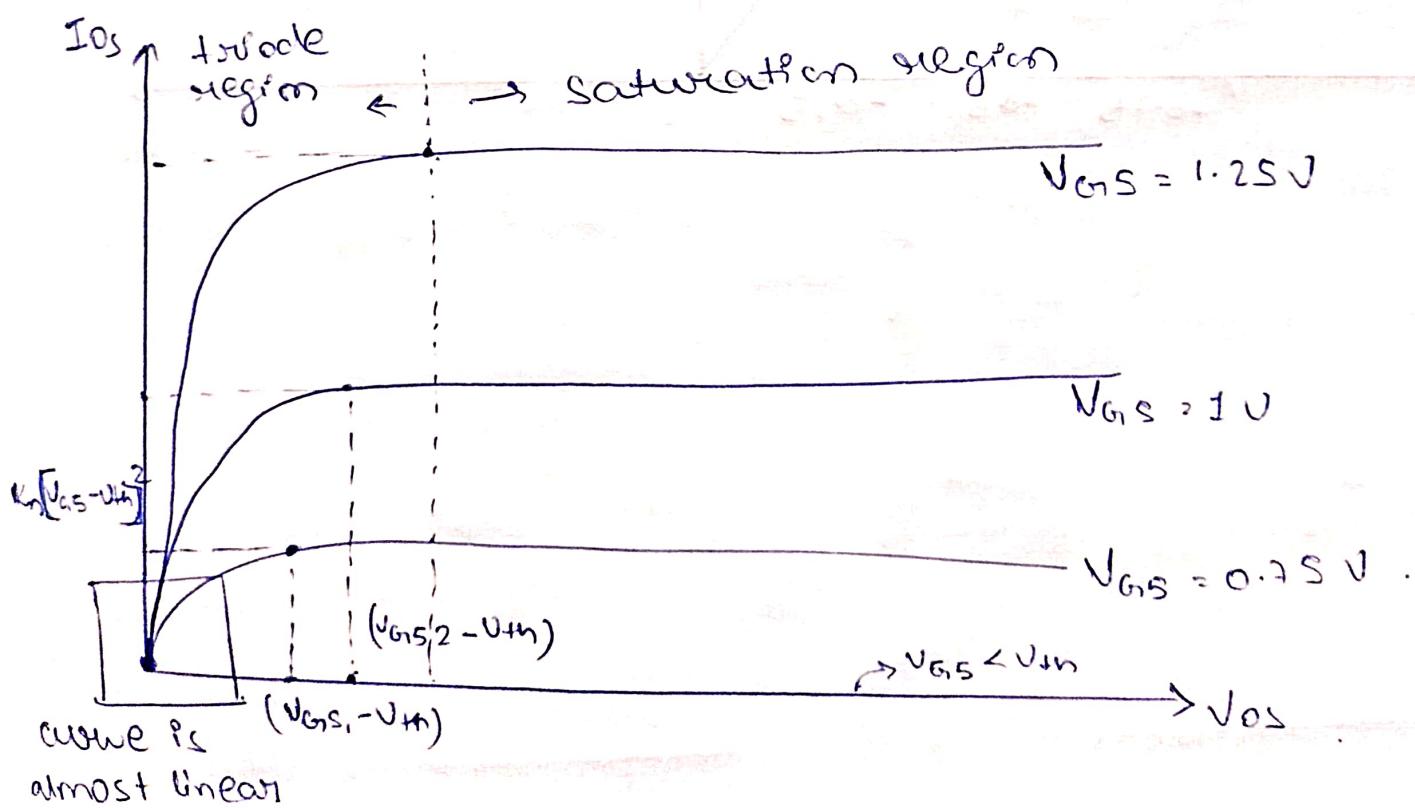


3. Energy band in inversion $n(\text{interface}) > P_0$

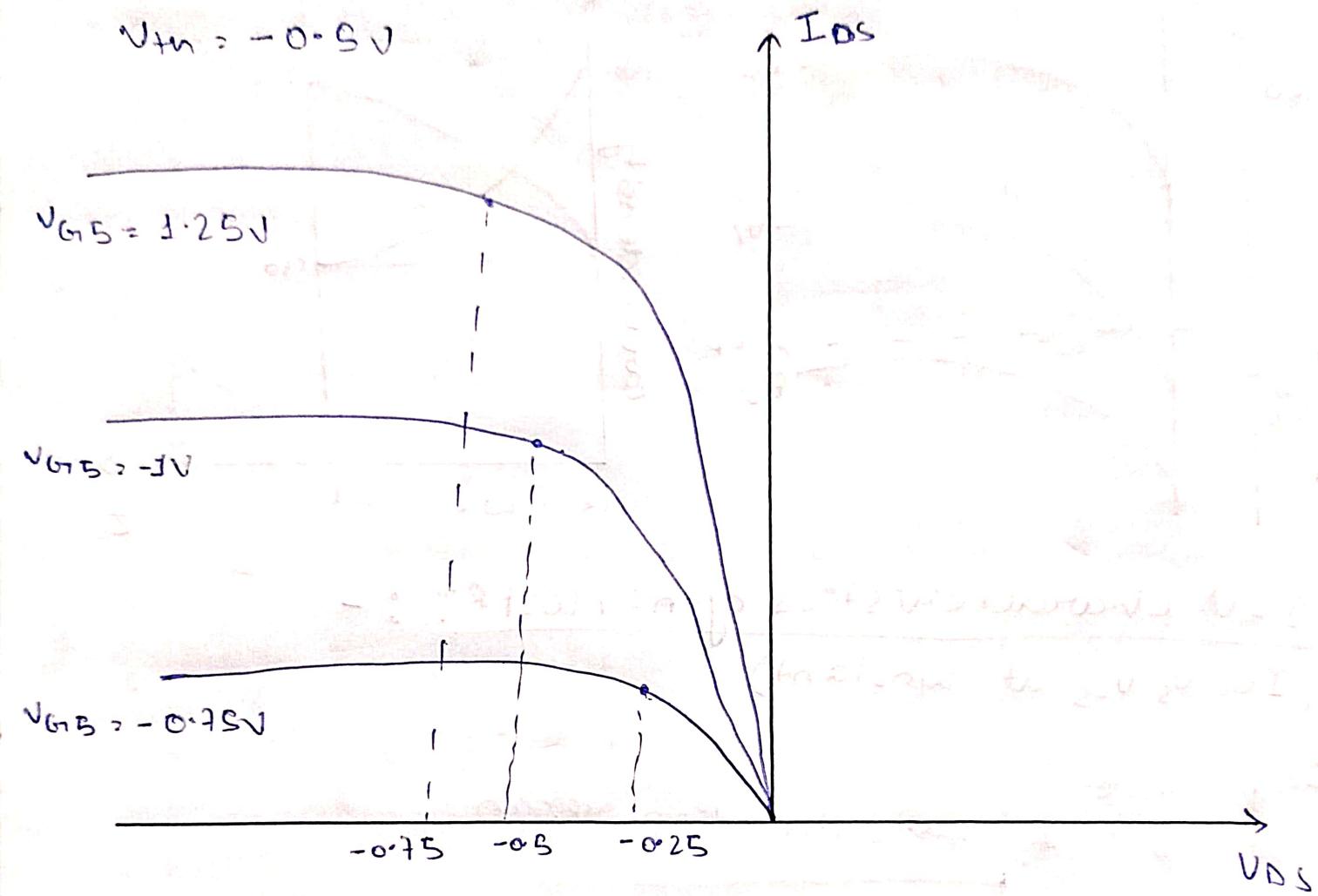


4. I-V characteristics of n-MOSFET :-

(I_{DS} , V_S , V_{DS} at constant)



5. IV characteristics of p-Mosfet :-



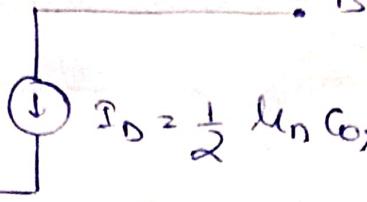
6. Large signal equivalent circuit model of Mosfet :-

- Saturation : $V_{G,S} > V_{th}$, $V_{DS} > V_{G,S} - V_{th}$

G +

$V_{G,S}$

S



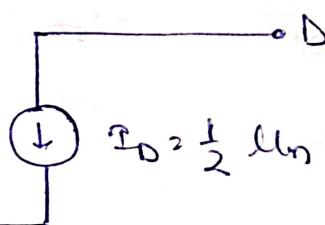
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{G,S} - V_{th})^2$$

- Triode : $V_{G,S} > V_{th}$, $V_{DS} < V_{G,S} - V_{th}$

G +

$V_{G,S}$

S



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{G,S} - V_{th})V_{DS} + V_{DS}^2]$$

- Deep triode : $V_{G,S} > V_{th}$, $V_{DS} \ll V_{G,S} - V_{th}$.

G +

$V_{G,S}$

S

$$I_D = \frac{1}{R_{on}} \quad R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{G,S} - V_{th})}$$

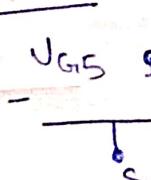
- Saturation including channel length modulation :

$V_{G,S} > V_{th}$

$V_{DS} > V_{G,S} - V_{th}$

G +

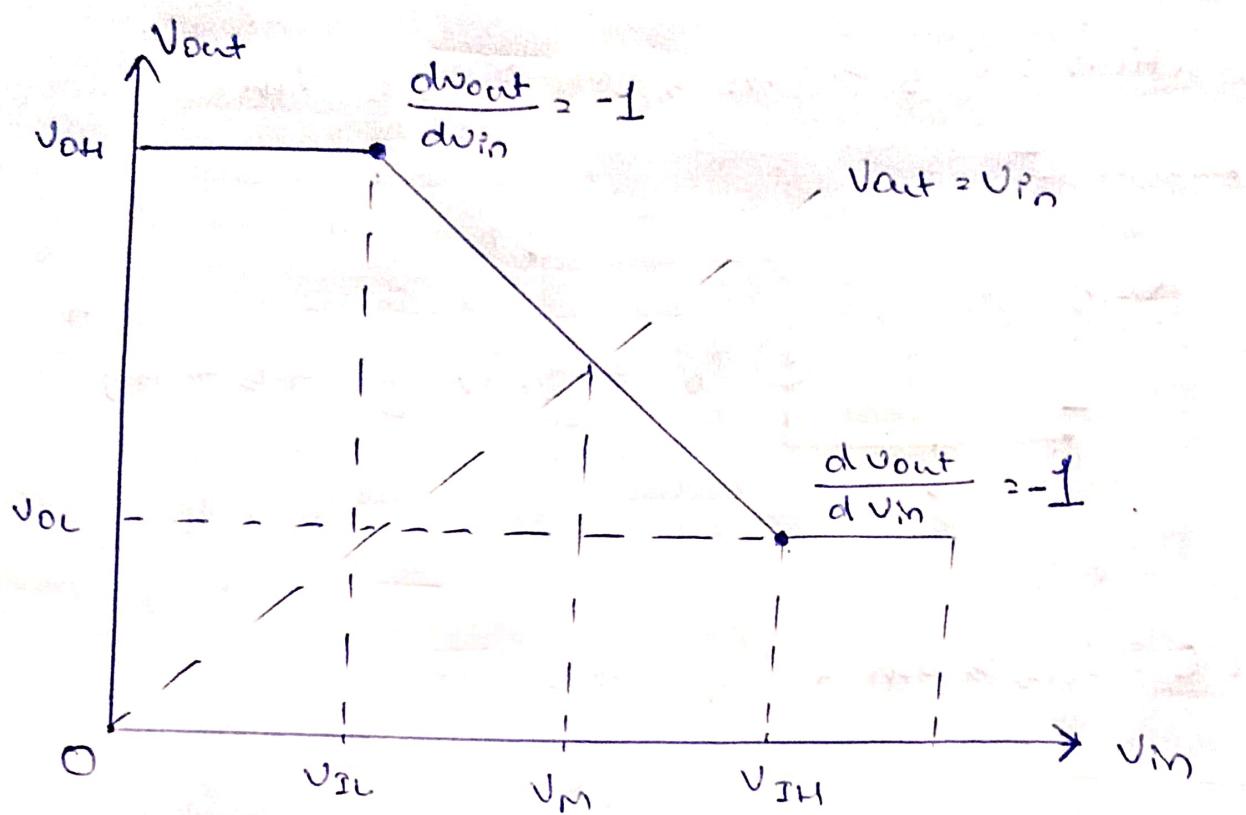
$V_{G,S}$



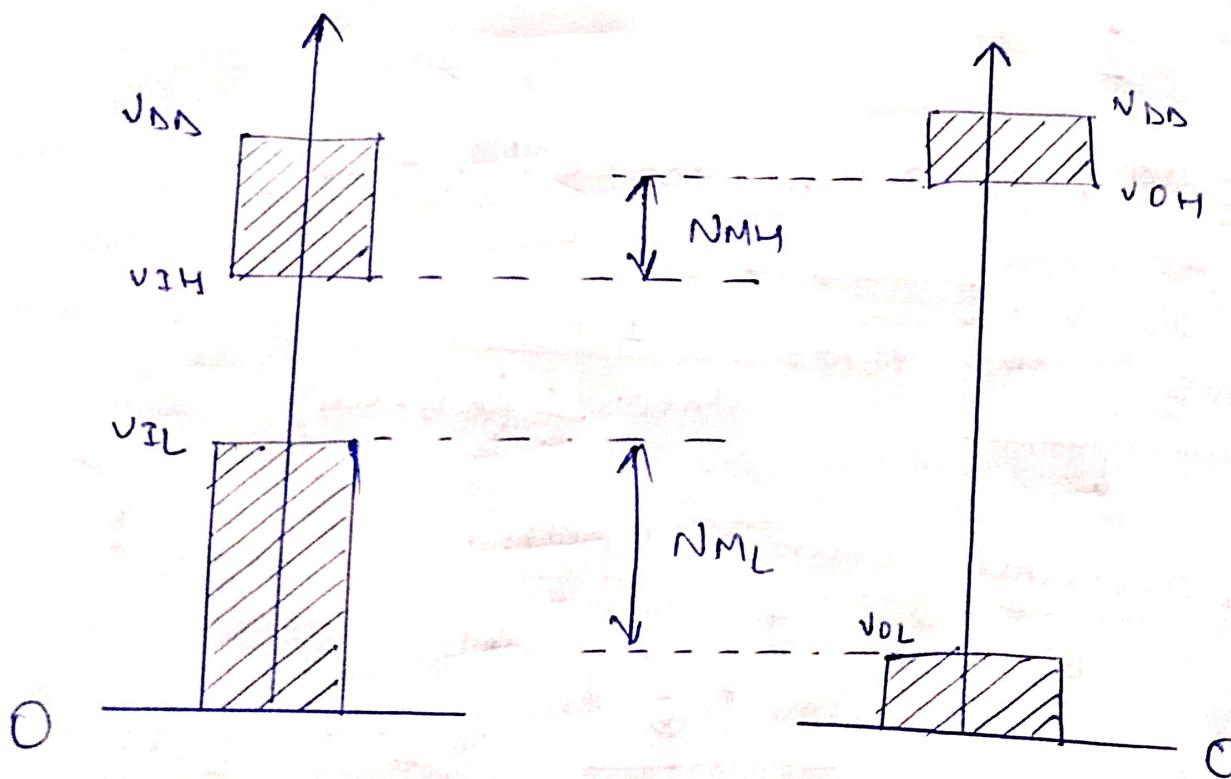
D

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{G,S} - V_{th})^2 (1 + k_V V_{DS})$$

7. Voltage transfer curve :-

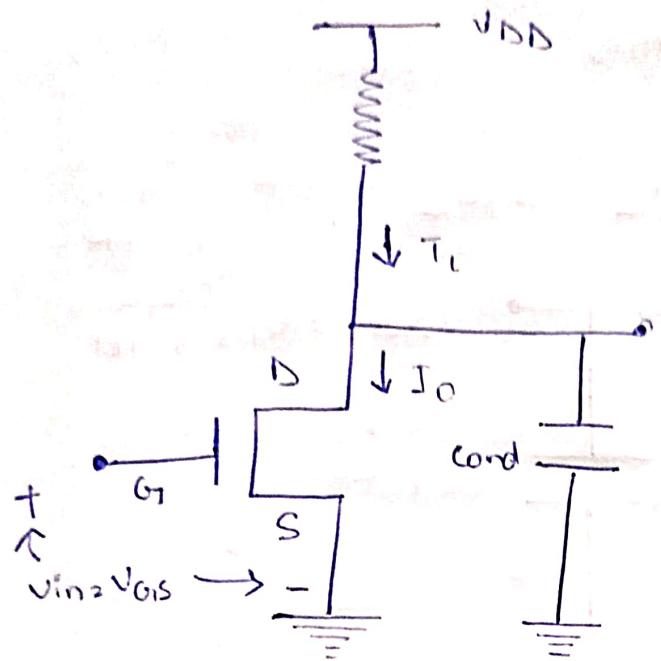


8. Noise Margin :-

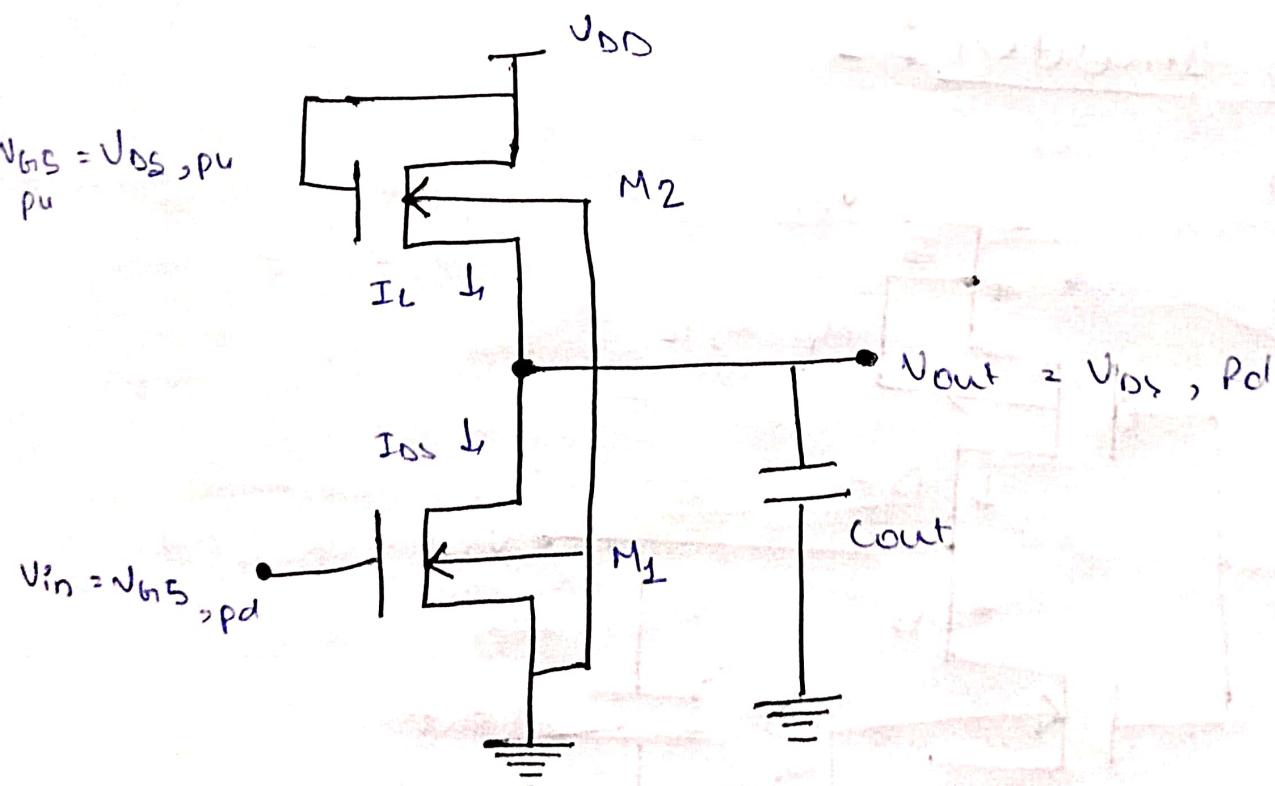


$$N_{NMH} = V_{OH} - V_{TH} \quad \text{and} \quad N_{NML} = V_{IL} - V_{OL}$$

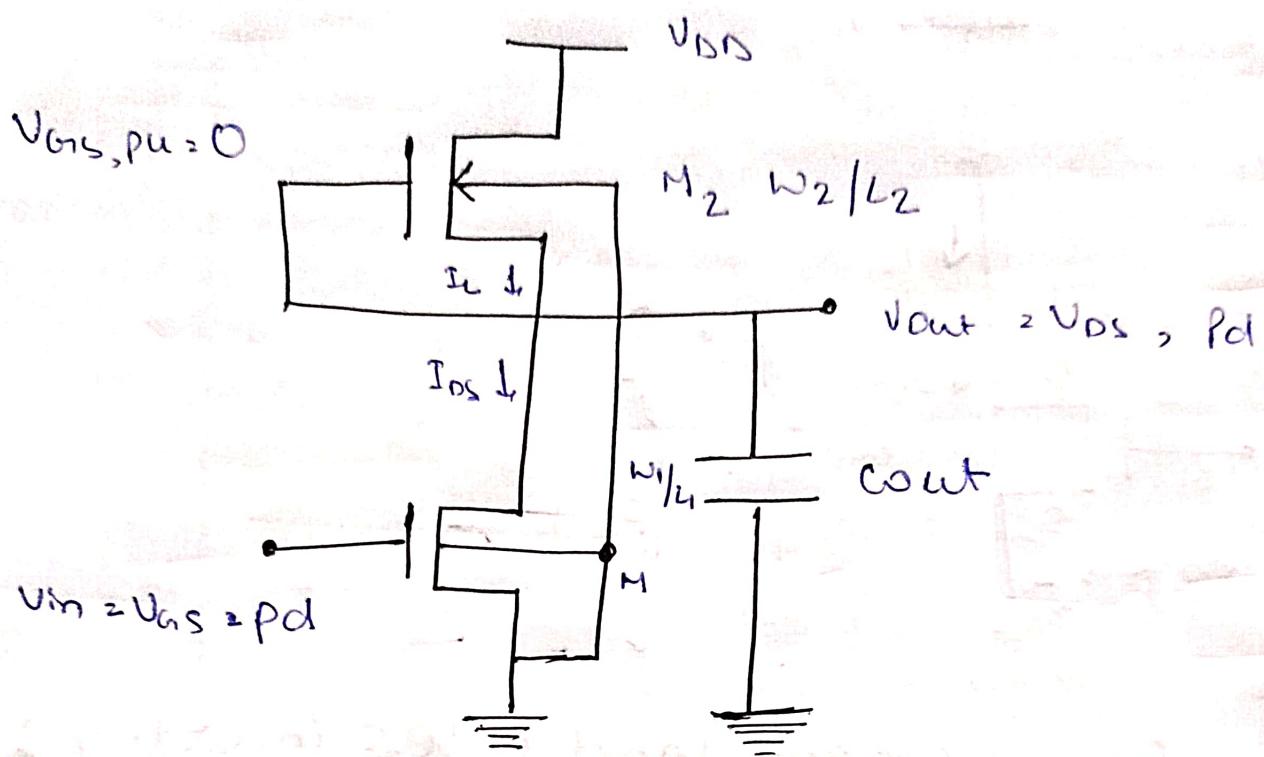
9. Resistive load n-MOS Inverter :-



10. Active Enhancement load nMOS inverter :-

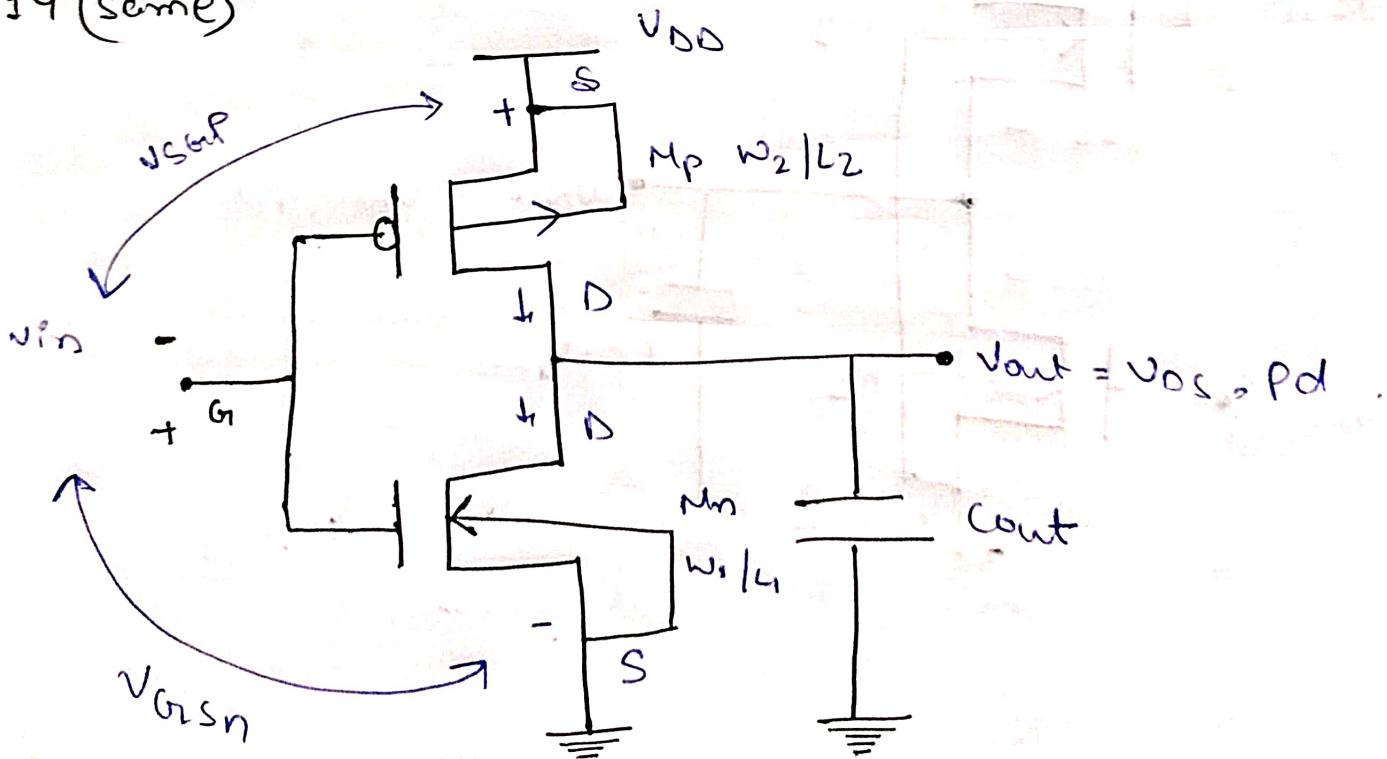


11. Active Depletion Load NMOS Inverter :-

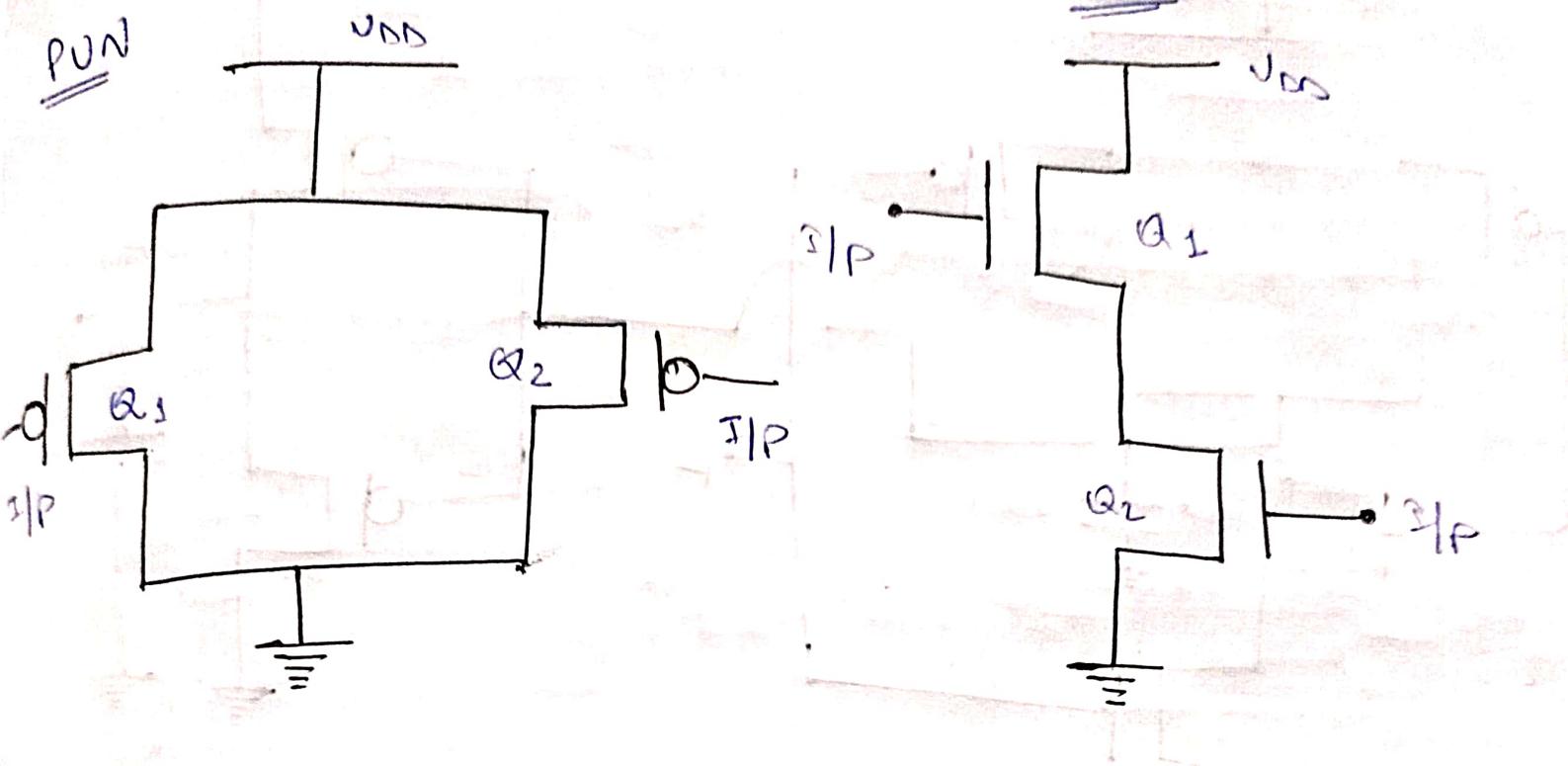


12. CMOS Inverter :-

& 14 (same)

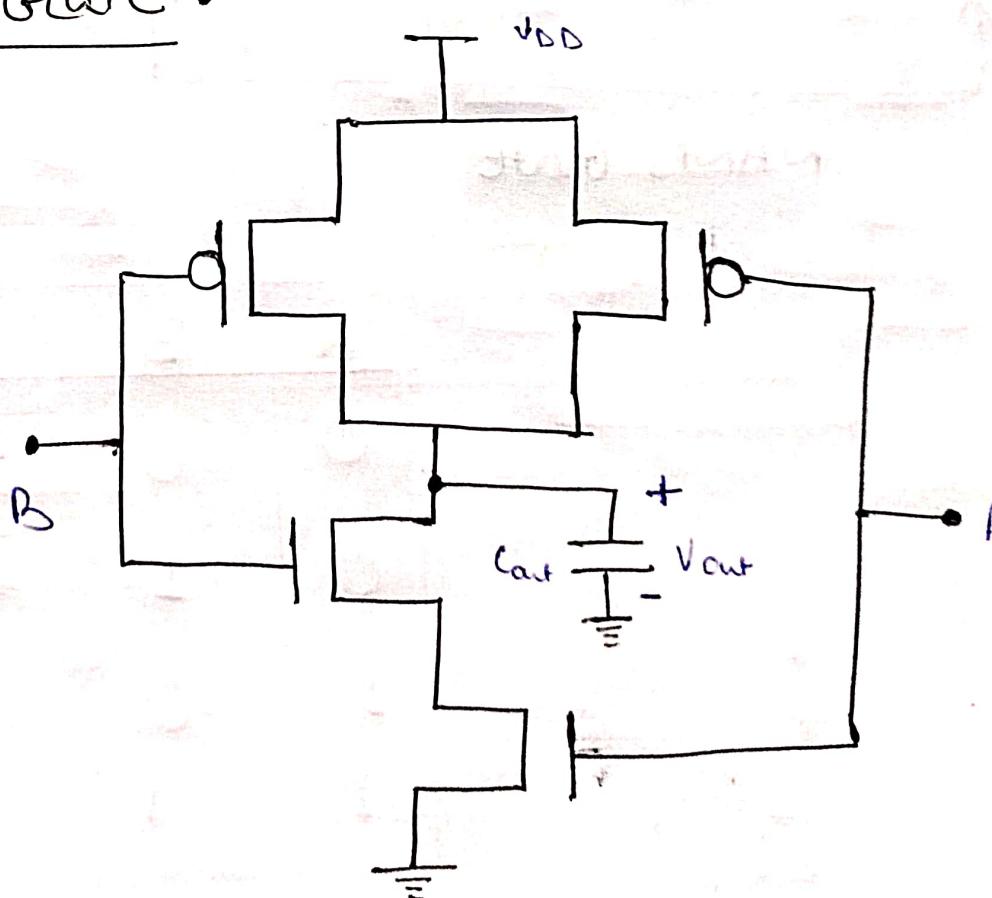


13. Pull up network & pull down network :-
(PUN & PDN)

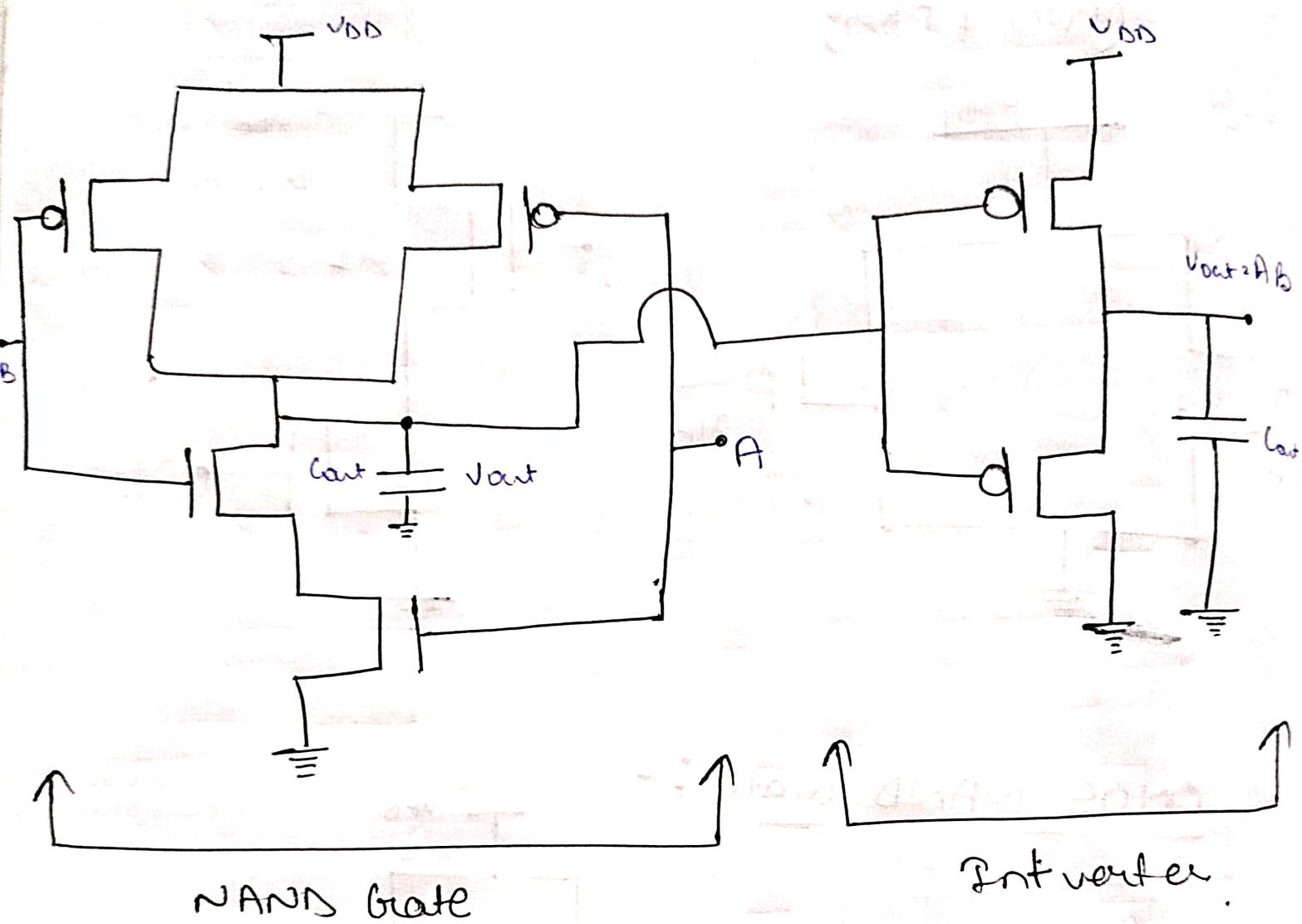


15. CMOS NAND Gate :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



16. CMOS AND GATE :-

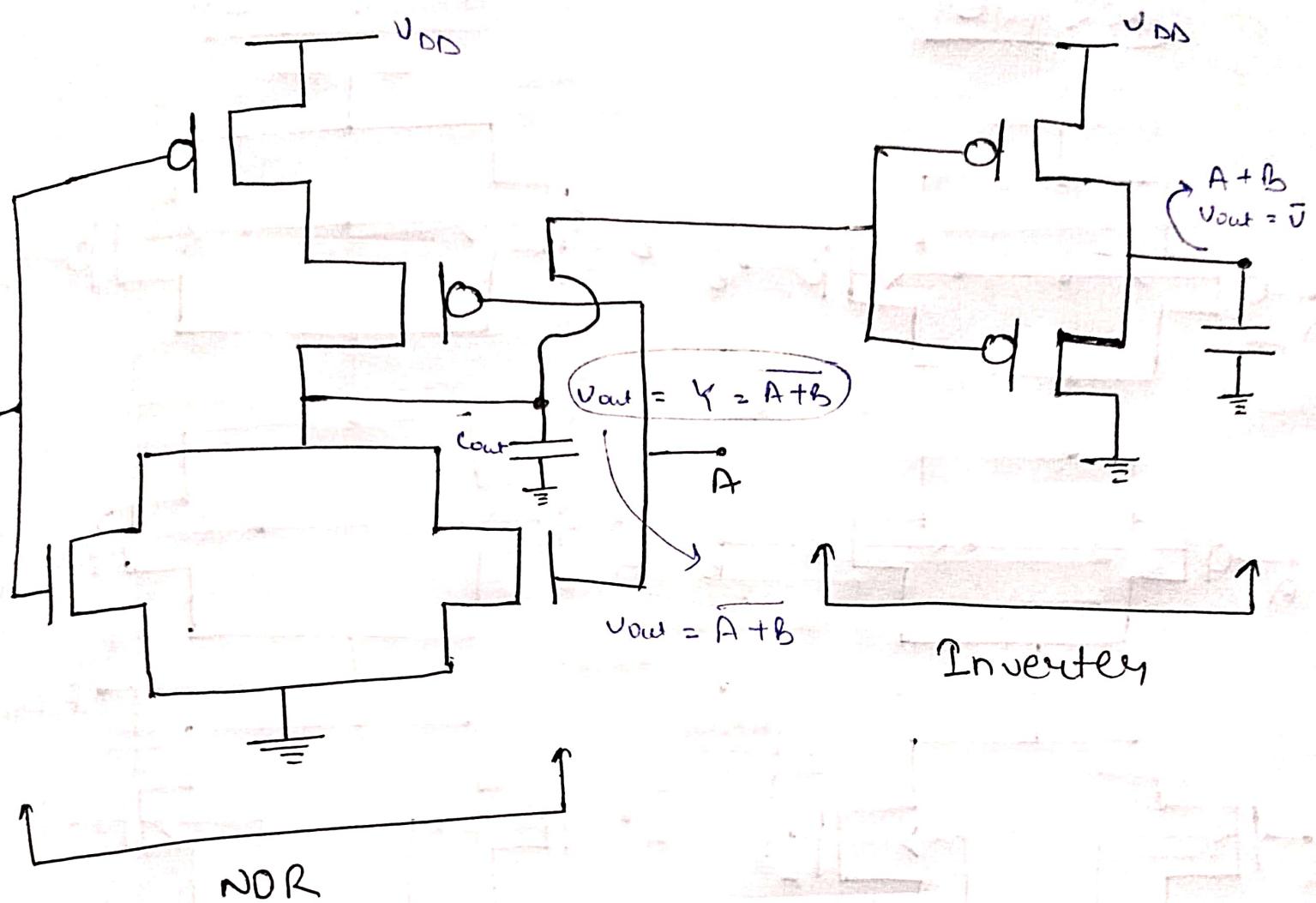


NAND Gate

Inverter

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

11. CMOS NOR Gate : $(A + B) \rightarrow 1$ & OR Gate :-



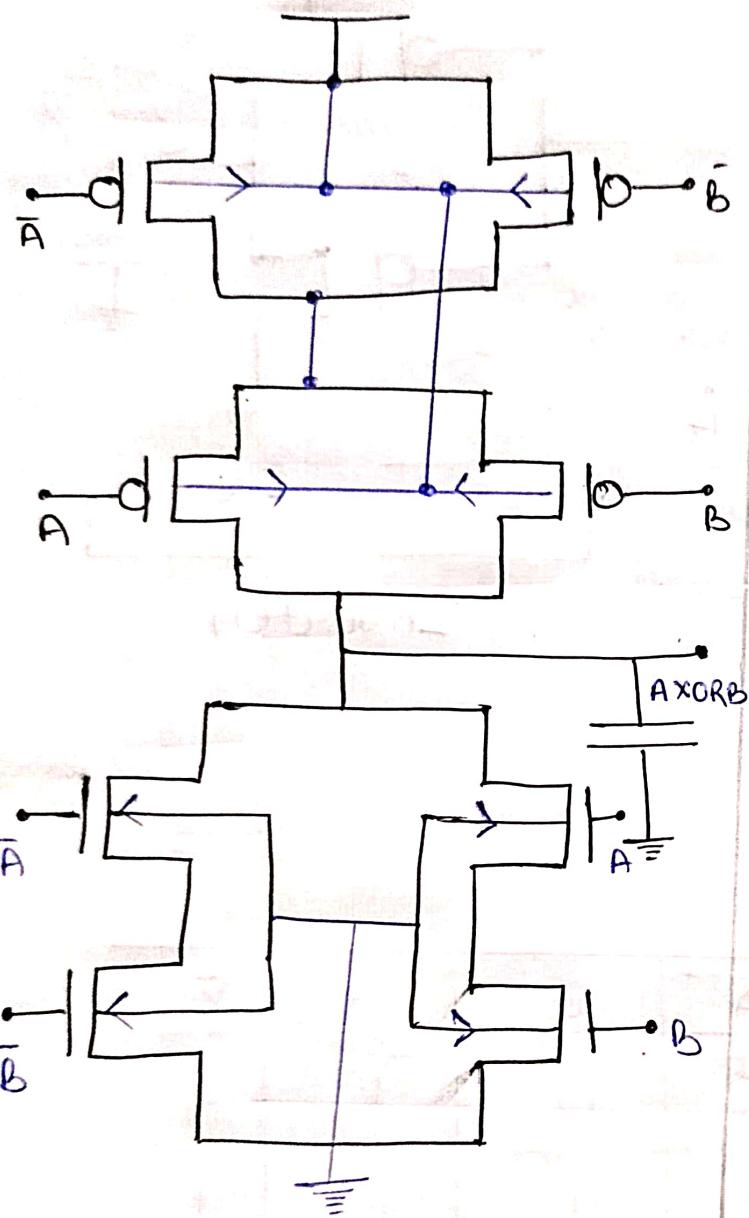
$$Y = \overline{A+B}$$

$$\bar{Y} = A+B$$

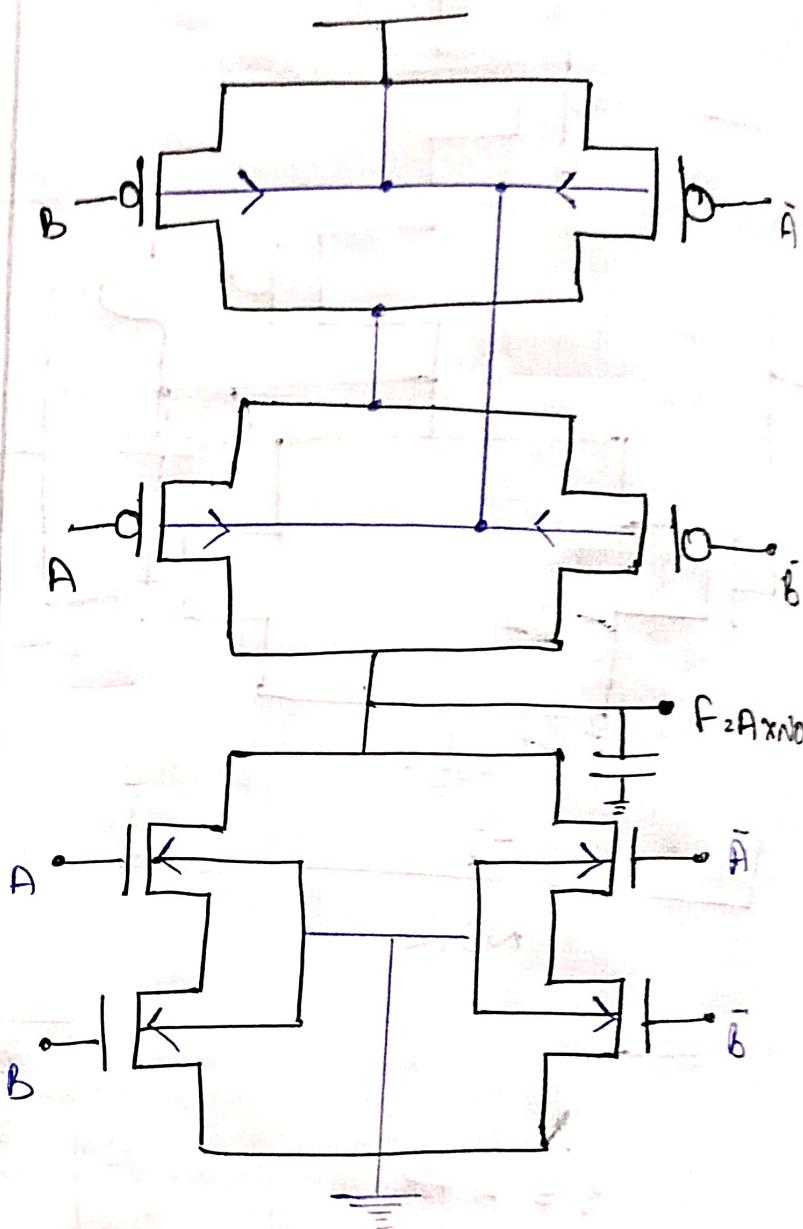
A	B	Y	\bar{Y}
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

19. CMOS AS XOR Gate & 20. XNOR Gate

[XOR gate]



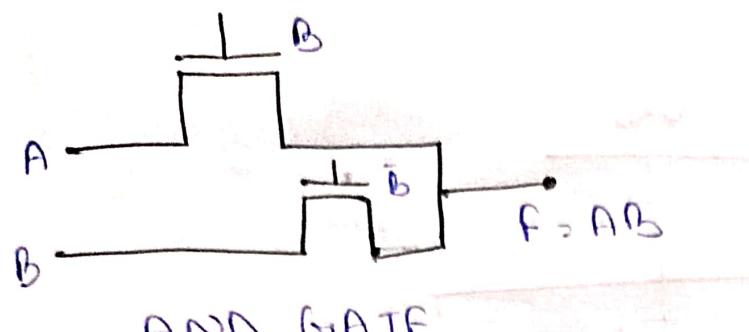
[XNOR gate]



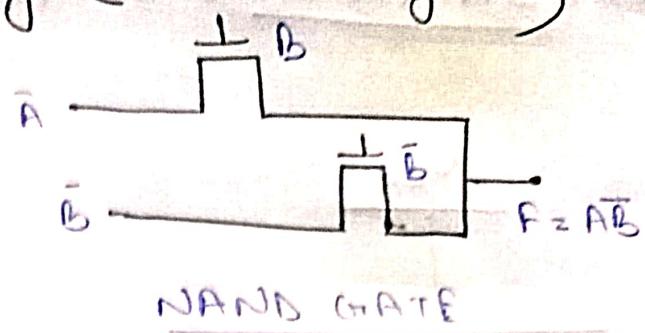
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

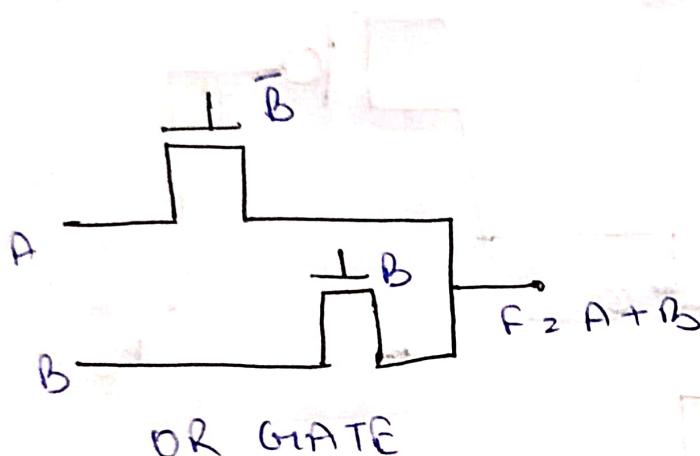
21. Pass Transistor logic of (all above gates)



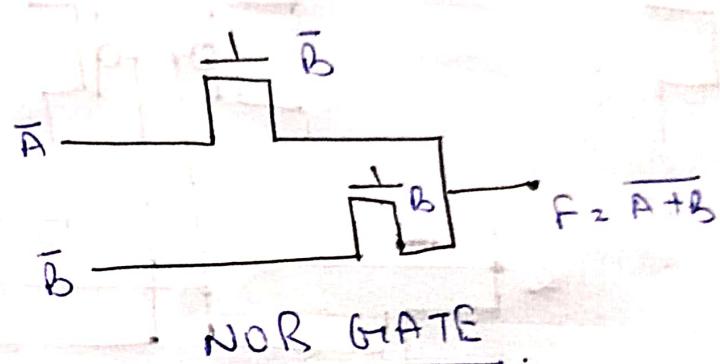
AND GATE



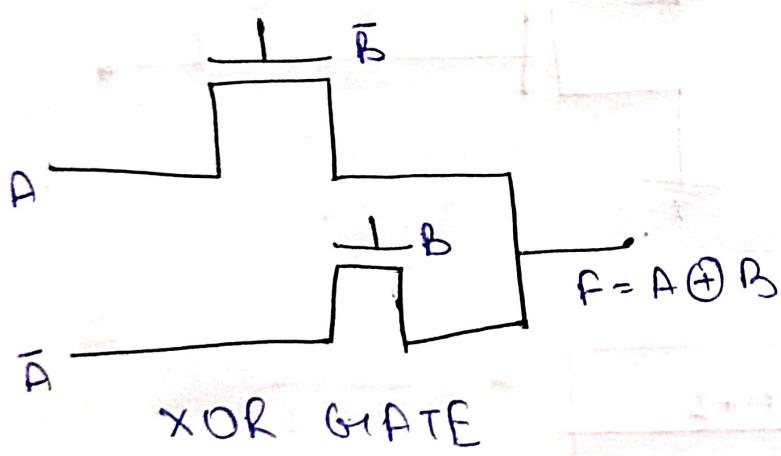
NAND GATE



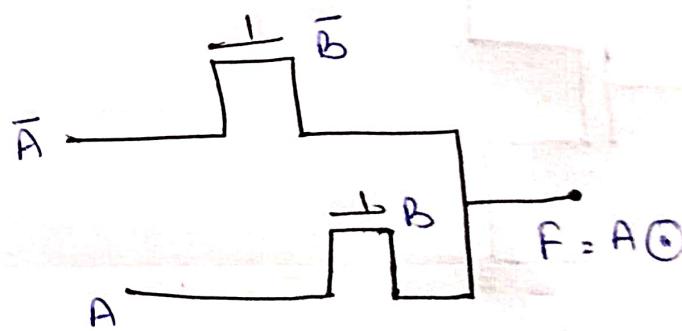
OR GATE



NOR GATE

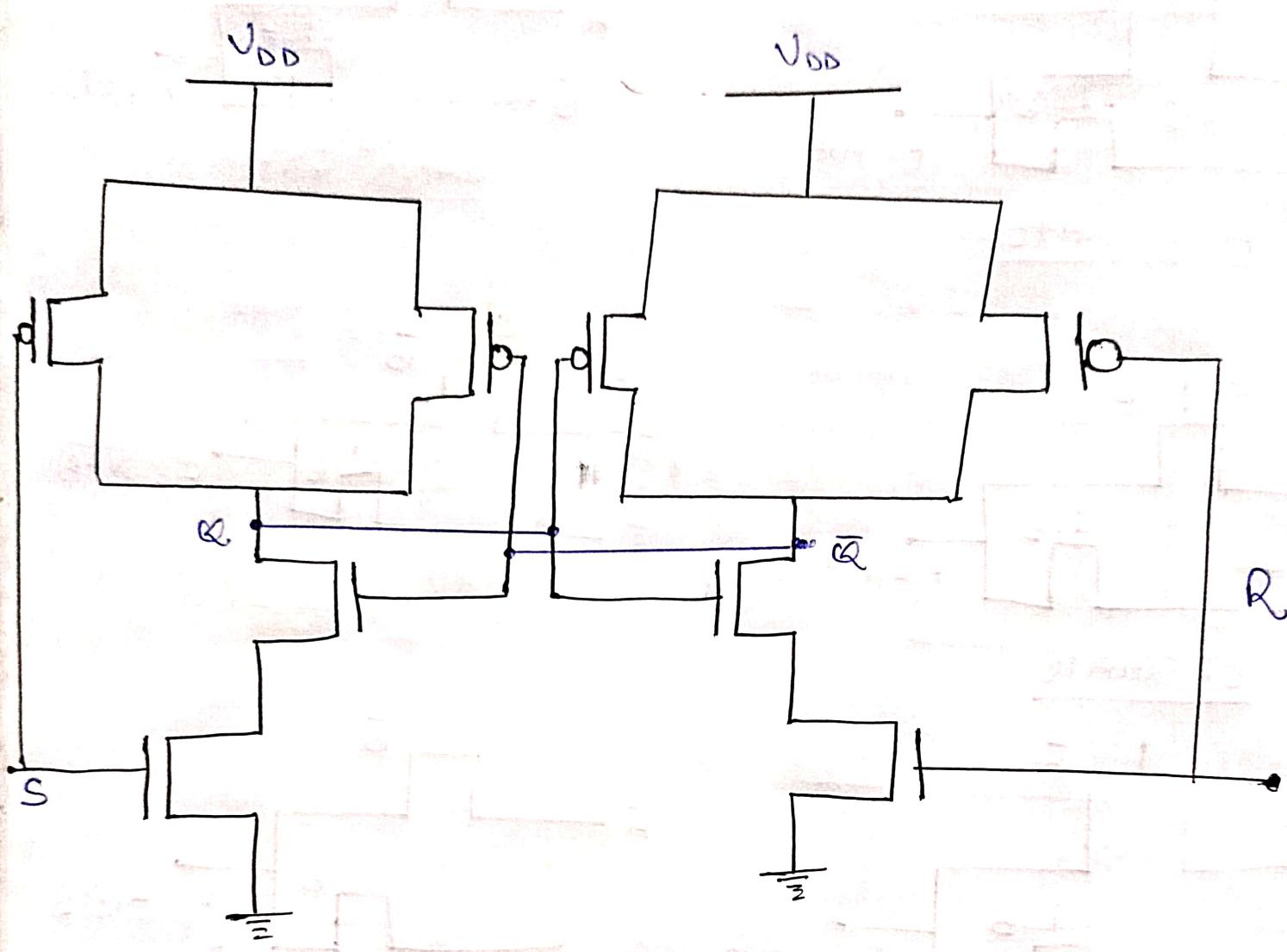


XOR GATE



XNOR GATE

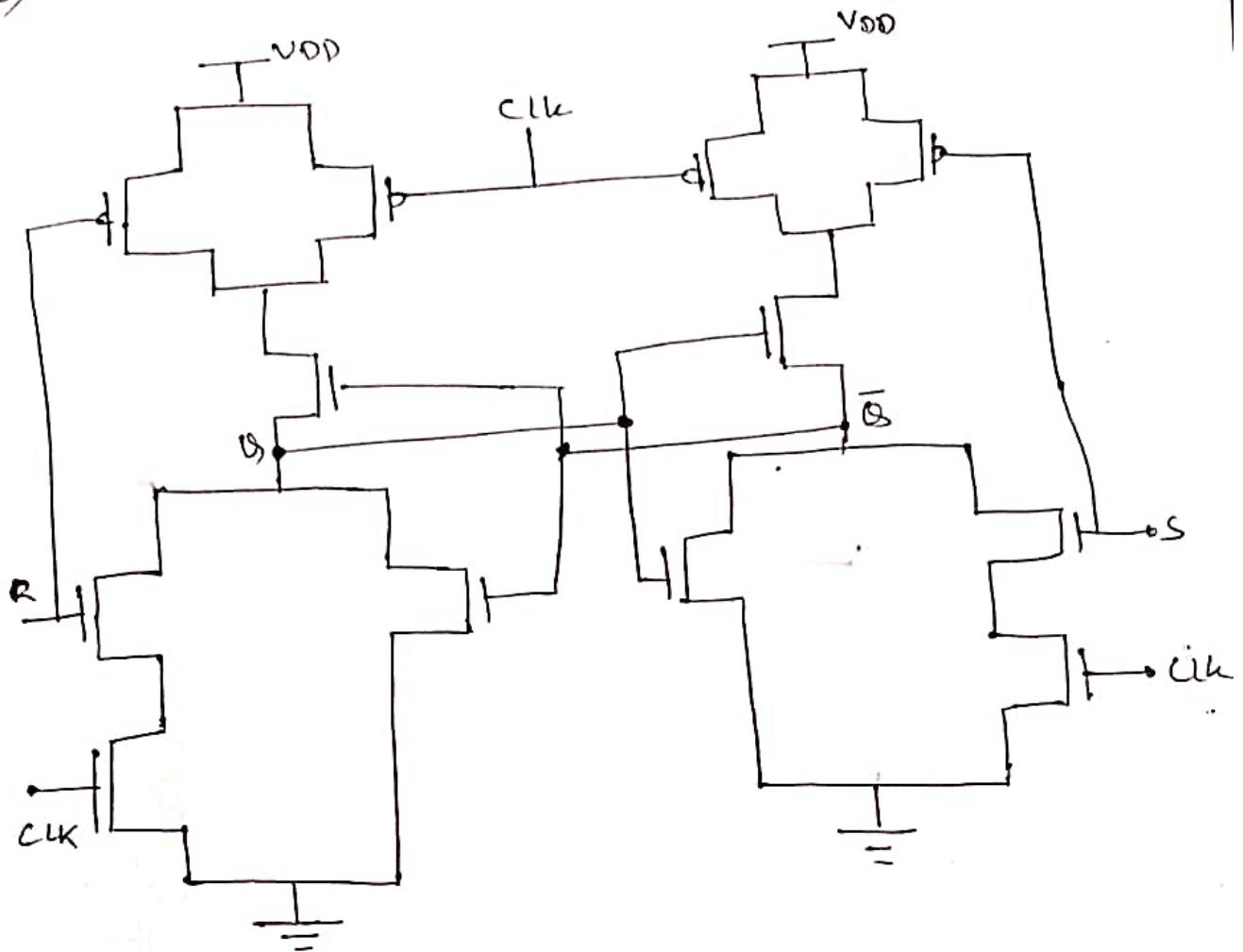
22. SR Latch : (21/P NAND gate)



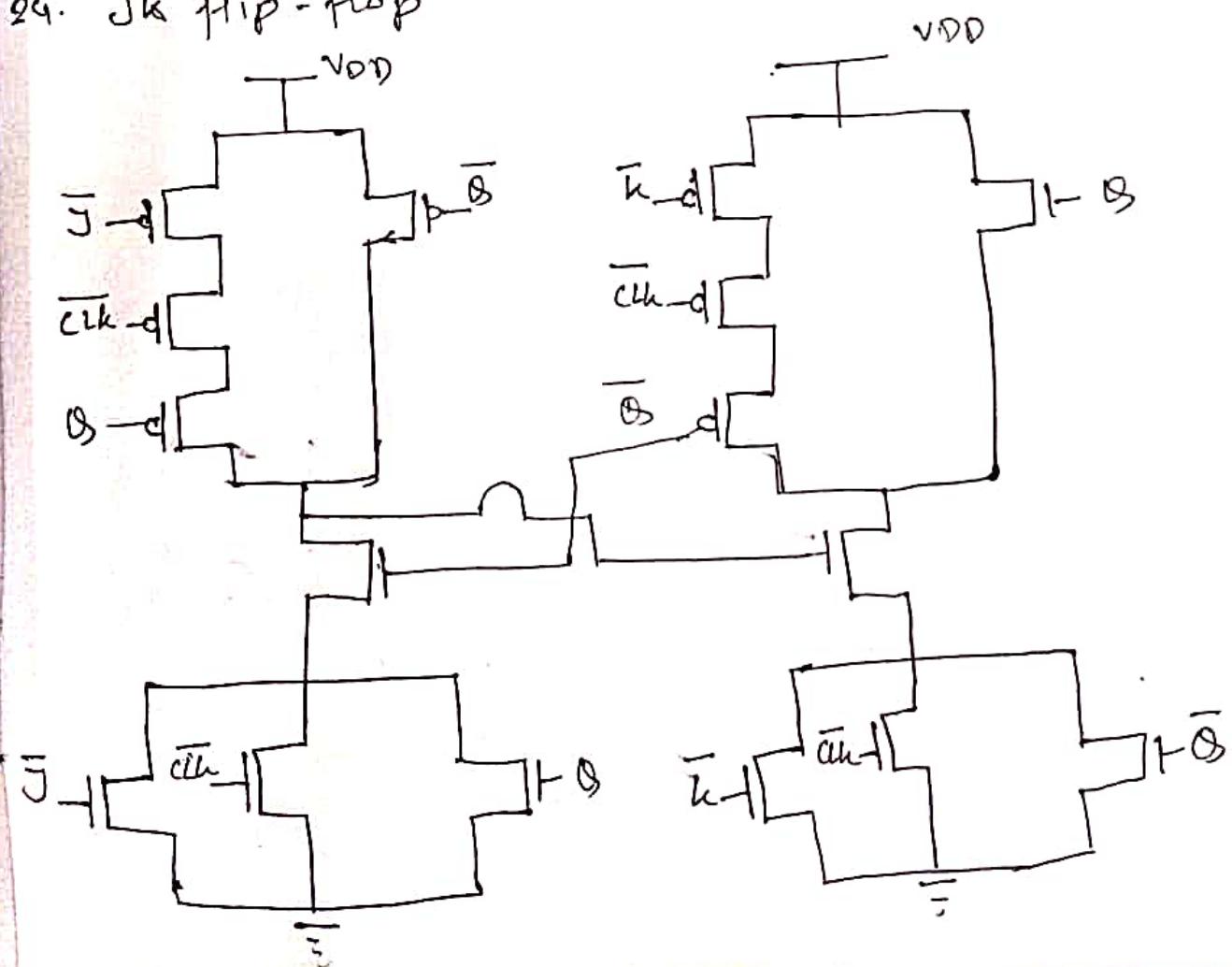
S	R	Q_{n+1}
0	0	invaled
0	1	1
1	0	0
1	1	Q_n

Truth Table

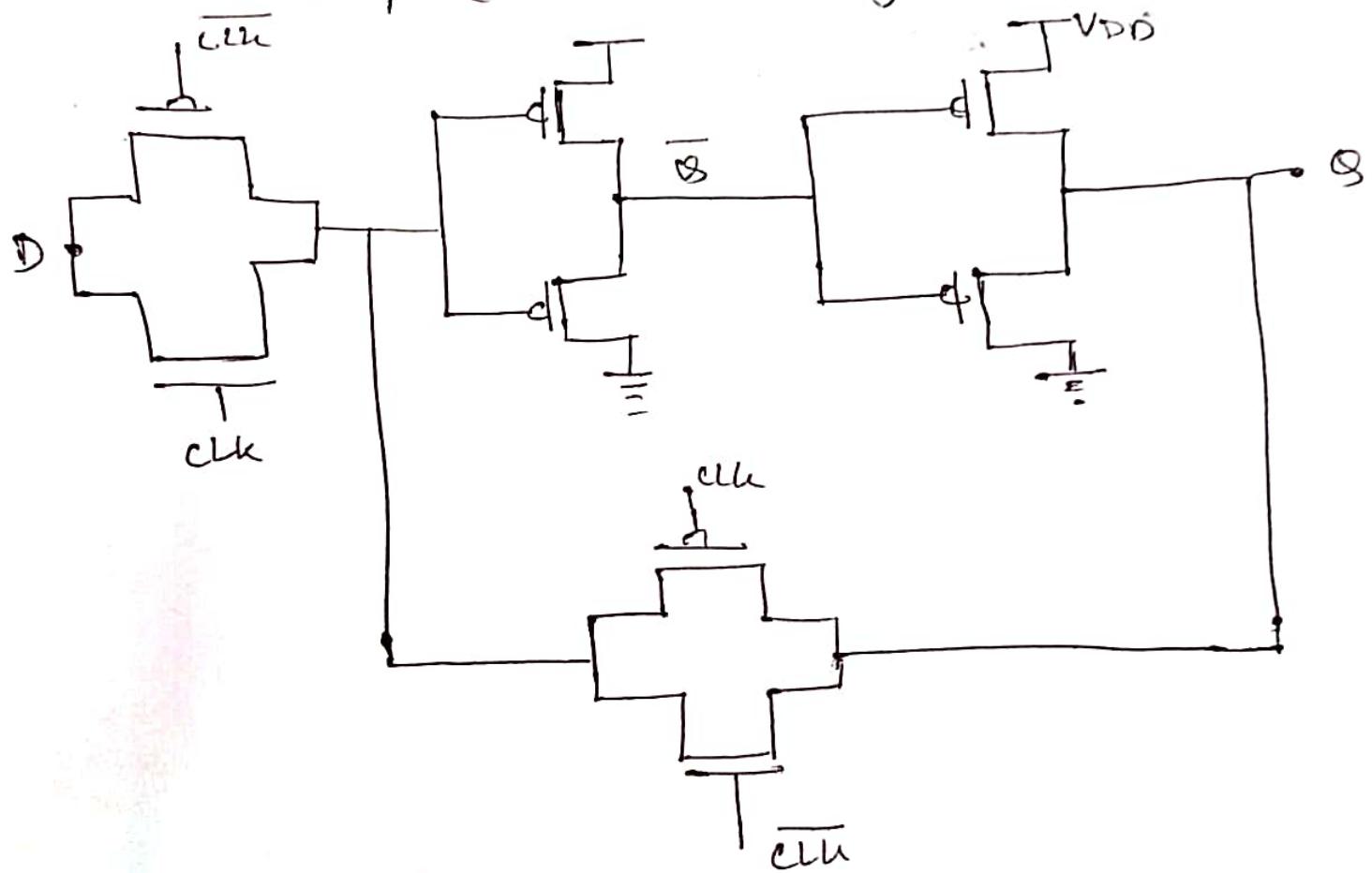
23) SR Flip-flop



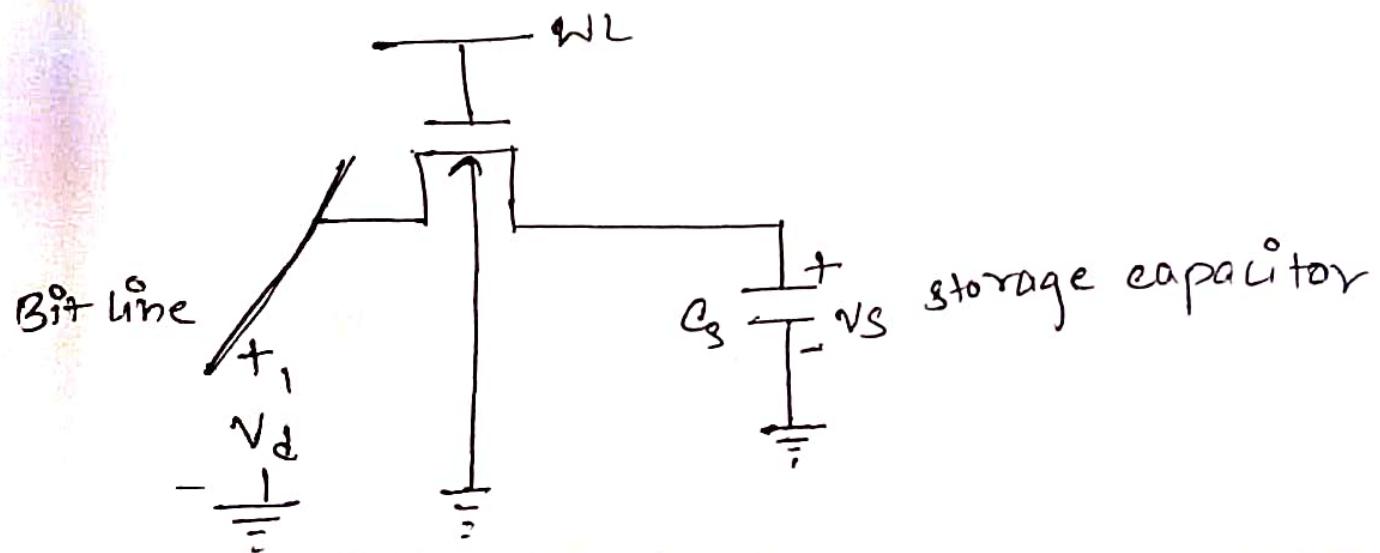
24. JK Flip-flop



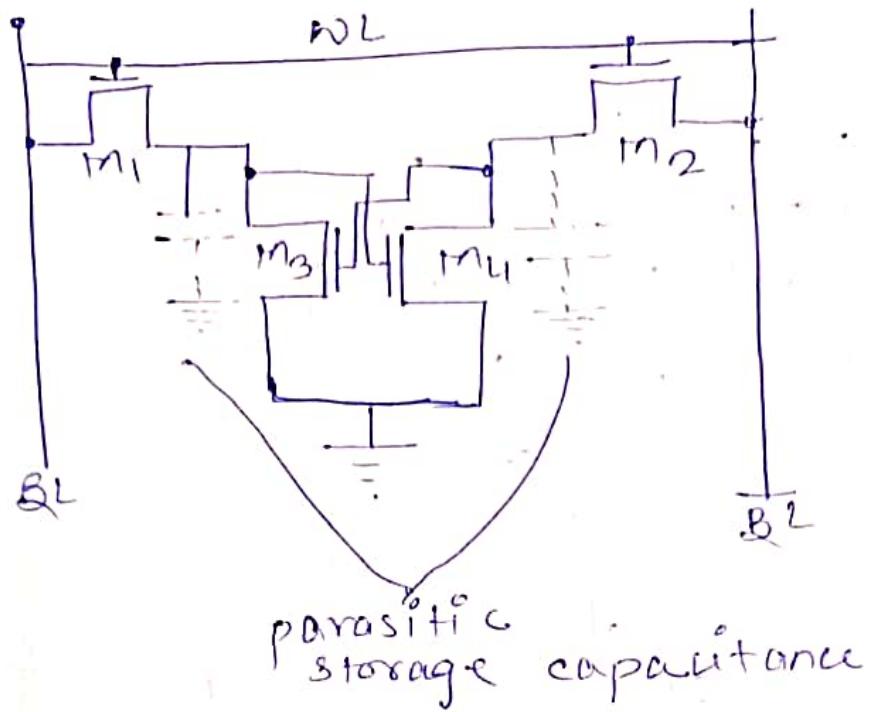
25) D flip flop (Transmission gate circuit)



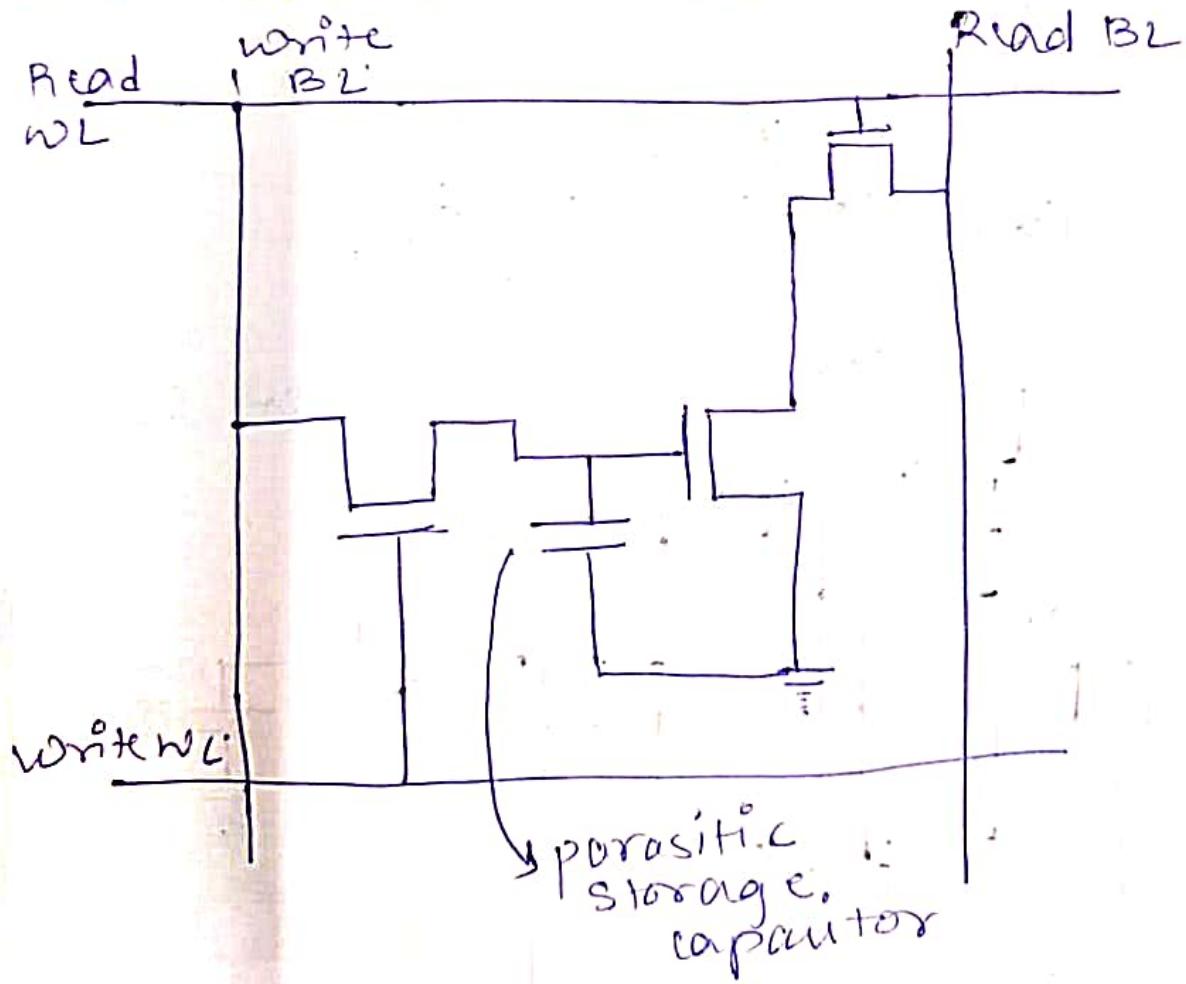
26) IT DRAM cell (one transistor DRAM cell)



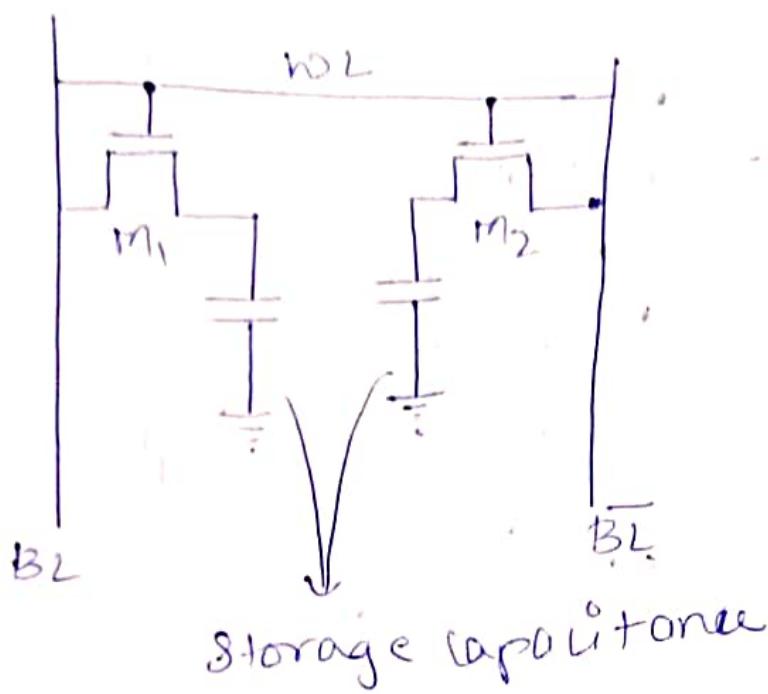
27) 4T DRAM cell (four transistor DRAM cell)



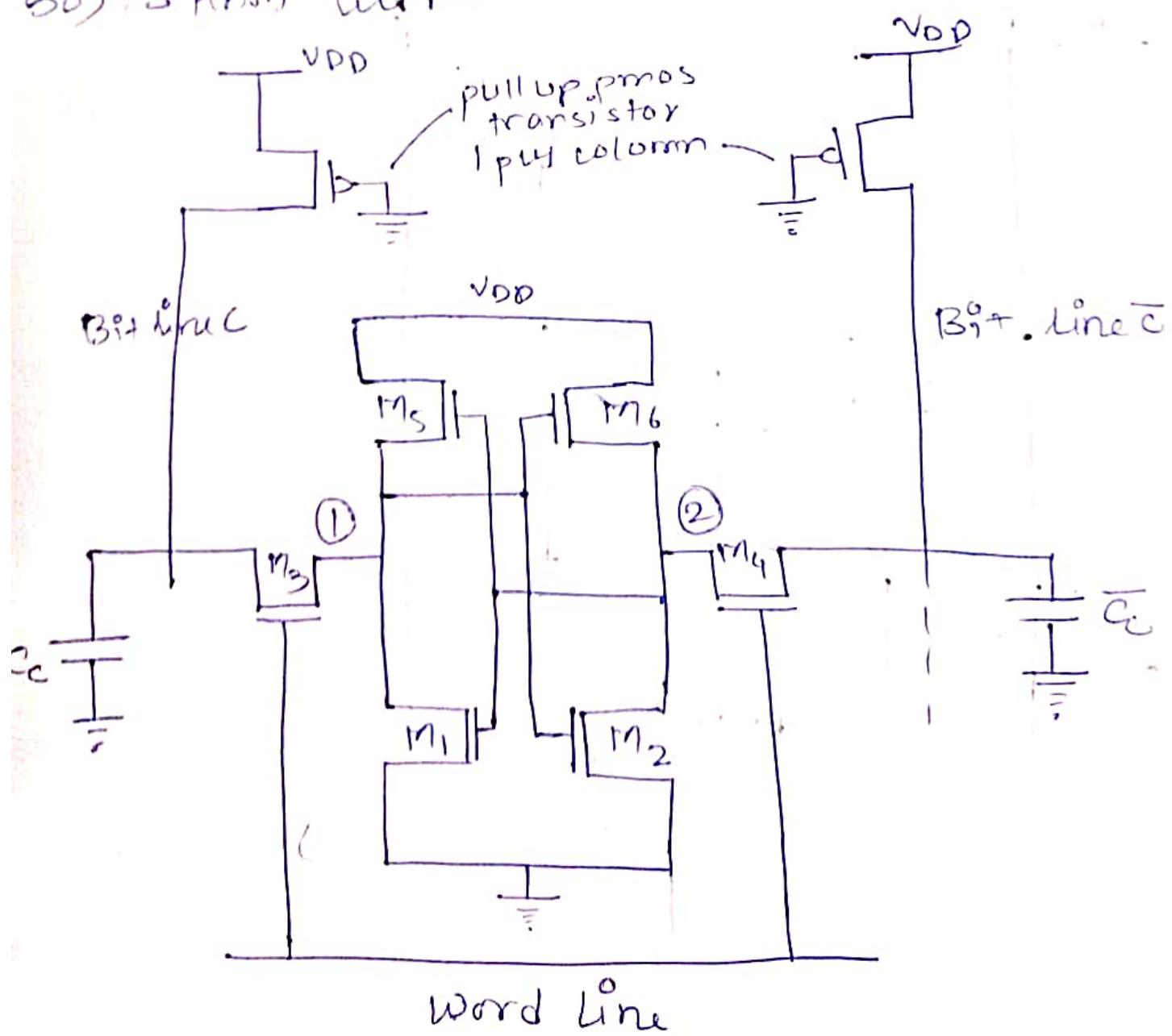
28) Three transistor DRAM cell



2A) 2T DRAM cell (Two-transistor DRAM cell)



3D) SRAM cell :-



3D ROM Model

