COMPSYS 304 - Assignment 3 Report

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Processor name

`Intel Core i7 7500U`

Cache sizes

There is no L4 cache in this processor, L1 is split by data and instruction. L3 is the only shared cache, there is two of the L2 and both L1s for each physical core. For sizes of each cache refer to Figure 1

```
LEVEL1_ICACHE_SIZE                 32768
LEVEL1_DCACHE_SIZE                 32768
LEVEL2_CACHE_SIZE                  262144
LEVEL3_CACHE_SIZE                  4194304
```

Figure 1: Extract from "getconf -a | grep CACHE_SIZE"

1 Cache measurement

N repetitions	size of a / bytes	time per iteration / ns	time per iteration / ns
		linear access	random access
1,000,000	8192	0.43	0.58
500,000	16,384	0.42	0.58
250,000	32,768	0.42	0.63
125,000	65,536	0.43	0.75
62,500	131,072	0.43	0.94
31,250	262,144	0.42	1.10
15,625	524,288	0.42	1.51
7812	1,048,576	0.43	4.07
3906	2,097,152	0.48	7.43
1953	4,194,304	0.50	9.33
976	8,388,608	0.51	10.35
488	16,777,216	0.50	10.90

Figure 2: Results of running cachetest1 and cachetest2

2 Matrix product

As per the assignment specification the matrices were all of size 1000x1000

2.1 Naive implementation

2.2 Temporary matrix

2.3 Blocking and temporary matrix

I started at a block size of 16