COMPSYS 304 - Assignment 3 Report

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1 Cache measurement

1.1 Linearly

1.2 Randomly

2 Matrix product

As per the assignment specification the matrices were all of size 1000x1000

2.1 Naive implementation

2.2 Temporary matrix

2.3 Blocking and temporary matrix

I found afte

Appendix

Hardware used

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i7 7500U

2 physical, 4 logical cores

Socket Designation: L1 Cache
Operational Mode: Write Back
Maximum Size: 128 kB
Associativity: 8-way Set-associative

Socket Designation: L2 Cache
Operational Mode: Write Back
Maximum Size: 512 kB
Associativity: 4-way Set-associative

Socket Designation: L3 Cache
Operational Mode: Write Back
Maximum Size: 4096 kB
Associativity: 16-way Set-associative
```

Software used

```
Ubuntu 16.04

GCC 5.4 with -O1 flag
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