**Tenstorrent** **January 2022 – May 2022**

*Design Verification Intern – RISC-V CPU Team (Full-time)* *Austin, TX*

- Compiled and modified Google's open-source System Verilog *riscv-dv* random instruction generator to create tests
- Constrained tests to help build testbenches for different blocks and ran this stimuli on VCS and Whisper to ensure functionality
- Migrated Tenstorrent's enhancements of the vector, floating point, load/store units - and more - to Google's head commit
- Generated diagrams in React using Python and data from SQL to visualize the RTL interfaces; streamlining testbench generation