Masaad Khan

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WORK EXPERIENCE

Intel **May 2022 – August 2022**

Xeon SoC Pre-silicon Verification Intern (Full-time) *Remote*

- The individual entries are indicated with a black dot, a so-called bullet

Tenstorrent **January 2022 – May 2022**

Design Verification Intern – RISC-V CPU Team (Full-time) *Austin, TX*

- Compiled Google's open-source System Verilog RISC-V DV toolkit and modified it to generate tests useful to Tenstorrent - familiarized myself with UVM
- Migrated Tenstorrent's enhancements to the vector, floating point, and more units to Google's head commit
- Produced testbenches using RISC-V DV and ran them in VCS and whisper (RISC-V ISS) to ensure no system breaking changes
- Generated diagrams in React using Python and data from SQL to describe our RTL interfaces; streamlines testbench generation

Tesla **January 2021 – August 2021**

Silicon Development Intern – Autopilot Hardware Group (Full-time) *Palo Alto, CA*

- Completed working voltage sensor and SPI drivers despite a complicated bug in Tesla's SPI silicon
- Implemented and rigorously tested a software architecture designed to funnel temperature and voltage data over SPI
- Improved a python script to recursively parse generated protobuf, automated sending protobuf messages by filling a .JSON/.proto file, and synced this script as well as the hardware based on messages received over UART
- Created a python script able to generate QSPI images working around the LittleFS library, which used linux-like commands
- Gained experience writing firmware running ARM CMSIS RTOS wrapper for FreeRTOS, including drivers, interrupt handlers, etc

RESEARCH

Wireless Networking and Communications Group - UT Austin **August 2021 – Present**

Undergraduate Researcher *Austin, TX*

- Generated image datasets of Airsim drone simulations in Unreal Engine using C++ and Python; made to help train a CV model
- Coordinated with another undergraduate student to deliver object-detection using MobilenetV2 on the Jetson Nano
- Provided a networking stack to detect latency for a center-less cloud of Jetson Nanos using ZeroMQ and Google Protobuf
- Worked closely with a PhD student under researching In/Out of Distribution inputs to neural networks

PROJECTS

Cycle-level CPU Simulation **August 2021 – Decenmber 2021**

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SKILLS

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- System Verilog, C, Verilog, C++, Python, Perl, Latex