Tenstorrent **January 2022 – May 2022**
Design Verification Intern – RISC-V CPU Team (Full-time) *Austin, TX*

- Compiled Google's open-source System Verilog RISC-V DV toolkit and modified it to generate tests useful to Tenstorrent
- - familiarized myself with UVM
- Migrated Tenstorrent's enhancements to the vector, floating point, and more units to Google's head commit
- Produced testbenches using RISC-V DV and ran them in VCS and whisper (RISC-V ISS) to ensure no system breaking changes

- Generated diagrams in React using Python and data from SQL to describe our RTL interfaces; streamlines testbench generation