HARDWARE IMPLEMENTATION OF CONVOLUTION NEURAL NETWORK AS PART OF SOC DESIGN FOR ECG ANALYSIS AND CLASSIFICATION

2025 ENGINEERING DESIGN PROJECT (GK02)

FACULTY LAB COORDINATOR

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PREAMBLE

SoPC (FPGA based SoC) have transpired in response to the performance limitations of CPU-based multi-core System-on-Chip (SoC) architectures. SoPC provides dedicated hardware accelerators to improve overall system performance for many applications. Electrocardiogram (ECG) records the electrical signal from the heart to check for different heart conditions. Application oriented hardware accelerator(s) such as Convolutional Neural Network (CNN) working along with the CPU will result in a successful high performance SoC implementation for ECG signal analysis and Classification.

OBJECTIVE

Investigate an FPGA based SoC involving faster (hardware) CNN core to perform ECG Signal Analysis and Classification.

PARTIAL SPECIFICATIONS

1. Study typical electrocardiogram (ECG) signals for a human heart to check for different human heart conditions.
2. Investigate and identify a suitable SoPC based on either Intel Altera (e.g., DE1-SoC) or AMD-Xilinx (Zynq-7000) SoCs.
3. Investigate ECG signal analysis algorithms/techniques and identify some of its computationally intensive parts such as CNN (Convolutional Neural Network).
4. Hardware (HDL) implementation of the CNN part for ECG classification.
5. Implement the rest of ECG analysis algorithm to be executed on the CPU.
6. Hardware-Software implementation using the CPU cores (e.g., Cortex A9) and hardware accelerators for CNN.
7. Verify the working of ECG classification system for a data-set of typical ECG signals to detect various heart conditions.

SUGGESTED APPROACH

1. Study and analysis of electrocardiogram (ECG) signals for a human heart.
2. Investigate and evaluate SoC architectures and programming models by exploring Intel (Altera) Cyclone IV/V (or AMD-Xilinx) based FPGA platforms for developing the SoC system for ECG signal analysis and classification.
3. CPU (all software) implementation of the ECG analysis technique involving CNN.
4. HDL (hardware) implementation of computationally intensive part (such as CNN) of the ECG analysis method.

5. Hardware-Software design of the SoC involving the CPU (software) and hardware accelerator for the CNN part.
6. Prototyping, implementation, and verification (testing) of the SoC implementation of ECG classification by employing some available human ECG Data-sets.

GROUP RESPONSIBILITIES

1. Study on-chip ARM processors and programming models as well as FPGA based (Cyclone DE1-SoC or Xilinx Zynq SoC) embedded platform for ECG analysis related applications.
2. Investigate and study CNN based ECG classification techniques being investigated by various groups working on ECG signal analysis.
3. Develop a detailed specification of CNN based ECG analysis technique and its Hardware-software implementation.
4. Design, develop and prototype the CNN based ECG classification technique for the FPGA based SoC platform.
5. Verify the Hardware-Software design of the ECG signal analysis technique.
6. Final Implementation of the hardware (HDL) accelerator for CNN part and Software (e.g., Cortex A9 CPU) implementation of the other parts of ECG analysis.
7. Verify and evaluate the working of ECG classification technique for various ECG data-sets.

STUDENT A RESPONSIBILITIES

1. Study some candidate SoPC-based platforms for ECG analysis and classification implementation.
2. Investigate and study ECG classification techniques involving CNN being used by various groups.
3. Identify computationally intensive parts of the selected ECG analysis technique such as CNN and its HDL (hardware) design.
4. Develop a detailed specification of ECG analysis and its Hardware-Software verification in using a language (such as C++ or SystemC).
5. Develop the overall SoPC design for ECG classification with the collaboration of students B, C and D.
6. Verify the hardware design of CNN and your overall ECG analysis design by working with the other students B, C and D.

STUDENT B RESPONSIBILITIES

1. Investigate some candidate ARM processor-based SoC platforms such an AMD Xilinx Zynq 7000 or Intel Altera DE1-SoC.
2. Investigate and study ECG classification techniques involving CNN being used by various groups.
3. Assist student A to identify and implement computationally intensive parts such as CNN of the ECG analysis/classification technique and its HDL (hardware part) design.
4. Work with student A to develop a detailed specification of ECG classification and its Hardware-Software partitioning and verification in a co-specification language such as SystemC, etc.
5. Develop the overall SoPC design for ECG classification with the collaboration of students A, C and D.
6. Collaborate with students A, C and D to manage the overall project design and implementation.

STUDENT C RESPONSIBILITIES

1. Identify some candidate on-chip ARM processor-based FPGA (SoPC) platforms such as Zynq 7000, DE1-SoC, etc.
2. Work with student A and B to develop a detailed specification of the ECG analysis method involving CNN and its Hardware-Software verification in a high level language (such as SystemC).

3. Support students A and B with the verification and testing of the SoC system for ECG analysis and classification.
4. Collaborate with students A, B and D to manage the overall project design and implementation.

STUDENT D RESPONSIBILITIES

1. Study some candidate on-chip ARM processor-based FPGA (SoPC) platforms available for ECG signal analysis.
2. Investigate and study ECG classification techniques involving CNN being used by various groups.
3. Assist student A to identify and implement computationally intensive parts such as CNN of the ECG analysis/classification technique and its HDL (hardware part) design.
4. Design and establish communication in-between CPU and CNN (hardware) accelerator for the ECG signal analysis and classification application.
5. Develop and verify the overall SoC for ECG analysis by collaborating with students A, B and C.
6. Work with the other group members to manage the overall hardware/software design and SoC implementation for ECG signal analysis and classification.

COURSE CO-REQUISITES

COE718, COE838

(Submission time stamp: Thu Aug 28 2025 14:20:09 GMT-0400 (Eastern Daylight Time))