MAS_MULTIPLIER
REFERENCE DOCUMENT

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MAS_MULTIPLIER Description

The MAS_MULTIPLIER consists of SystemVerilog verification testbench for 2 different multiplier designs written in SystemVerilog. The multiplier designs are based on Radix 4 and Vedic algorithm. Both multiplier designs have the same inputs and outputs shown in the following diagrams:

RADIX 4 multiplier top level

VEDIC multiplier top level

Algorithm: Radix 4

Multiplier bits			Partial product
i_{+1}	i	i_{-1}	
0	0	0	0
0	0	1	+1*multiplicand
0	1	0	+1*multiplicand
0	1	1	+2*multiplicand
1	0	0	-2*multiplicand
1	0	1	-1*multiplicand
1	1	0	-1*multiplicand
1	1	1	0

Booth Encoding table for radix 4

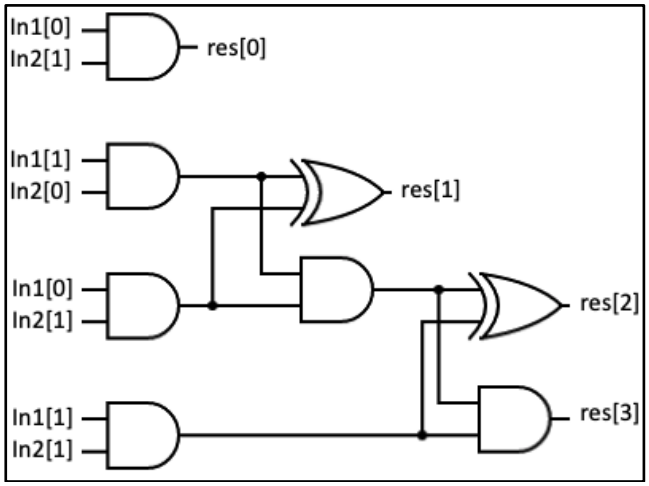
File List

File	Description
mas_mul_radix_top.sv	Top level file that wraps on encoder and adder modules.
mas_radix_encoder.sv	Perform booth encoding.
mas_radix_adder.sv	Perform addition or subtraction.

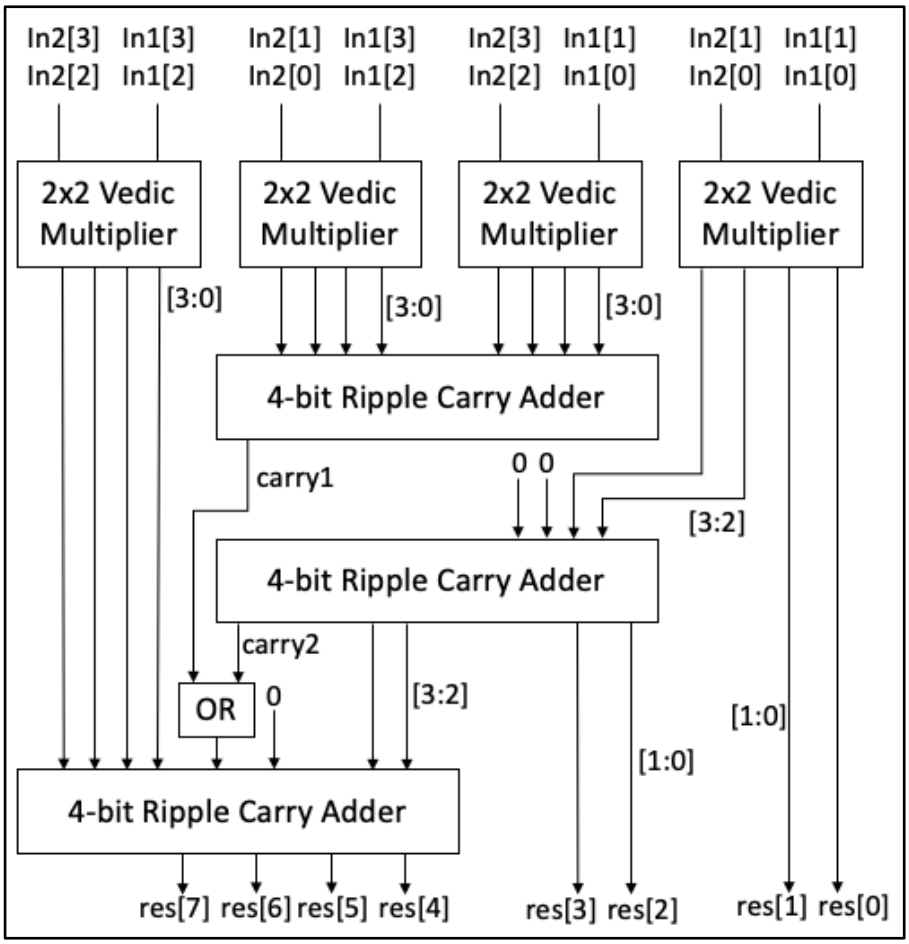
Testbench File List

File	Description
mas_mul_radix_tb.sv	Top testbench instantiating DUT & test.
mas_mul_program.sv	Initialize environment and run test.

Algorithm: Vedic

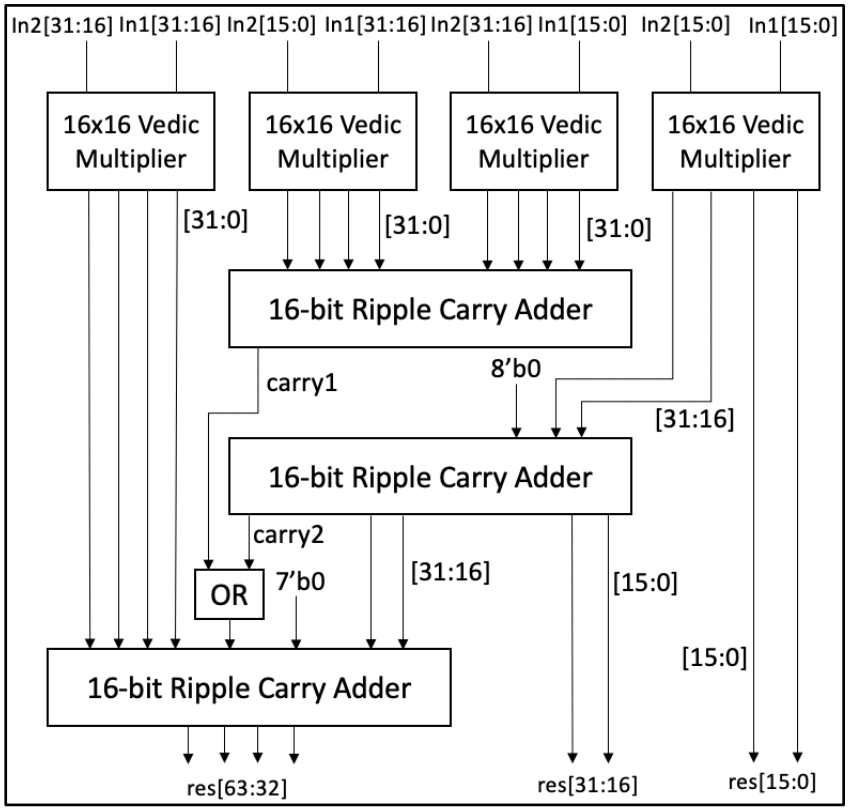


2x2 VEDIC multiplier module



4x4 VEDIC multiplier module

Using similar method constructing 4x4 VEDIC multiplier with 2x2 VEDIC multiplier, 32x32 VEDIC multiplier module is presented as follows:



32x32 VEDIC multiplier module

Design File List

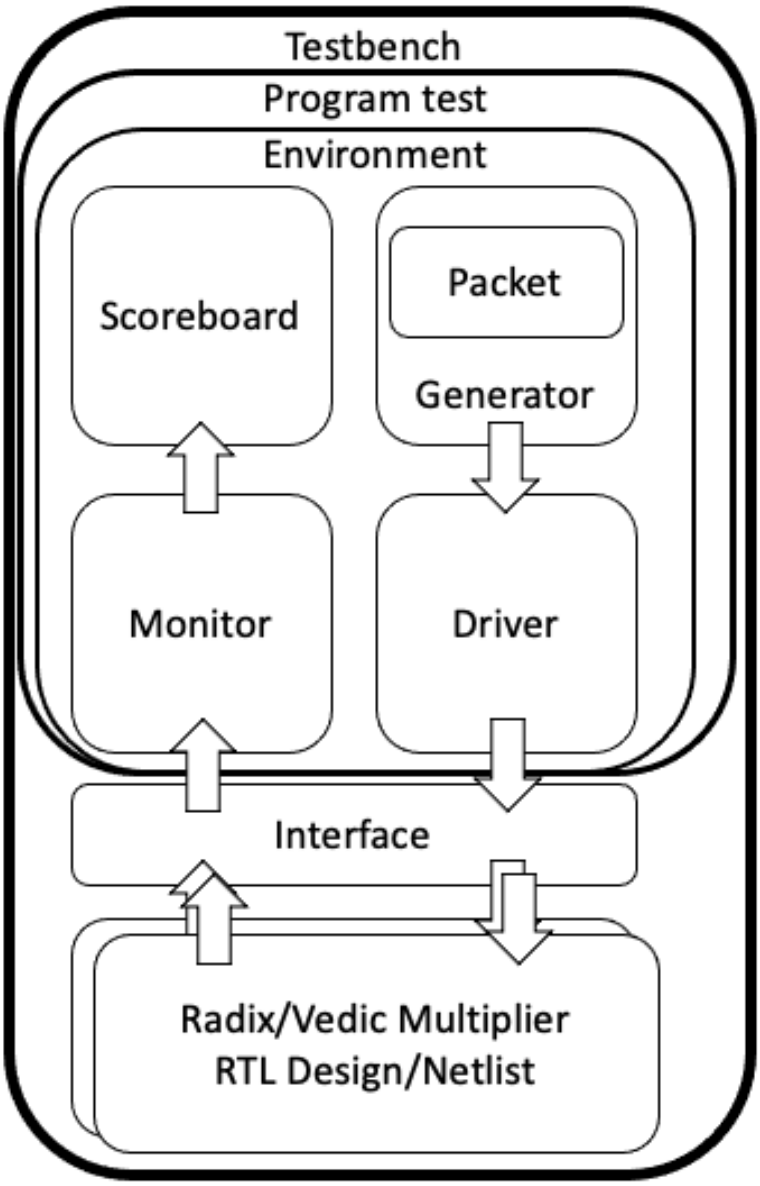
File	Description
mas_mul_vedic_32x32.sv	32 bits VEDIC multiplier
mas_mul_vedic_16x16.sv	16 bits VEDIC multiplier
mas_mul_vedic_8x8.sv	8 bits VEDIC multiplier
mas_mul_vedic_4x4.sv	4 bits VEDIC multiplier
mas_mul_vedic_2x2.sv	2 bits VEDIC multiplier
mas_ripple_carry_adder_32b.sv	32 bits ripple carry adder.
mas_ripple_carry_adder_16b.sv	16 bits ripple carry adder.
mas_ripple_carry_adder_8b.sv	8 bits ripple carry adder.
mas_ripple_carry_adder_4b.sv	4 bits ripple carry adder.

Testbench File List

File	Description
mas_mul_vedic_tb.sv	Top testbench instantiating DUT & test.
mas_mul_program.sv	Initialize environment and run test.

Testbench

The verification testbench includes verification IPs such as generator, driver, monitor and scoreboard that are reusable for both multipliers in RTL/Gate-level simulation.



Testbench Architecture

File List

File	Description
mas_mul_test_configuration.svh	Contains macros for test configuration
mas_mul_packets.sv	Classes containing design inputs & output with constraints.
mas_mul_generator.sv	Class containing stimulus generation task for random and specific test.
mas_mul_driver.sv	Class containing stimulus driving task for random and specific test.
mas_mul_monitor.sv	Class containing design output monitoring task for random and specific test.
mas_mul_scoreboard.sv	Class containing task for design output functionality check and print to file for post-processing.
mas_mul_environment.sv	Groups all components for verification
mas_mul_interface.sv	Interface construct for connectivity with design in testbench.