1. Description

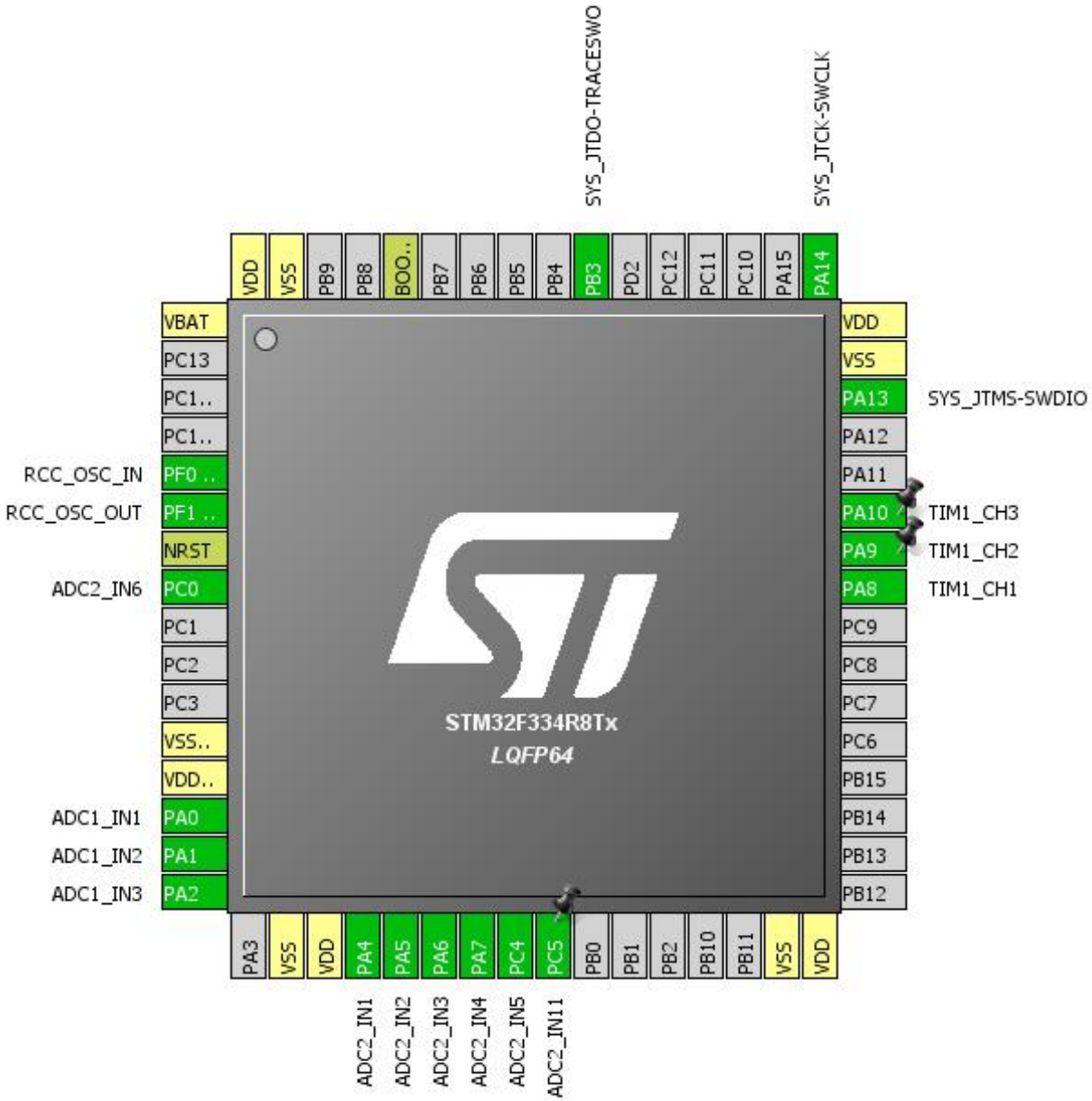
1.1. Project

Project Name	Tri-SPWM
Board Name	Tri-SPWM
Generated with:	STM32CubeMX 4.22.0
Date	08/10/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F334
MCU name	STM32F334R8Tx
MCU Package	LQFP64
MCU Pin number	64

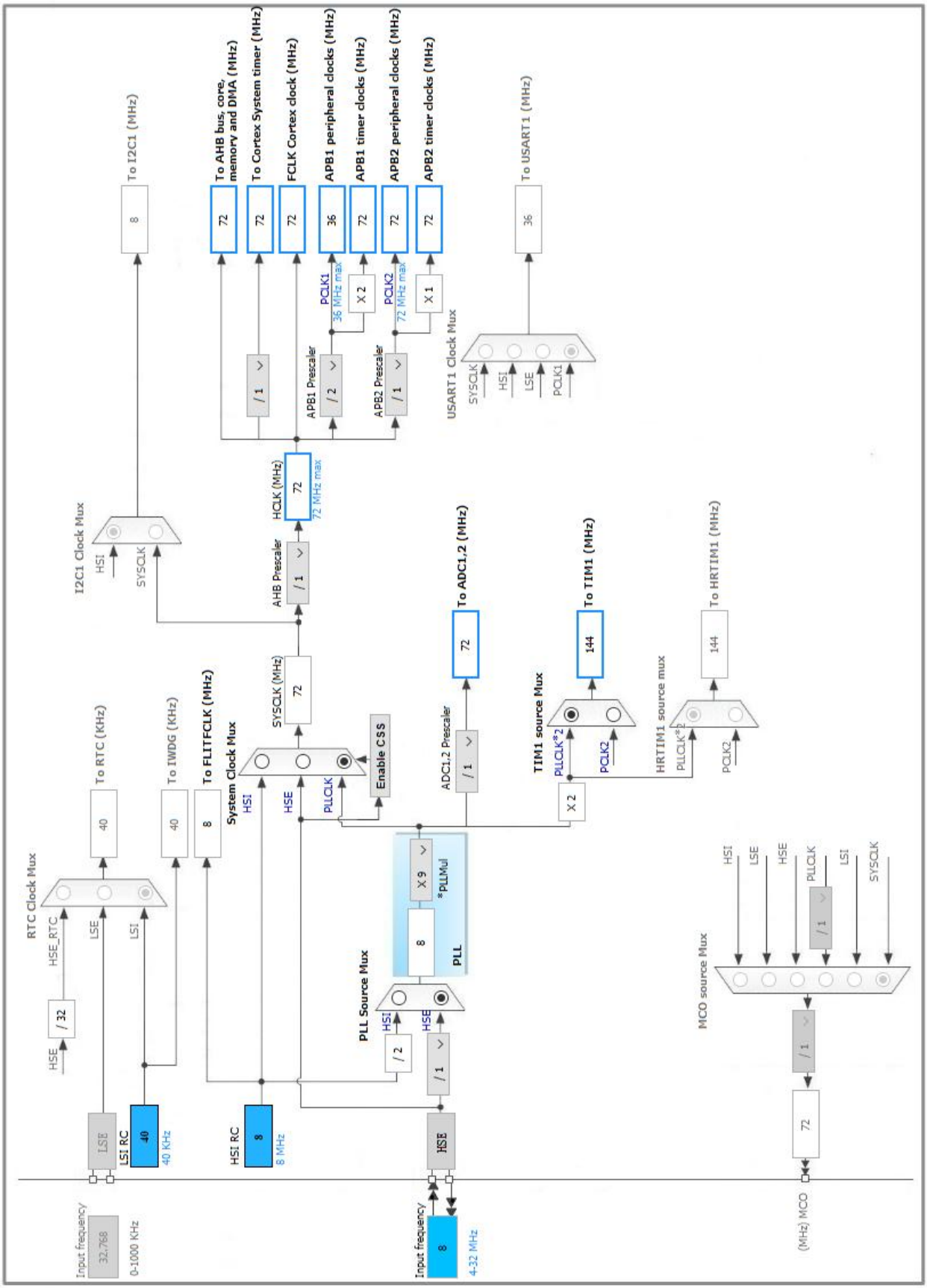
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0 / OSC_IN	I/O	RCC_OSC_IN	
6	PF1 / OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC2_IN6	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	ADC1_IN1	
15	PA1	I/O	ADC1_IN2	
16	PA2	I/O	ADC1_IN3	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC2_IN1	
21	PA5	I/O	ADC2_IN2	
22	PA6	I/O	ADC2_IN3	
23	PA7	I/O	ADC2_IN4	
24	PC4	I/O	ADC2_IN5	
25	PC5	I/O	ADC2_IN11	
31	VSS	Power		
32	VDD	Power		
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
55	PB3	I/O	SYS_JTDO-TRACESWO	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	**3 ***
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	**Disable ***

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	**3 ***
External Trigger Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Injected Conversion Mode	**Discontinuous Mode ***
Queue Injected Context Mode	Injected Queue enabled with Mode 0 (2 contexts, last active)
Rank	1
Channel	Channel 1
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Injected Offset	0
Rank	

	2 *
Channel	**Channel 2 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Injected Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Injected Offset	0
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN1: IN1 Single-ended
IN2: IN2 Single-ended
IN3: IN3 Single-ended
IN4: IN4 Single-ended
IN5: IN5 Single-ended
IN6: IN6 Single-ended
IN11: IN11 Single-ended

5.2.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***

Number Of Discontinuous Conversions	**6 ***
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**6 ***
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 5 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 11 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset

Offset	0
ADC_Injected_ConversionMode:	
Enable Injected Conversions	**Disable ***
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:	
VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)
RCC Parameters:	
HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.4. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM7

5.5. TIM1

Trigger Source: ITR0

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3599 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	**3 ***
auto-reload preload	**Enable ***
Slave Mode Controller	Slave mode disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.6. TIM6

mode: Activated

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**359 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

5.7. FREERTOS

mode: Enabled

5.7.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	**Disabled ***
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	**Enabled ***
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	**Dynamic / Static ***
TOTAL_HEAP_SIZE	3072
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.7.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled

vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	
ADC2	PC0	ADC2_IN6	Analog mode	No pull up pull down	n/a	
	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	
	PA5	ADC2_IN2	Analog mode	No pull up pull down	n/a	
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	
	PC4	ADC2_IN5	Analog mode	No pull up pull down	n/a	
	PC5	ADC2_IN11	Analog mode	No pull up pull down	n/a	
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1 / OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull up pull down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC2	DMA1_Channel2	Peripheral To Memory	Low

ADC2: DMA1_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel2 global interrupt	true	5	0
TIM1 update and TIM16 interrupts	true	0	0
TIM6 global and DAC1 underrun error interrupts	true	0	0
TIM7 global and DAC2 underrun error interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 trigger and commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F334
MCU	STM32F334R8Tx
Datasheet	025409_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Tri-SPWM
Project Folder	D:\Game\Tri-SPWM
Toolchain / IDE	EWARM
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No