Design of a 1.2V LDO for 1mA-25mA Load Range in 0.18μm CMOS

Error Amplifier Architecture

The output impedance due to load regulation is approximately:

$$\text{Load Regulation} \approx \frac{r_{dsp}}{1+T_0} \approx \frac{r_{dsp}}{A_{EA0} \cdot g_{mp} \cdot r_{dsp} \cdot \beta} = \frac{1}{A_{EA0} \cdot g_{mp} \cdot \beta}$$

To meet the specification:

$$\frac{1}{A_{EA0} \cdot g_{mp} \cdot \beta} \leq 50\,\mu\text{V/mA} = 0.05$$
$$\Rightarrow A_{EA0} \cdot g_{mp} \cdot \beta \geq 20$$

Given:

$$g_{mp} \approx 20\,\text{mS}, \quad \beta = \frac{2}{3} \Rightarrow A_{EA0} \cdot 20 \times 10^{-3} \cdot \frac{2}{3} \geq 20 \Rightarrow A_{EA0} \geq 1500$$

The line regulation is approximated by:

$$\text{Line Regulation} \approx \frac{1}{A_{EA0} \cdot \beta} \leq 500\,\mu\text{V/V} = 0.0005$$

$$\Rightarrow A_{EA0} \cdot \beta \geq 2000 \Rightarrow A_{EA0} \geq \frac{2000}{\beta} = \frac{2000}{2/3} = 3000$$

From both line and load regulation requirements, the minimum gain required is:

$$A_{EA0} \geq 3000 \quad (\approx 69.54\,\text{dB})$$

To ensure margin, a higher DC gain of approximately 90 dB was chosen. Since bandwidth was not a primary concern for this design, the tradeoff of lower speed for higher gain was acceptable.

To meet this high gain target while minimizing power and avoiding excess poles, a triple-cascode telescopic amplifier was selected as the error amplifier. This architecture was favored over folded cascode and multi-stage alternatives due to its superior gain efficiency and simplicity in compensation.

Choosing Parameters

To achieve the required open-loop gain for the error amplifier, we use the gain expression for a triple-cascode amplifier:

$$A_{EA0} = \frac{1}{2}(g_m r_{ds})^3$$

Solving for $A_{EA0} = 31622$, we get:

$$g_m r_{ds} = \sqrt[3]{2A_{EA0}} = \sqrt[3]{63244} \approx 39.84$$

To ensure sufficient gain, this was rounded up:

$$g_m r_{ds} = 42$$

Based on this, we chose:

$$g_m = 80\,\mu\text{S}, \quad r_{ds} = 525\,\text{k}\Omega$$

Since a triple-cascode topology was used, the drain voltage swing is limited. To maintain saturation with minimum v_{ds}, we selected a small $\Delta = 0.1\,\text{V}$. With:

$$v_{ds} = 0.2\,\text{V}, \quad \Delta = 0.1\,\text{V}$$

The transconductance and bias current relationship is:

$$g_m = \frac{2I_D}{\Delta} \Rightarrow I_D = \frac{g_m \cdot \Delta}{2} = \frac{80 \times 10^{-6} \cdot 0.1}{2} = 4\,\mu\text{A}$$

For this bias current, the NMOS transistor width was chosen as:

$$W_{NMOS} = 6.03\,\mu\text{m}$$

This sizing achieves the desired transconductance while keeping the device in saturation with appropriate headroom for cascoding.

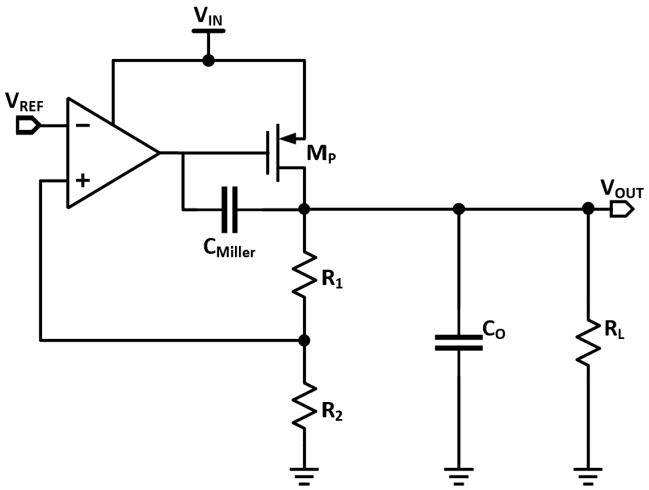

Figure 1: LDO schematic.

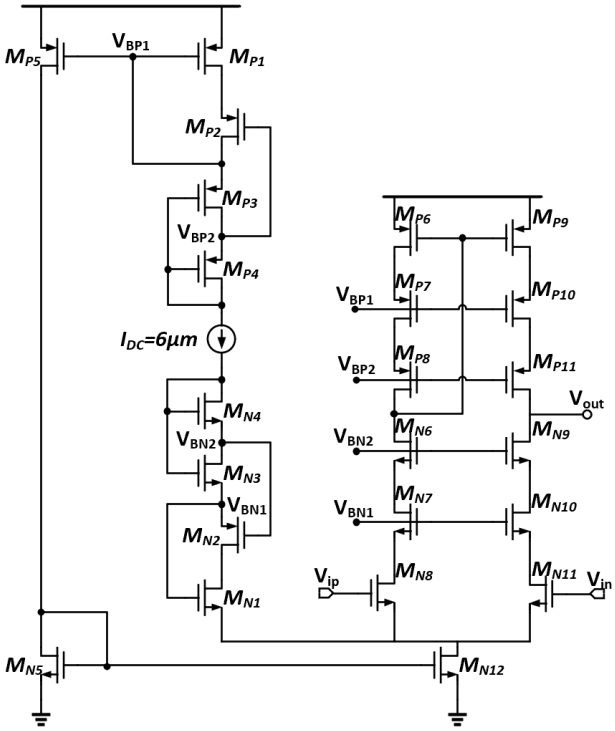

Figure 2: Error Amplifier Transistor-Level Schematic

Pass Transistor Sizing:
To properly size the PMOS pass transistor for the target load current range of 1mA to 25mA, we began by setting both V_{gs} and V_{ds} to 0.9V, and perform a sweep of the PMOS transistor width. After narrowing down the suitable width range, we performed an additional sweep over V_{gs} to ensure that the chosen device would reliably conduct the required current across expected variations in gate voltage. Following these iterations, we selected a PMOS width of 650μm as it provided sufficient drive strength across the specified voltages and currents.

Resistor Sizing
We selected a feedback ratio of $\beta = \frac{2}{3}$, where:

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$$

To satisfy this ratio, we chose:

$$R_{F1} = 10\,\text{k}\Omega, \quad R_{F2} = 20\,\text{k}\Omega$$

These values are reasonable, as they set the feedback divider current to approximately 40 μA when $V_{\text{OUT}} = 1.2\,\text{V}$, which is acceptable given the overall quiescent current budget, particularly under maximum load

conditions ($I_L = 20\,\text{mA}$).

Miller Capacitor Compensation

To ensure loop stability and achieve a phase margin (PM) close to 60°, Miller compensation was implemented. A compensation capacitor C_c was placed between the output of the error amplifier and an internal high-impedance node. This introduces a dominant pole at low frequency and pushes the non-dominant poles to higher frequencies through pole-splitting. To determine the optimal value of C_c, a parameter sweep was performed in simulation under the worst-case loading condition ($I_L = 20\,\text{mA}$)

Table 1: MOSFET Characteristics

Device	W	L	g_m	r_{ds}	I_{ds}	Δ	Region of Operation
M_{P1}	540nm	360nm	27.06μS	195.6KΩ	-6μA	-284.4mV	Linear
M_{P2}	1.62μm	360nm	56.93μS	1.548MΩ	-6μA	-172.4mV	Saturation
M_{P3}	540nm	360nm	17.78μS	49.53KΩ	-6μA	-350.4mV	Linear
M_{P4}	1.62μm	360nm	55.28μS	1.869MΩ	-6μA	-183.4mV	Saturation
M_{N1}	360nm	360nm	48.97μS	90.22KΩ	6μA	167.8mV	Linear
M_{N2}	810nm	360nm	81.89μS	907.2KΩ	6μA	120.1mV	Saturation
M_{N3}	270nm	360nm	29.69μS	31.4KΩ	6μA	219.3mV	Linear
M_{N4}	810nm	360nm	83.13μS	943.5KΩ	6μA	124.8mV	Saturation
M_{P5}	1.26μm	360nm	74.93μS	1.24MΩ	-15.3μA	-284.3mV	Saturation
M_{N5}	6.03μm	360nm	279.8μS	288.7KΩ	15.3μA	80.08mV	Saturation
M_{P6}	4.995μm	495nm	62.34μS	945.6KΩ	-4.125μA	-103.3mV	Saturation
M_{P7}	4.995μm	495nm	61.74μS	598.6KΩ	-4.125μA	-107.2mV	Saturation
M_{P8}	9μm	540nm	71.6μS	739.9KΩ	-4.125μA	-90.44mV	Saturation
M_{P9}	4.995μm	495nm	62.34μS	945.8KΩ	-4.125μA	-103.3mV	Saturation
M_{P10}	4.995μm	495nm	71.6μS	613.3KΩ	-4.125μA	-107.1mV	Saturation
M_{P11}	9μm	540nm	72.38μS	1.89MΩ	-4.125μA	-89.46mV	Saturation
M_{N6}	4.5μm	540nm	86.99μS	1.192MΩ	4.125μA	68.93mV	Saturation
M_{N7}	4.005μm	360nm	88.67μS	186KΩ	4.125μA	64.28mV	Saturation
M_{N8}	6.03μm	360nm	93.28μS	391.5KΩ	4.125μA	56.59mV	Saturation
M_{N9}	4.5μm	540nm	87.04μS	1.162MΩ	4.125μA	69.18mV	Saturation
M_{N10}	4.005μm	360nm	88.6μS	180KΩ	4.125μA	64.31mV	Saturation
M_{N11}	6.03μm	360nm	93.28μS	391.2KΩ	4.125μA	56.59mV	Saturation
M_{N12}	6.03μm	360nm	263.6μS	220.8KΩ	14.25μA	79.1mV	Saturation
M_P	650μm	180nm	-	-	-	-	-

Table 2: Performance summary

Design parameter/variable	Simulated performance	Specification
Input voltage	1.8V	$\leq$ 1.8V
Output voltage	1.2V	1.0V $-$ 1.4V
Load current	20mA	1mA $-$ 25mA
DC load regulation	$0.022\mu V/mA$	$\leq 50\mu$V/mA
DC line regulation	$15.7\mu V/V$	$\leq 500\mu$V/V
Quiescent current (I_L = 1mA/I_L = 25mA)	40μA/40μA	Minimum
PSR (@F_{in} = 1KHz/F_{in} = 1MHz)	-4.7dB/-61.8dB (I_L = 25mA)	–
Worst-case PSR	-0.33dB	–
DC loop gain (I_L = 1mA/I_L = 25mA)	114.48dB/106.22dB	–
Loop-gain unity gain frequency (I_L = 1mA/I_L = 25mA)	1.185MHz/1.00135MHz	–
Loop-gain phase margin(I_L = 1mA/I_L = 25mA)	84.47°/88.89°	–
Loop-gain gain margin (I_L = 1mA/I_L = 25mA)	38.87dB/41.79dB	–
Output noise (I_L = 1mA/I_L = 25mA)	63.27μV/59.52μV	–

Loop-gain AC response

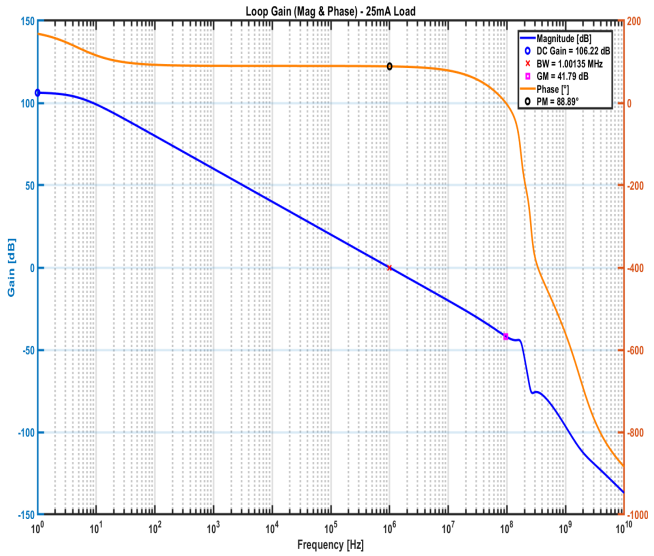

Figure 3: Loop Gain (at $I_L = 25\text{mA}$) vs Freq

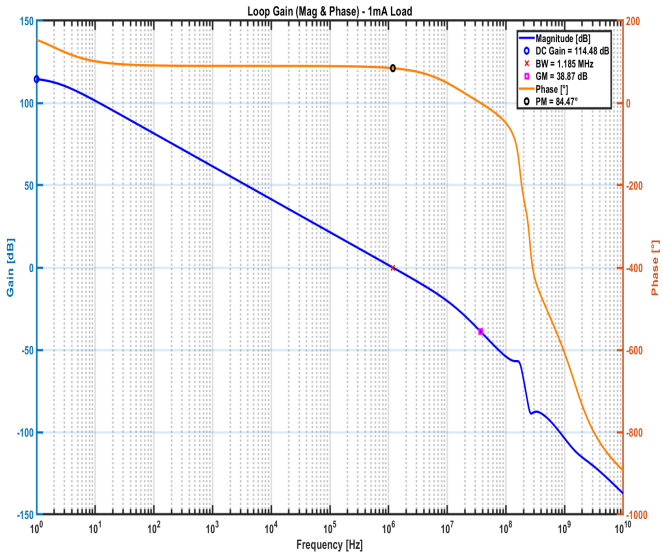

Figure 4: Loop Gain (at $I_L = 1\text{mA}$) vs Freq

DC load and line regulation response

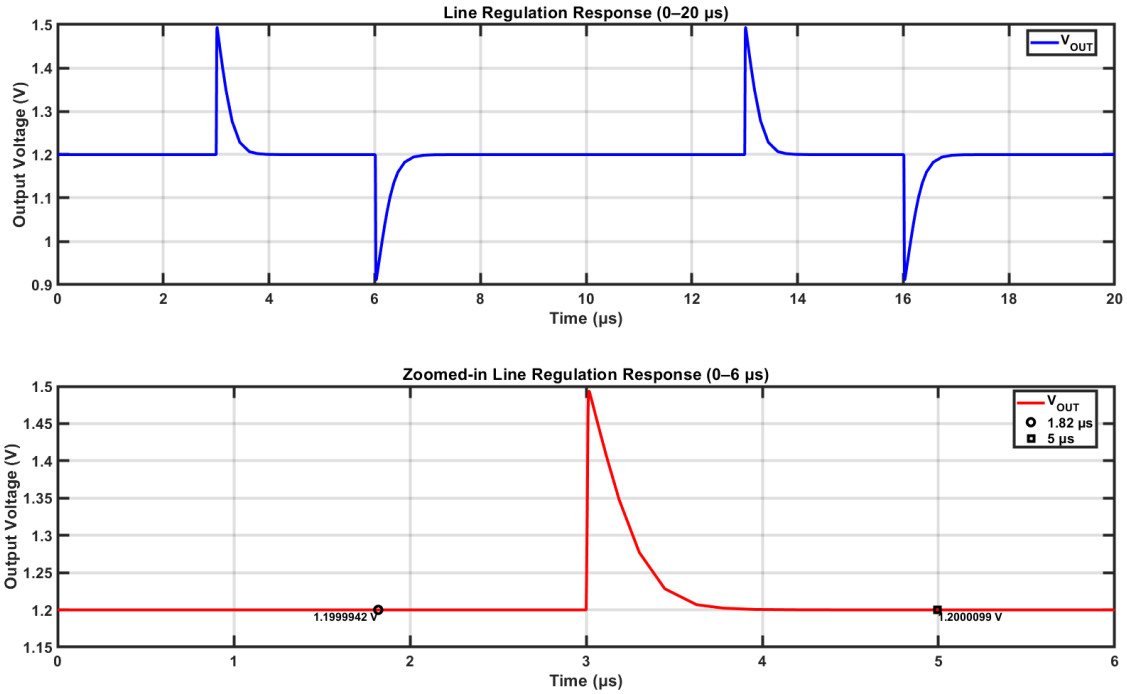

Figure 5: Line Regulation (at $I_L = 20\text{mA}$) vs Time (μ s).

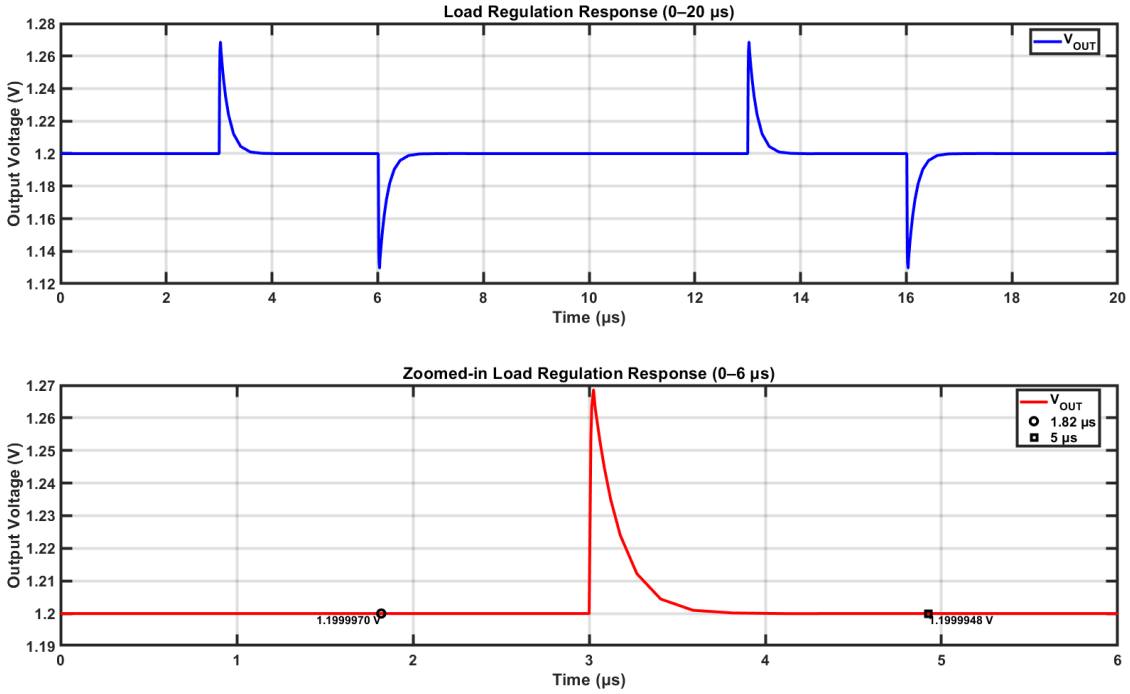

Figure 6: Load Regulation (at $I_L = 20\text{mA}$) vs Time (μ s).

Power supply rejection and Output Noise

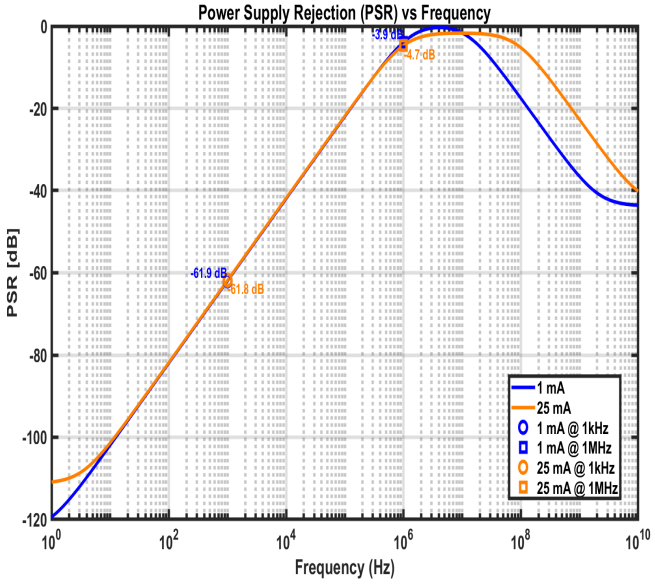

Figure 7: Power Supply Rejection (PSR) ($I_L = 1\text{mA}$ / 25mA) vs Frequency

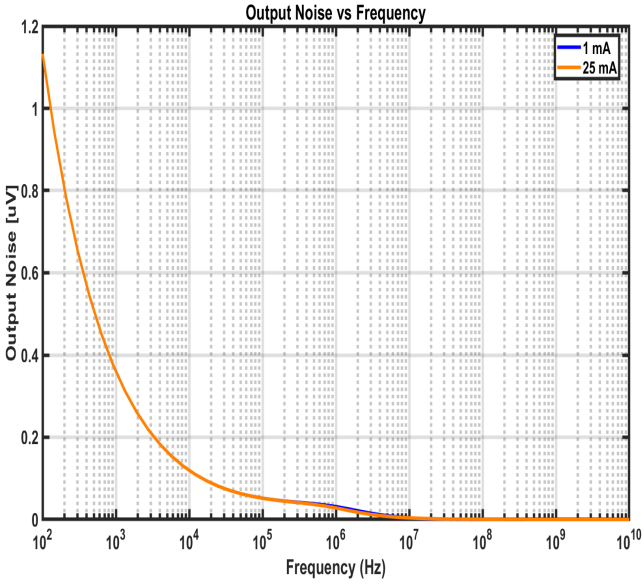

Figure 8: Output Noise ($I_L = 1\text{mA}$ / 25mA) vs Frequency