Design of the frontend for LEN5, a RISC-V Out-of-Order processor

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POLITECNICO
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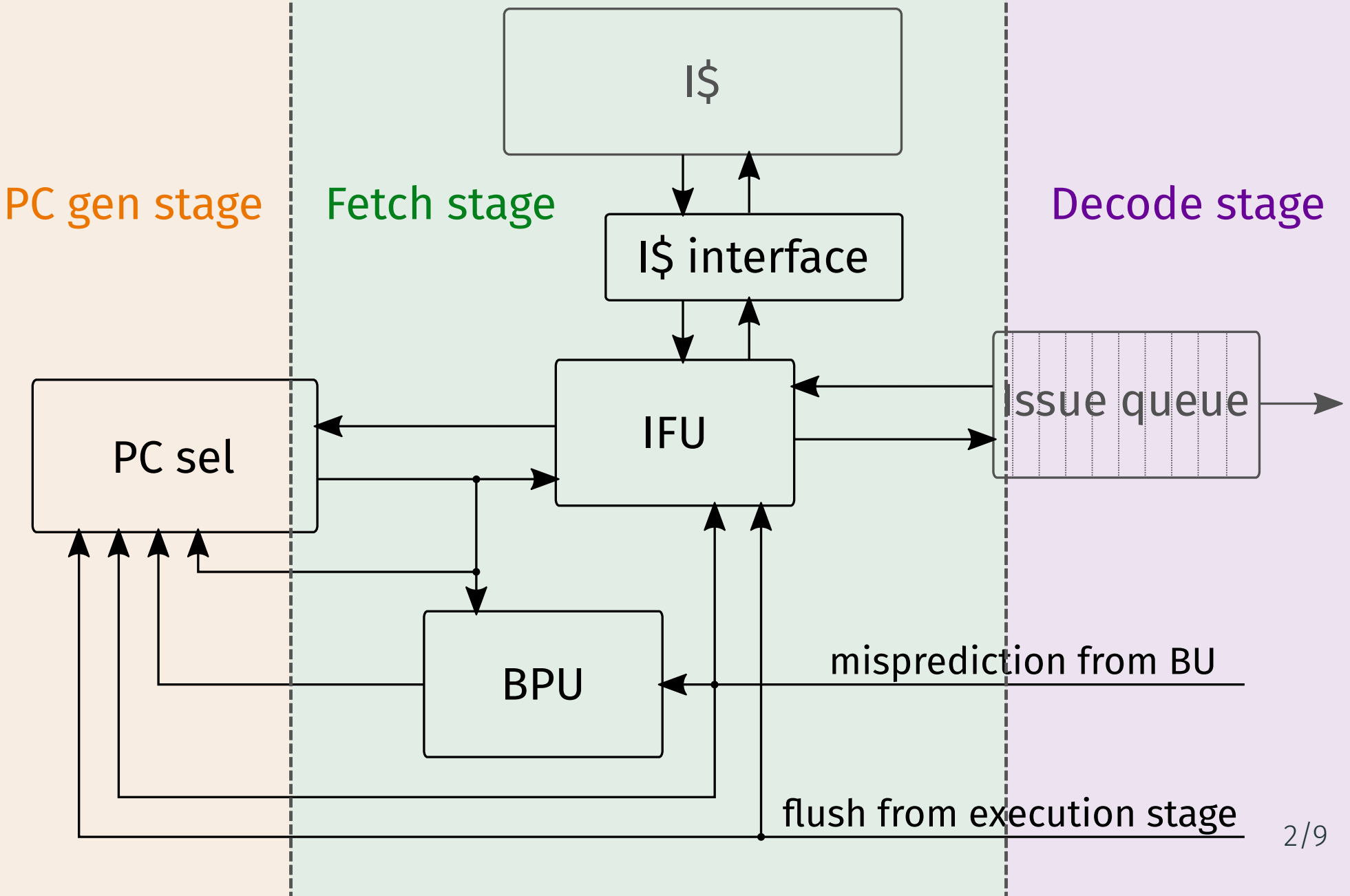
LEN5 overview

First Frame

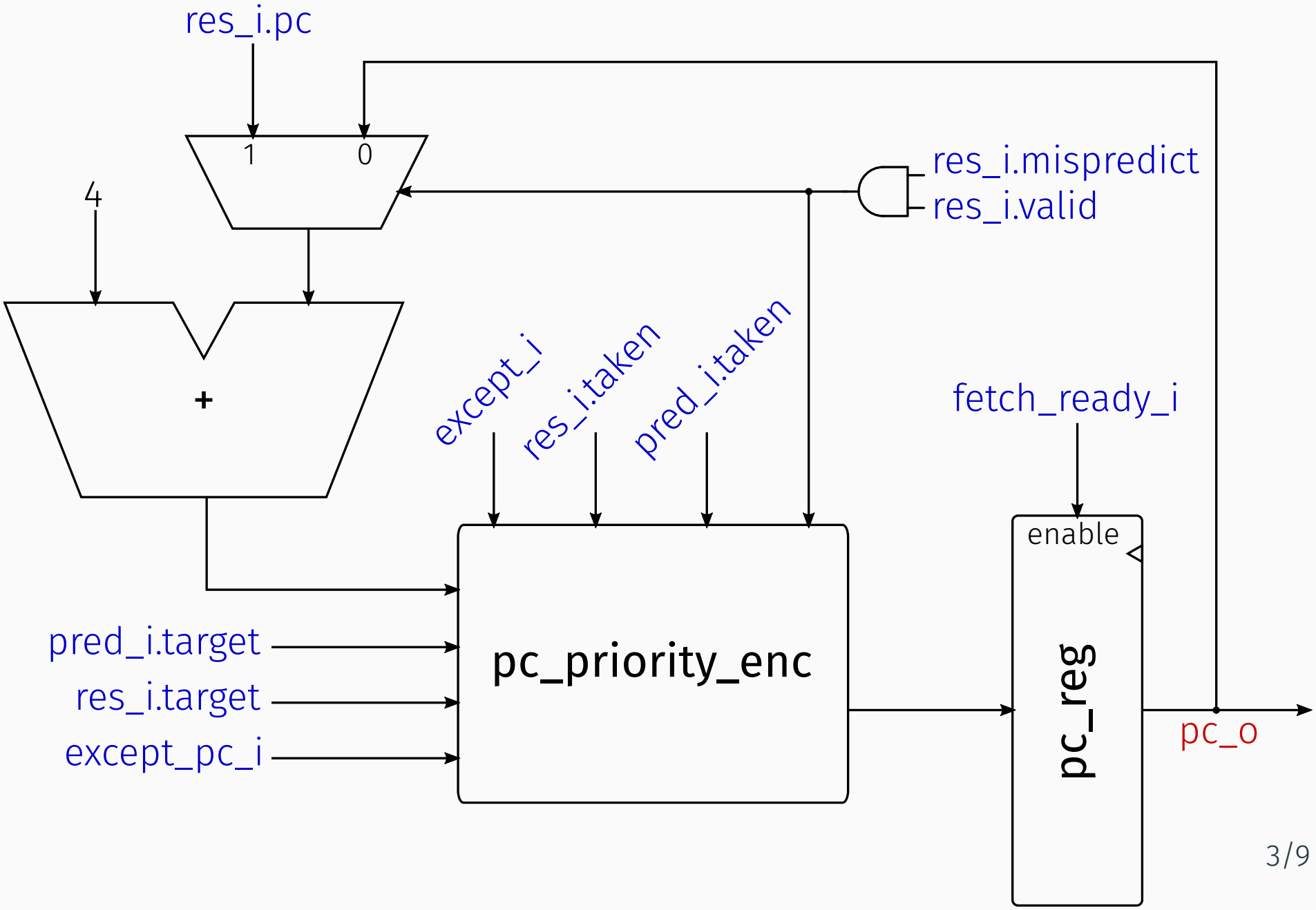
Hello, world!

Frontend design

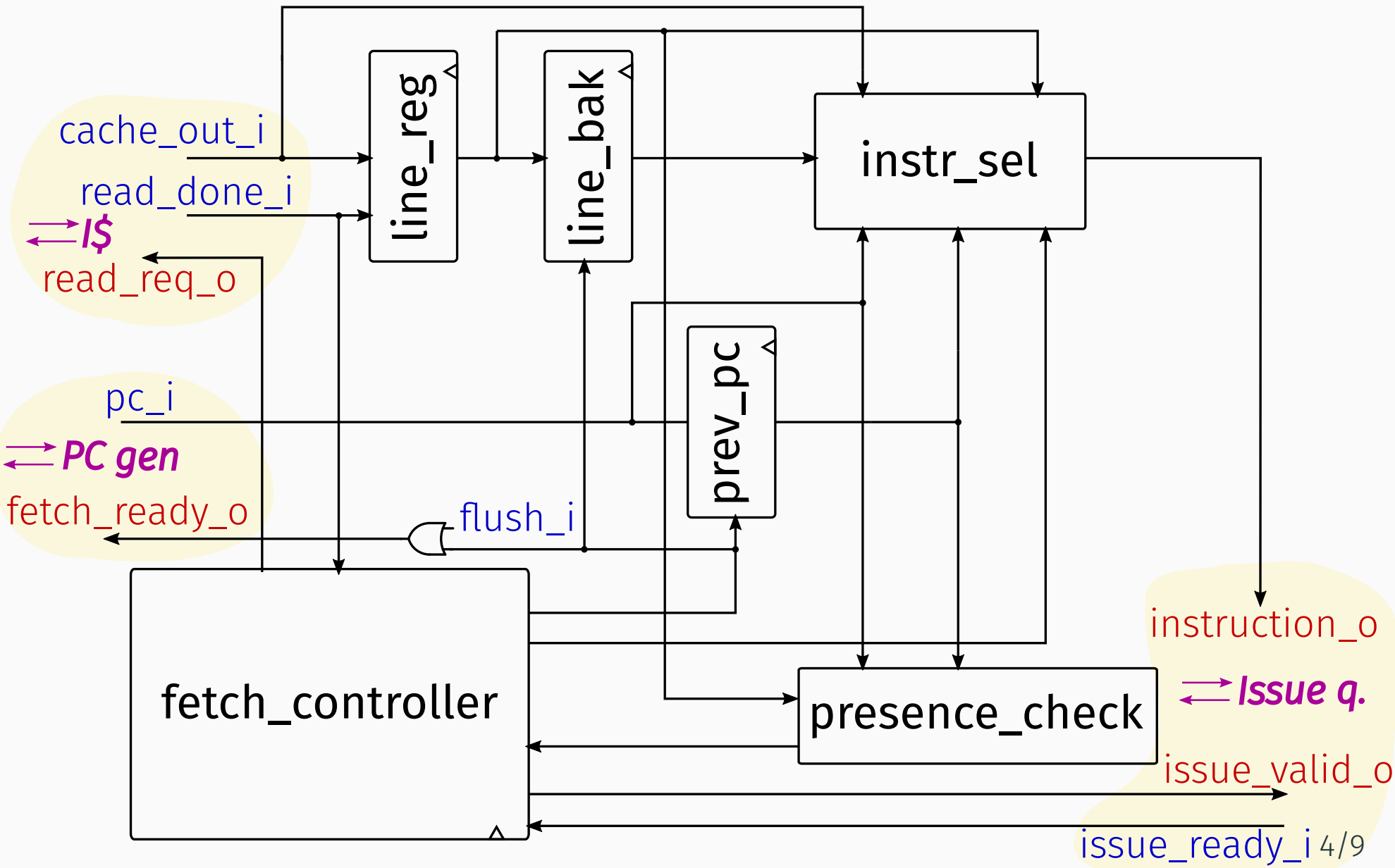
Frontend overview



PC gen stage

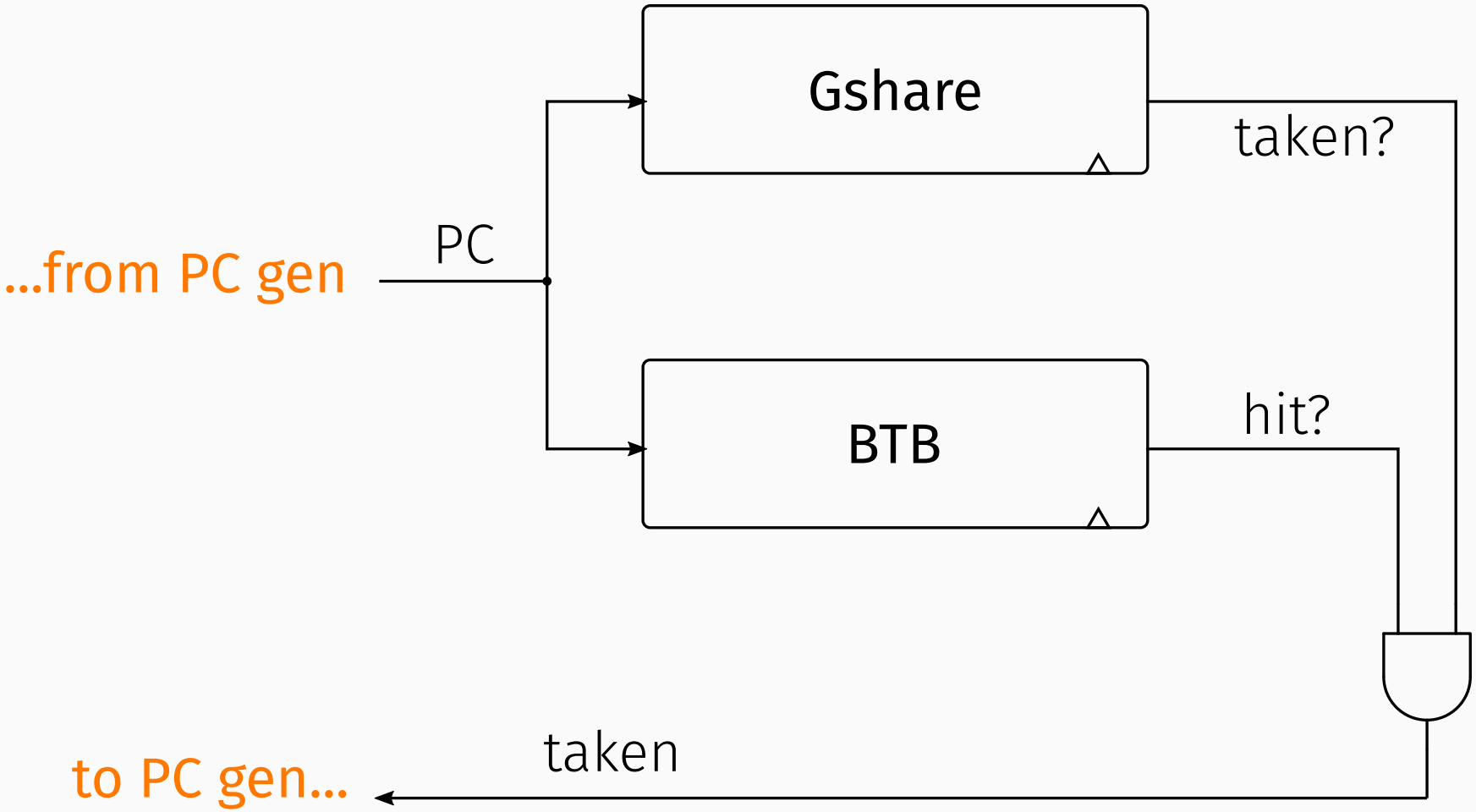

res_i.pc
1
0
4
+
res_i.mispredict
res_i.valid
except_i
res_i.taken
pred_i.taken
fetch_ready_i
enable
pred_i.target
res_i.target
except_pc_i
pc_priority_enc
pc_reg
pc_o

Instruction Fetch Unit (IFU)

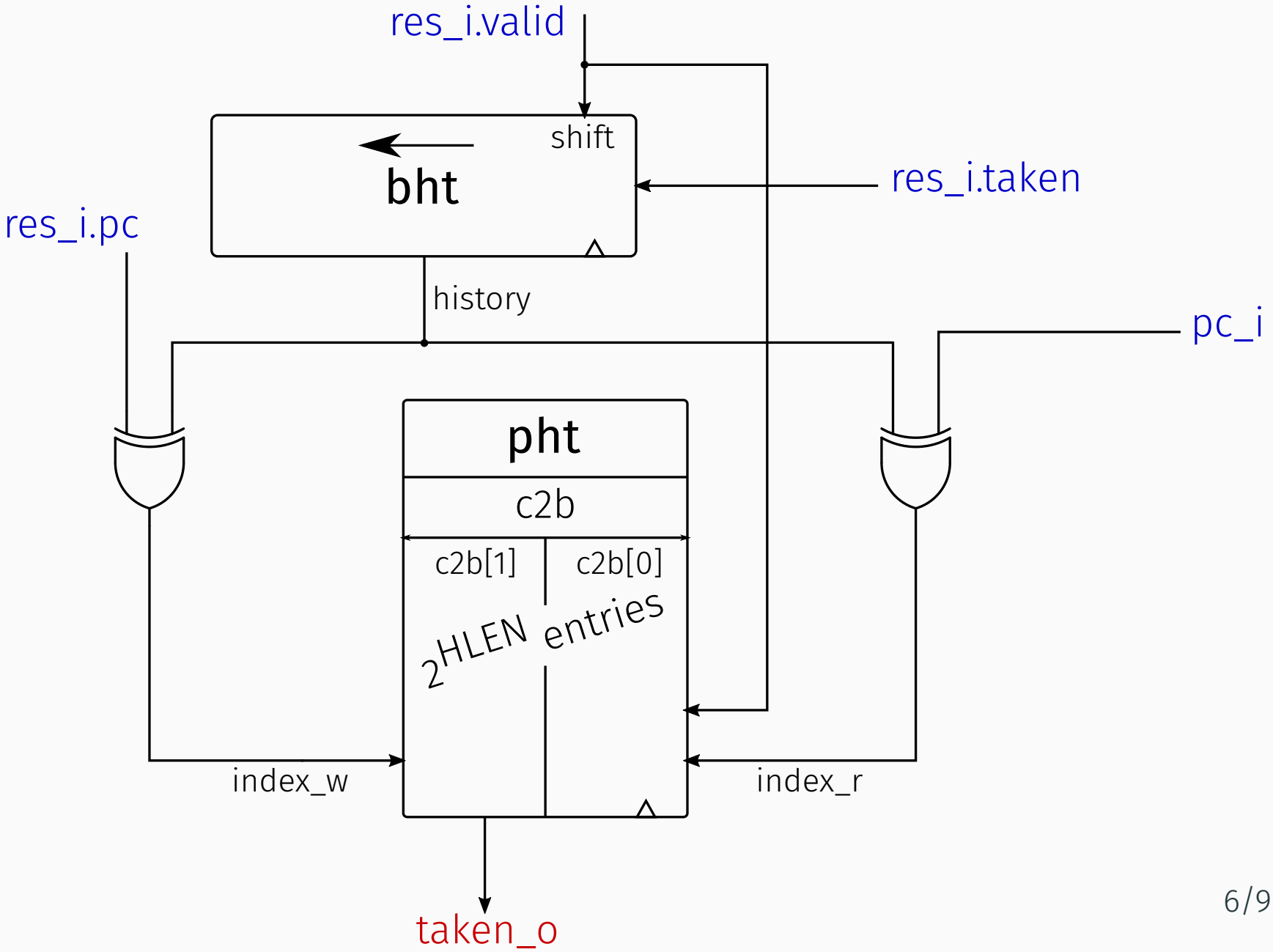


Branch management

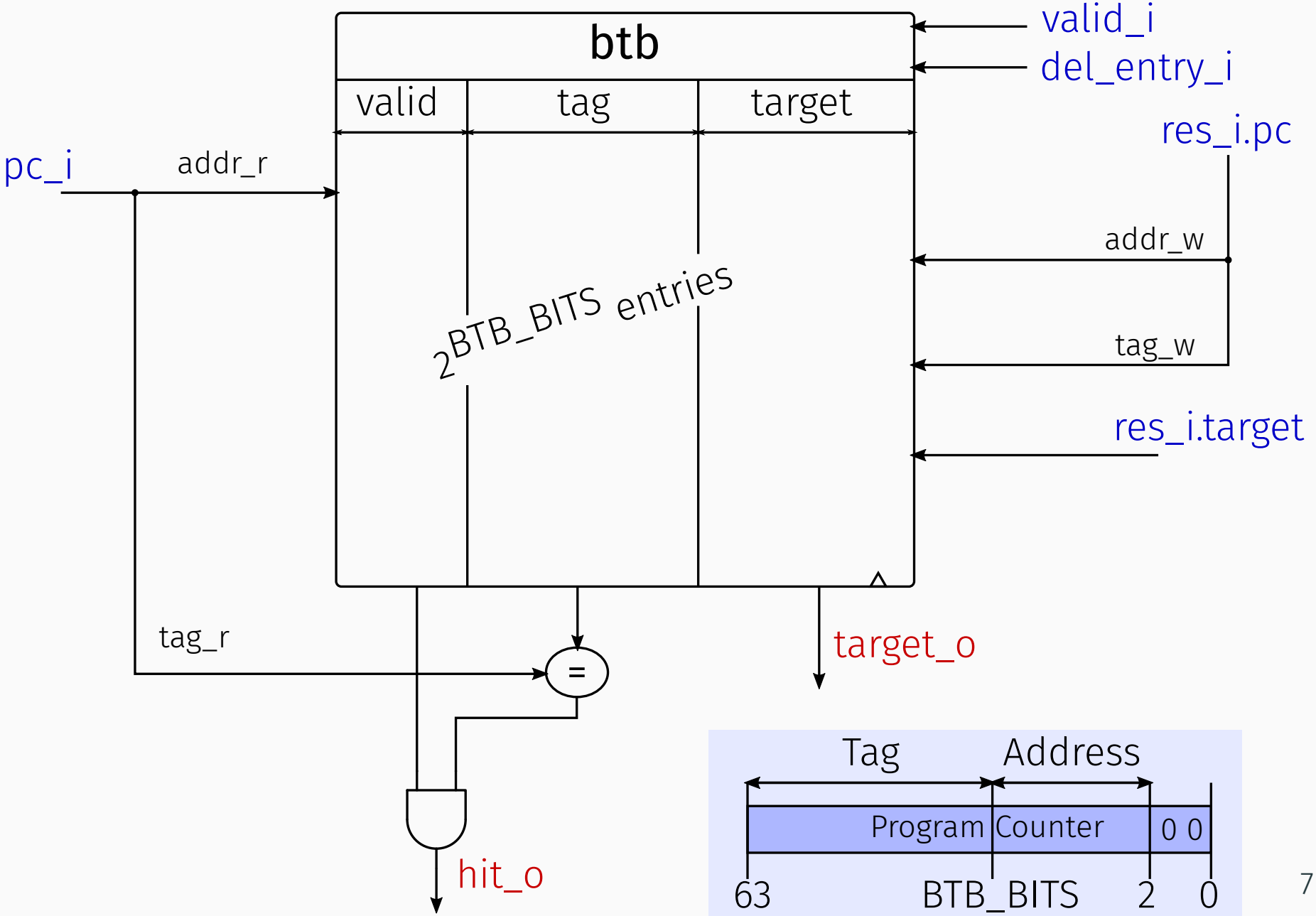
Branch Prediction Unit (BPU)



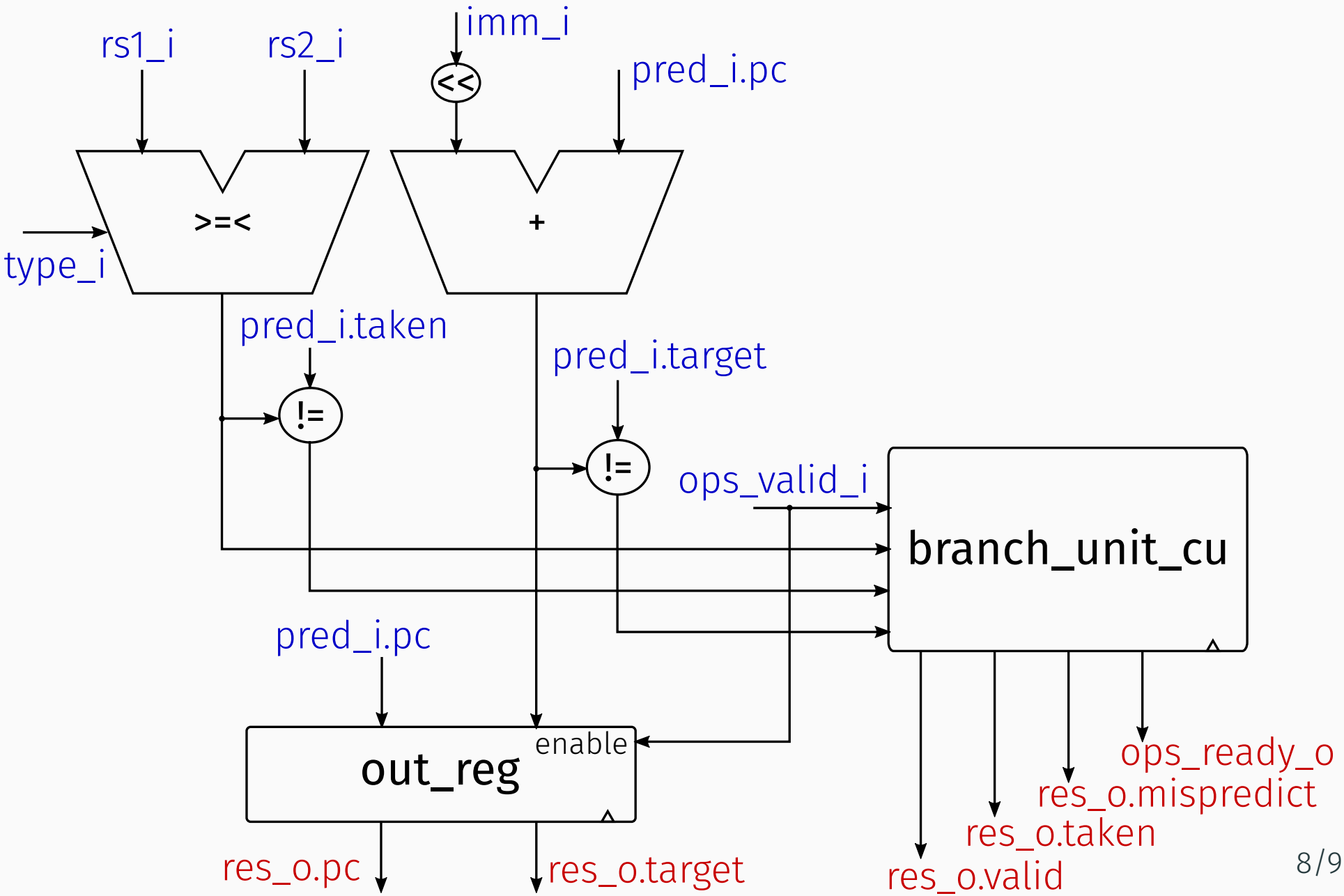
Gshare branch predictor



Branch Target Buffer (BTB)



Branch unit


rs1_i
rs2_i
imm_i
<<
pred_i.pc
>=<
+
type_i
pred_i.taken
pred_i.target
!=
!=
ops_valid_i
branch_unit_cu
pred_i.pc
enable
out_reg
ops_ready_o
res_o.mispredict
res_o.taken
res_o.valid
res_o.pc
res_o.target

BPU update actions

Prediction	Resolution	Target	Action
Taken	Taken	✔	Increment 2-bit counter
		✖	Increment 2-bit counter Update BTB entry Flush, go to right target
	Not taken	–	Decrement 2-bit counter Remove BTB entry Flush, go to branch PC+4
Not taken	Not taken	–	Decrement 2-bit counter
	Taken	–	Increment 2-bit counter Add BTB entry Flush, go to right target

Results