Digital Microelectronics 2018
Final project report

Group 5

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1 Introduction

The goal of this final project is to design and characterize two logic gates of a standard cell library. These are in particular an inverter whose transistors have width four times the minimum (`INV_X4` in the following), and a half adder (`HA_X1` in the following).

The design starts with the schematic drawing, using an available `.png` image as a reference, which has to be simulated as an initial condition. Then, the layout of the cell must be drawn and the parasitic elements must be extracted from it. Finally, those parasitics must be used for the final characterization in order to fill in the Liberty file of the standard cell library.

2 Inverter

2.1 Schematic

2.2 Layout

2.3 Characterization

3 Half adder

3.1 Schematic

3.2 Layout

Given that the layout of the half adder is quite more complex than the one of the inverter, we started by deeply analyzing the possible approaches using the pen-and-paper method. The final solution that we found consisted in sharing source/drain diffusions as much as possible, in order to minimize the area in the horizontal direction.

When actually drawing the design in Virtuoso, we made sure of running the Design Rule Checker very often, in order to avoid problems in advance.

3.3 Characterization