

**Digital Microelectronics**

POLITECNICO DI TORINO

DIPARTIMENTO DI ELETTRONICA E TELECOMUNICAZIONI

**Final Project:**  
**Standard Cell layout of an inverter and a  
half-adder**

*Group 5:*

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Date: June 12, 2018

## 1 Introduction

The goal of this final project is to design and characterize two logic gates of a standard cell library. These are in particular an inverter whose transistors have width four times the minimum (INV\_X4 in the following), and a half adder (HA\_X1 in the following).

The design starts with the schematic drawing, using an available .png image as a reference, which has to be simulated as an initial condition. Then, the layout of the cell must be drawn and the parasitic elements must be extracted from it. Finally, those parasitics must be used for the final characterization in order to fill in the Liberty file of the standard cell library.

## 2 Inverter

### 2.1 Schematic

Starting from the schematic of the available .png (figure 1), we copied it using Virtuoso Schematic Editor, obtaining the result shown in figure 2. Note that the four PMOS and NMOS transistors in parallel will be just one large transistor in the layout.

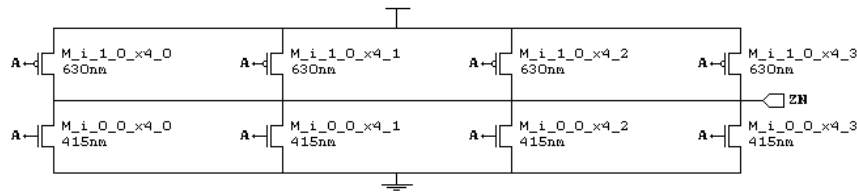


Figure 1: Reference schematic of the inverter

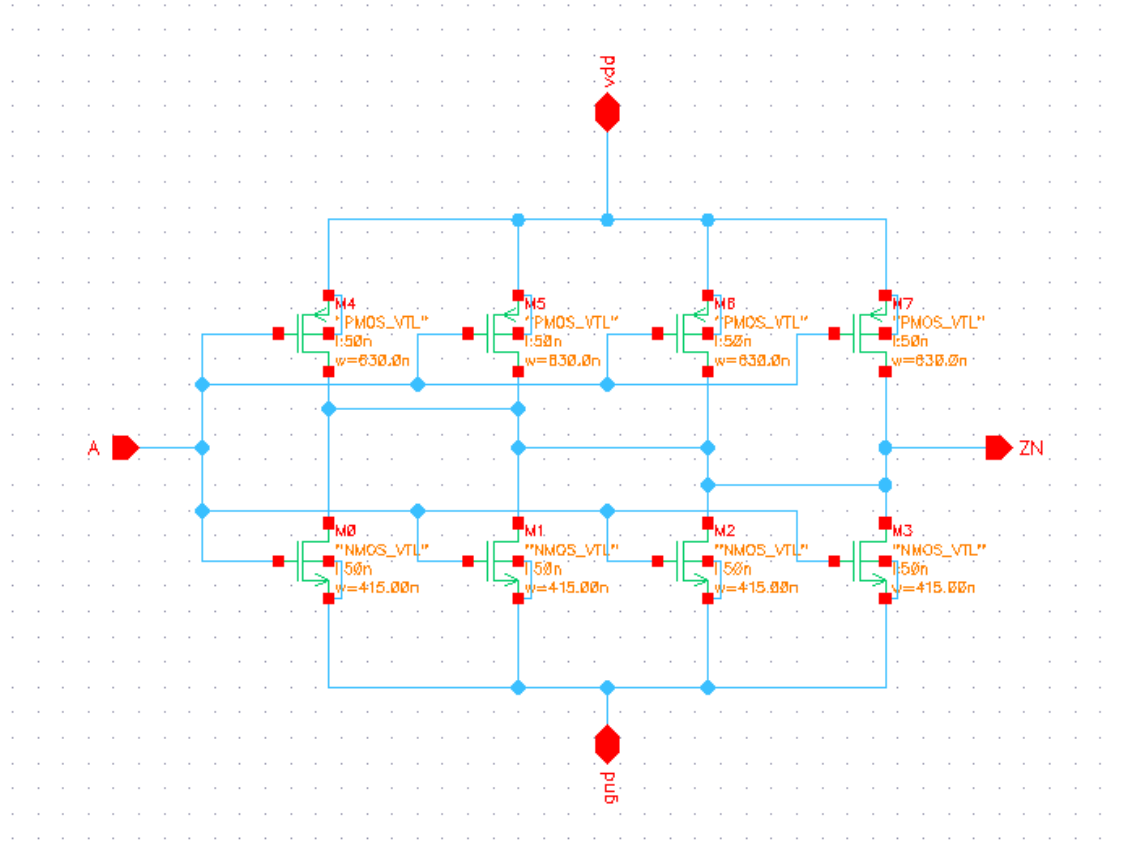


Figure 2: Final schematic of INV\_X4

We then carried out some preliminary simulations using a test bench, to confirm that the circuit works correctly. We measured rise and fall times, as well as propagation delays, that will be compared with the actual characterization later on. We also measured the transfer characteristic, shown in figure 3.

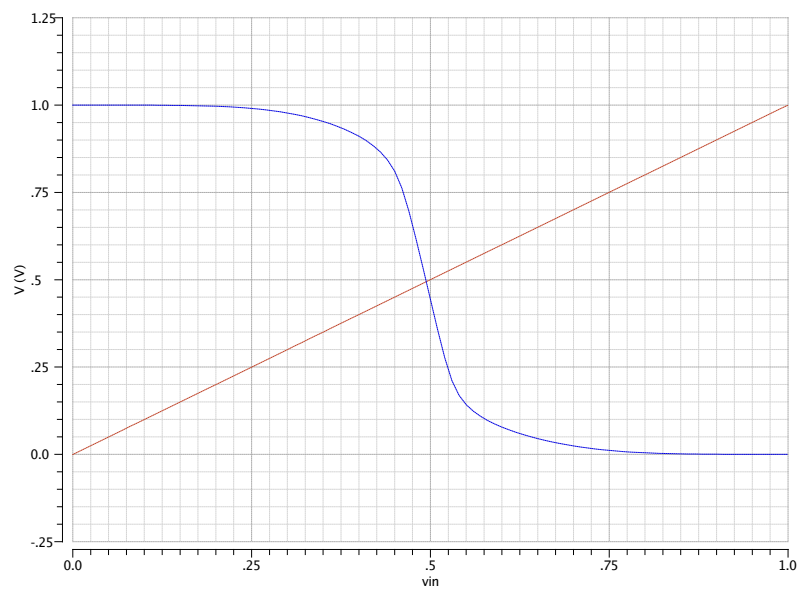


Figure 3: Inverter transfer characteristic

## 2.2 Layout

## 2.3 Characterization

# 3 Half adder

## 3.1 Schematic

The schematic was drawn using Virtuoso schematic editor.

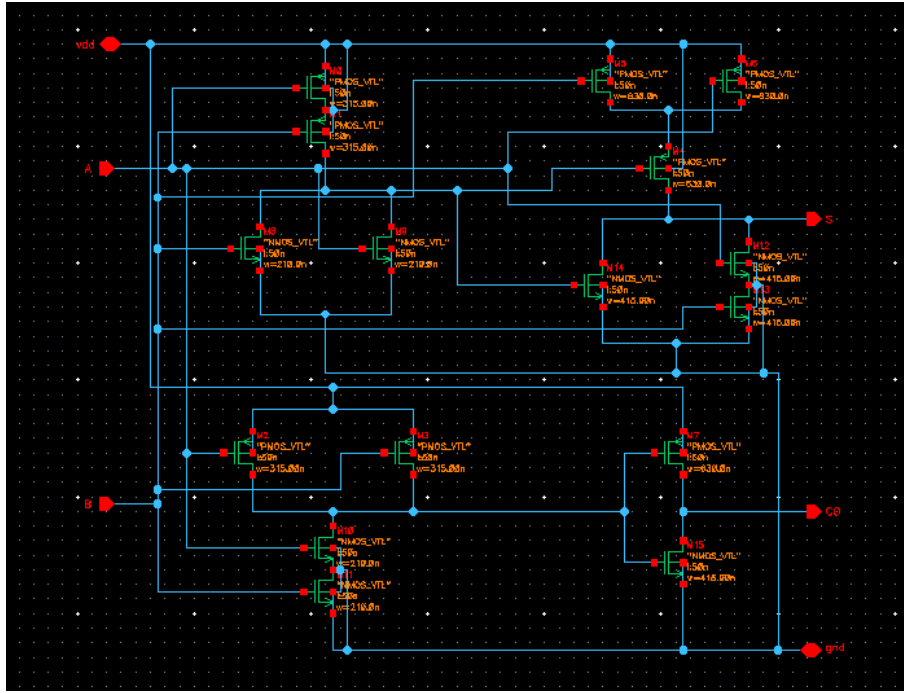


Figure 4: HAX1 schematic

## 3.2 Layout

Given that the layout of the half adder is quite more complex than the one of the inverter, we started by deeply analyzing the possible approaches using the pen-and-paper method. The final solution that we found consisted in sharing source/drain diffusions as much as possible, in order to minimize the area in the horizontal direction.

When actually drawing the design in Virtuoso, we made sure of running the Design Rule Checker very often, in order to avoid problems in advance.

Layout design started looking at the schematic. First of all we tried to put the two outputs on the opposite sides of the cell, because this way, if the input are brought over it in the middle with the `metal 2` and linked with vias, the input-output paths are more probably balanced in length. Thus we started drawing on a paper the first nMOS of the inverter whose output was CO. With a view to share the sources/drains as much as possible we began putting all the transistors one near the other drawing only the strictly necessary metal. We used different colours to have an easier readability and go on drawing only the `metal` for the sources/drains and the `polysilicon` for the gates until the end of the port and left the routing last. Then we completed the layout linking together the various elements coherently with the schematic view.

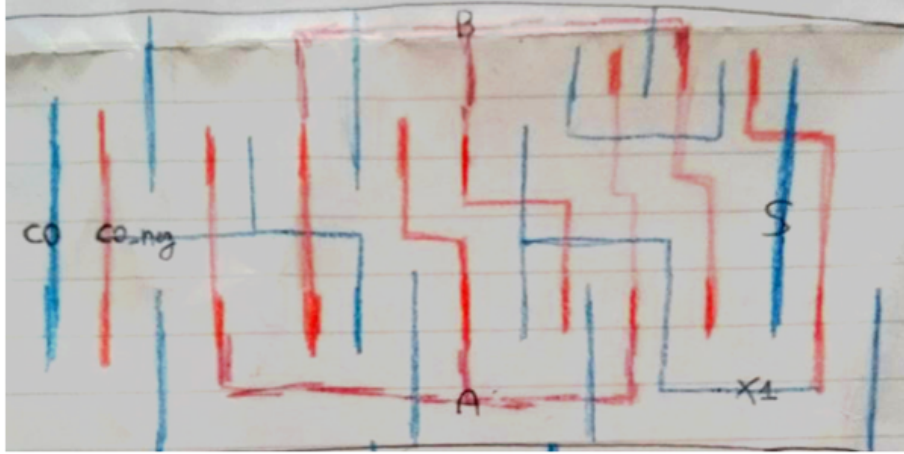


Figure 5: First sketch of the layout. Blue: metal1, red: polysilicon. Labels are not related with the position of the corresponding via.

Then we converted this sketch in a real layout design using the Virtuoso embedded layout editor. During our sessions we paid attention to reduce every distance to the minimum with the aid of the meter tool and in accordance with the Design Rules. We made a lot of effort to have a cell with the minimum area because the area is directly linked to the yield of the process and to logic ports density, capacitance and therefore delay and power cost per commutation. The less is the area, the more ports can stay in a chip or the more the chip will be small, and it is harder to find defects on a single chip if it is small, because the density of the defects per unit area is about constant (higher yield for the process). The delay and the power costs rise with the area because if more material is used, more resistance/capacitance is added. For this reason we also tried to reduce the length of every wire.

The height of the cell is fixed because this is a standard cell. The top and the ground of it are made of metal which has to feed the transistors. Many entity like this one can be put one next to the other to form a line of cells packed together and fed with global Val-GND voltages. This way it is simpler to reach every port with its supply.

When we drew the layout with the editor we changed a little bit the connections. Instead of putting a single wire of polysilicon to connect each gate with the related input A/B, we used vias and metal1. It would have been interesting to compare the performances of two implementations.

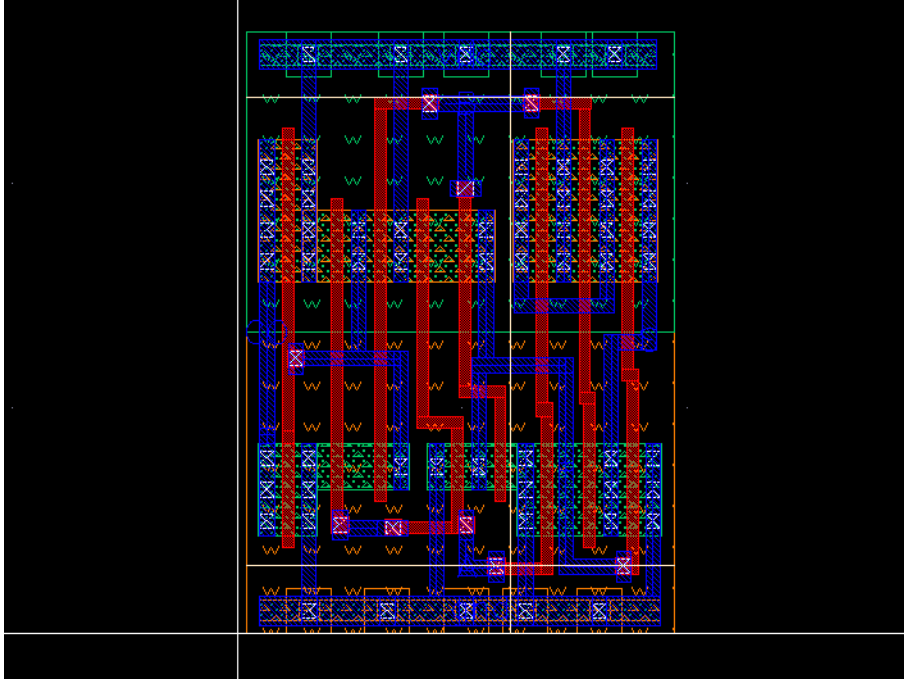


Figure 6: HAX1 layout, more metal1 and vias on pull-down connections

In the pull up network the advantage of putting `metal1` seems to be huge, whereas in the pull down network it's not so clear. We present here another possible implementation. For time reasons we have characterized only the first one, though.

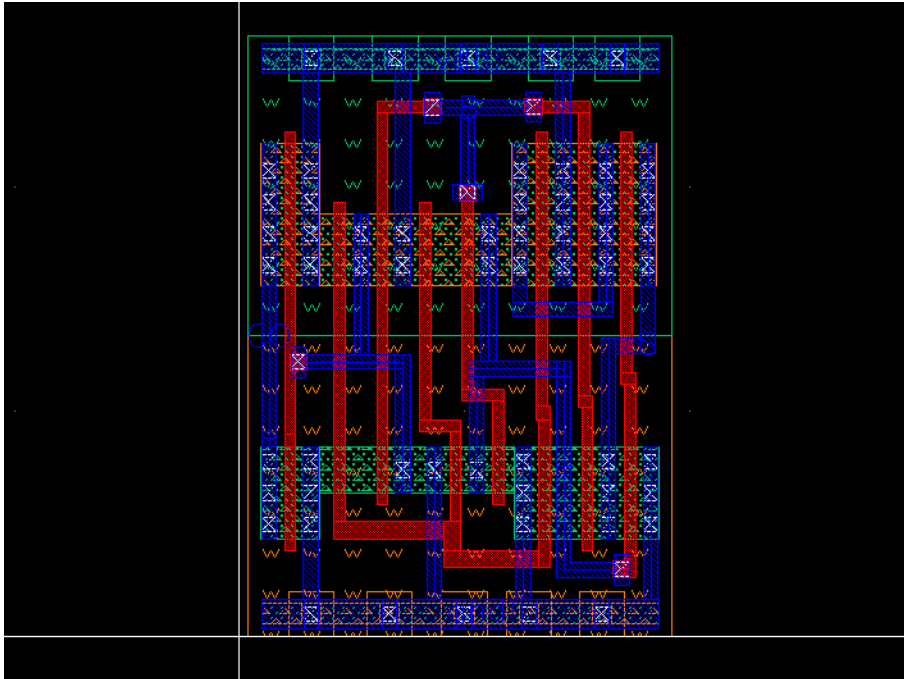


Figure 7: HAX1 layout, more polysilicon on pull-down connections

### 3.3 Characterization