Digital Microelectronics

Politecnico di Torino

Dipartimento di Elettronica e Telecomunicazioni

Final Project: Standard Cell layout of an inverter and a half-adder

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1 Introduction

The goal of this final project is to design and characterize two logic gates of a standard cell library. These are in particular an inverter whose transistors have width four times the minimum (`INV_X4` in the following), and a half adder (`HA_X1` in the following).

The design starts with the schematic drawing, using an available `.png` image as a reference, which has to be simulated as an initial condition. Then, the layout of the cell must be drawn and the parasitic elements must be extracted from it. Finally, those parasitics must be used for the final characterization in order to fill in the Liberty file of the standard cell library.

2 Inverter

2.1 Schematic

Starting from the schematic of the available `.png` (figure 1), we copied it using Virtuoso Schematic Editor, obtaining the result shown in figure 2. Note that the four PMOS and NMOS transistors in parallel will be just one large transistor in the layout.

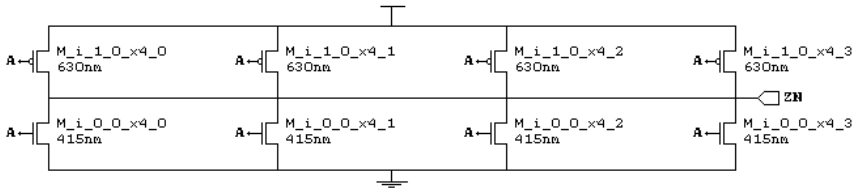

Figure 1: Reference schematic of the inverter

We then carried out some preliminary simulations using a test bench, to confirm that the circuit works correctly. We measured rise and fall times, as well as propagation delays, that will be compared with the actual characterization later on. We also measured the transfer characteristic, shown in figure 3.

2.2 Layout

2.3 Characterization

3 Half adder

3.1 Schematic

The schematic was drawn using Virtuoso schematic editor.

3.2 Layout

Given that the layout of the half adder is quite more complex than the one of the inverter, we started by deeply analyzing the possible approaches using the pen-and-paper method. The final solution that we found consisted in sharing source/drain diffusions as much as possible, in order to minimize the area in the horizontal direction.

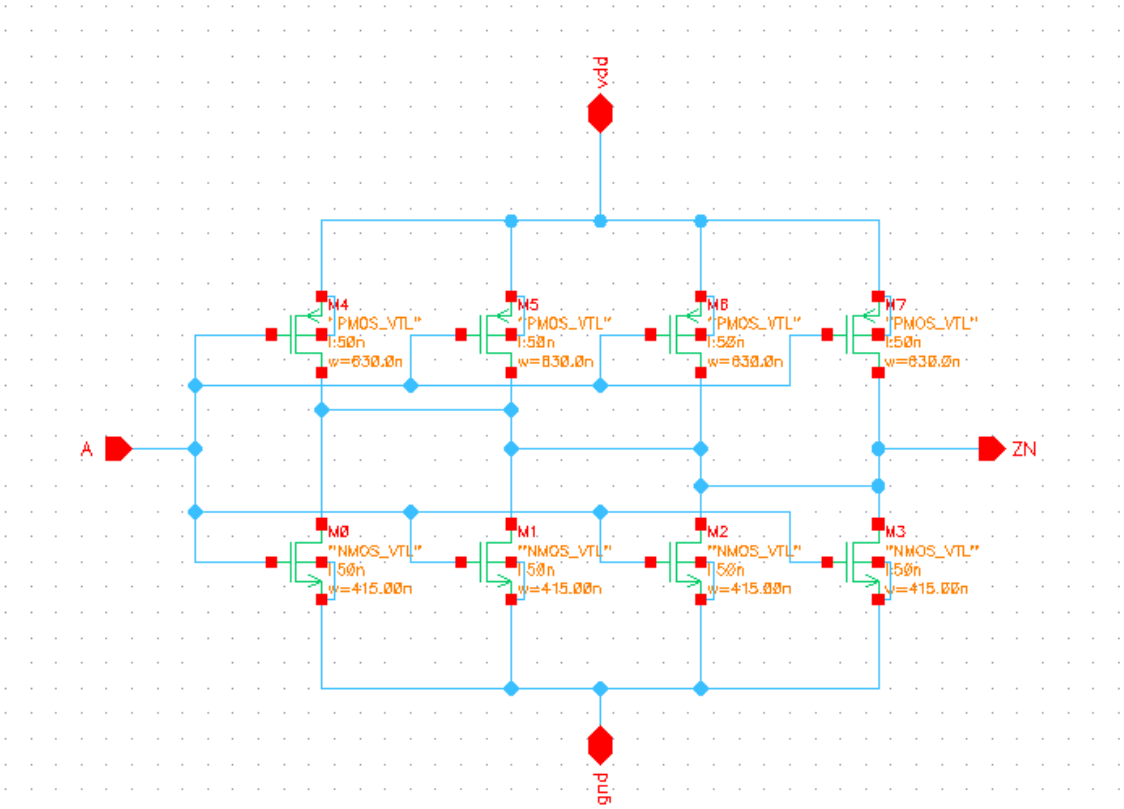

Figure 2: Final schematic of `INV_X4`

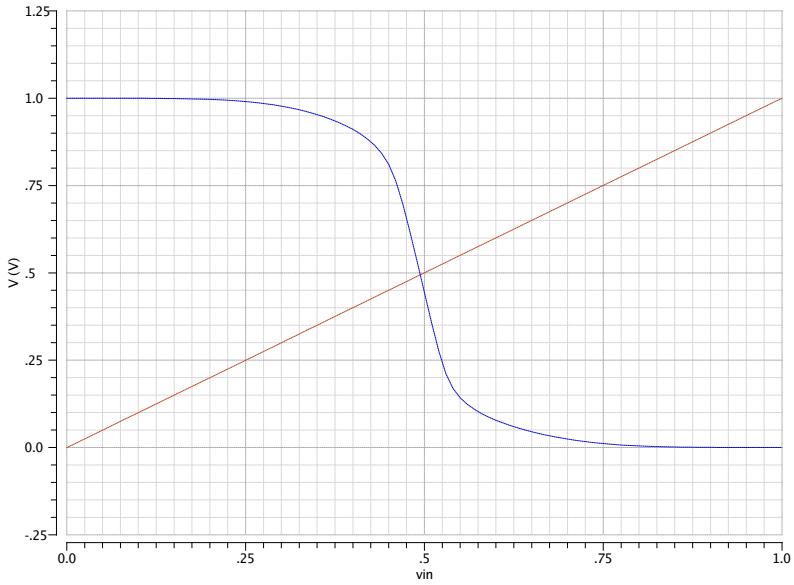

Figure 3: Inverter transfer characteristic

When actually drawing the design in Virtuoso, we made sure of running the Design Rule Checker very often, in order to avoid problems in advance.

The design started with the schematic. We tried to put the two outputs on the opposite sides of the cell, because this way the paths input-output are long $\frac{w}{2}$ at maximum, if the inputs are linked Il design stato inizialmente fatto carta e penna, guardando lo schematico disegnato. Si partiti dall'imporre che i due output fossero ai lati estremi della cella, per fare in modo che i percorsi input-output fossero al massimo circa met della dimensione orizzontale della cella. Tutto questo perch l'intenzione iniziale era quella di mettere i vias per gli input circa a met cella.

Si quindi partiti dall'uscita CO per iniziare a disegnare il layout. Abbiamo disegnato il primo nMos dell'inverter e, nell'ottica di condividere il pi possibile i sources, abbiamo piazzato il secondo

3.3 Characterization