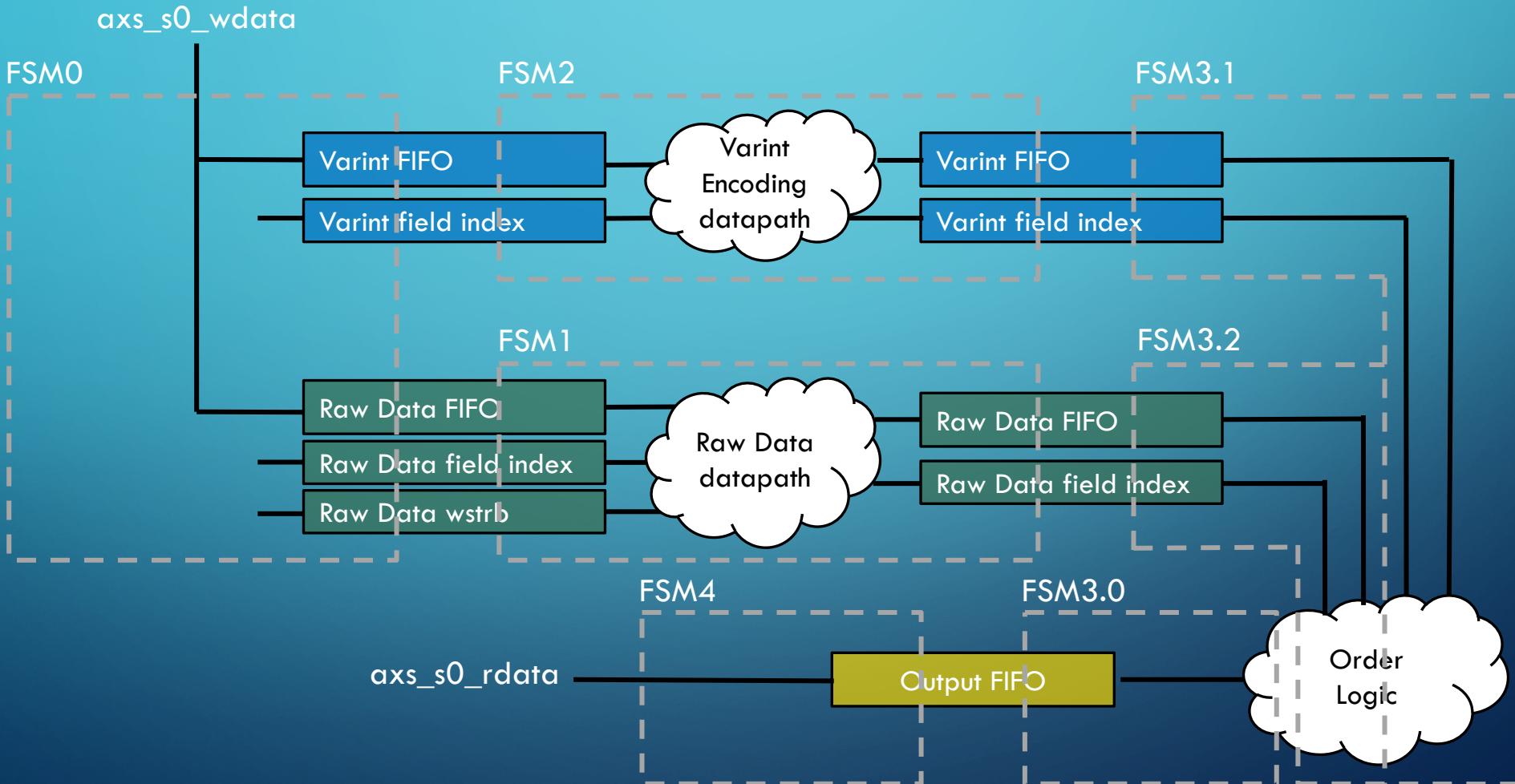


Protobuf Processing Unit (PPU): architecture, datapaths



Protobuf Processing Unit (PPU): controller design

- FSM0 Implements AXI4 slave write transactions (AW, W, B channels)
- FSM1 Processes incoming raw data (uses wstrb signal to validate bytes)
- FSM2 Varint encoding datapath (supports 32-bit and 64-bit integers)
- FSM3.1 Fetch varint data for input to ordering logic
- FSM3.2 Fetch raw data for input to ordering logic
- FSM3.0 Push data to output FIFO preserving write transaction order
- FSM4 Implements AXI4 slave read transactions (AR, R channels)