DESIGN CONSIDERATIONS FOR
CHARACTERIZATION OF CAPACITORS

by

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SCHOOL OF GRADUATE STUDIES

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_____
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Master of Science
candidate for the _____ degree*.

*We also certify that written approval has been obtained for any proprietary material contained herein.

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Dedication

Dedication text

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Abstract

0.1 Previous Abstract

This paper presents an analysis of capacitor performance at up to 600VDC bias. The analysis is accomplished through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. All tests are recorded by means of multiple ADCs and computer analysis.

0.2 Current Abstract

This paper presents an analysis of capacitor performance degredation at up to a 600VDC bias. It proposes a testing method through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. Circuit analysis and itinial prototypes will be discussed.

1 Background

The following is a list of the questions that I will be answering in my background section.

1. Where are capacitors used with a high DC bias?

    (a) What characteristics are the most important there?

    (b) What are the main failure modes?

    (c) What are the current specifications of the parts in use now?

    (d) What research is being done to develope better capacitors for this use case?

    (e) How do they currently evaluate the capacitors?

    (f) How would they benefit from my research?

2. What is the state of the art in capacitance measurement?

    (a) Impedance analyzers

    (b) Capacitance bridges

    (c) Hi pot testers

    (d) What are the good and bad points of each of these technologies?

    (e) Why do they not solve the problem that I stated?

    (f) Why does this technology not currently exist?

3. What work has been done similar to this in the past?

4. What are the important characteristics of capacitors?

5. Is there any evidence that a capacitor's properties will change over DC bias?

2 History of Capacitors

This section will chronolog the history of capacitors. It will link various introductions in the technology to advances in industry, and it will map the driving forces behind capacitor development.

Types of capacitors:

1. Leyden jars

2. ceramic

3. aluminum electrolytic

4. tantalum

5. polymer

6. metalized film

7. foil film

8. titanium

Driving forces for development:

1. scientific study

2. military

3. radio industry

4. consumer electronics

Significant players:

1. ...

2.1 Comments

*You talk about the different types of MLCCs but are not very clear as to how the differences are achieved. *The only company you mention is Sprague but Cornell Dublier is also a big and I would need to think about others such as Aerovox. I am sure there are others. *You said very little about electrolytics in your discussion and the latest are low-voltage supercapacitors.

2.2 History

Capacitors have their origin in the invention of the Leyden jar by Peter van Musschenbroek of Leiden University in 1745. [13] It allowed for the storage of electrical energy for the first time in known history.

The Leyden jar was typically made from a glass jar with metal sheets spread on the inside and outside. Electricity could be stored by charging the jar with an electrostatic device and the removing the jar. This breakthrough in the study of electricity was exremely important to scientists, as it allowed electricity to be stored and then used later. [10]

The most common design for the Leyden jar was to use a glass jar with metal foil lining the inside and out. Then inner surface was typically charged via an electrostatic generator, while the outer surface was connected to ground. The charge would stay on the metal foil until a short or small resistance was connected between them. Charge could be stored this way, allowing scientists and showmen, to use greater amounts of charge than they could generate at any one moment.

Since the Leyden jar, many different types of capacitors have risen and fallen in prominence in the market. This section will cover the historical introduction of some of the major types.

Paper capacitors use waxed paper as a dielectric. They are primarily used in high

voltage applications. But they are not preferred for much due to their high leakage and tolerances.[14] In 1876 Fitzgerald introduced wax impregnated paper dielectric capacitors with foil electrodes.[3, ch. 11] [14] They were typically used for power supply filtering in radios. In the early 1920s, they existed as tubes encapsulated in plain, bakalized cardboard, with bitman sealing the ends.[3, ch 3]

Impregnated paper capacitors used paper that was soaked in mineral oil. It was interleaved with metal foil and then rolled to make the capacitor.[23, ch. 8.2.1.1] During WW2, paper capacitors were upgraded with metal-cased tubes with a rubber end.[23, ch. 8.1] Metalized paper capacitors were created as a replacement for impregnated paper capacitors. They were constructed similarly with the improvement that one side of the paper dielectric was sprayed with metal.[6]

Karol Pollak discovered the principle of the electrolytic capacitor in 1886 while he was researching the anodization of metals. In 1897, he received a patent for the borax-solution aluminum electrolytic capacitor. In 1926, Julius Lilienfeld patented an electrolytic capacitor containing electrolyte soaked paper. Ralph D. Mershon developed the first practical, commercially available radio electrolytic capacitor. After the start of WW2, increased funding and effort was applied to the cause of electrolytic capacitors and technics such as "etching and pre-anodizing" greatly increased their reliability. [31]

In 1897, Charles Pollak received a patent for the borax electrolyte aluminum electrolytic capacitor. In 1936 Cornell-Dubilier opened a factory to produce aluminum electrolytic capacitors. These capacitors became more reliable after WW2, when the industry applied additional resources to develope the technology.[8]

M. Bauer of Germany invented the mica capacitor in 1874. The original mica capacitor was a "clamped" style capacitor, which was used through the 1920s.[32] Clamped style mica capacitors were eventually replaced by silver mica capacitors, which greatly increased mica capacitors' characteristics.[14].

Mica's inherent inertness and reliability allowed for extreme reliability and efficiency in a packaged capacitor.[29] The mica capacitor was heavily used in the radio industry due to its superb stability at RF frequencies and physical robustness.[22]

During WWI, mica capacitors began to be produced in large quantities. This was mainly due to it being able to survive shock from weapons better than its glass counterpart. Also, it allowed the capacitors to be shrunk to achieve the same purpose. [3, f. 37-41]

In light of mica supply chain problems and the emergence of ceramic capacitors during WW2, mica capacitors fell from prominence to a niche market.[1, Ch 3, Sec II]

The first glass dielectric capacitor was, in fact, the Leyden jar. While this early capacitor was used mainly for scientific experiments, commercial glass capacitors came later.

Glass tubular capacitors appeared in 1904 and were used in Marconi's experiments in wireless transmission. They were know as Moscicki tubes. They continued to be used in wireless communication until about WWI. [3, p. 102]

Scientists in Germany created the first steatite ceramic capacitor in 1920. [1, Ch 3 Sec II] [12] Also known as talc, this ceramic capacitor variant was able to closely match the temperature coefficient of mica.[7]

Rutile ceramic capacitors were introduced with a dielectric constant of 10 times that of steatite. It was typically blended with steatite to get a better temperature coefficient. A ceramic composition wth barium titanate (BaTiO3) was first discovered in 1941. Barium titanate was quickly found to be able to exhibit a dielectric constant over 1000; an order of magnitude greater the best at this time (rutile - $Ti0_2$). It was not until 1947, that barium titanate appeared in its first commercial device, phonograph pickups.[11][6][1, Ch 3 Sec III] Today barium titanate is still seen in multi layer ceramic capacitors.

Multi-layer ceramic capacitors are the current leading technology in commercially

produced units. They are divided up into three classes. Class 1 type MLCCs are known for their extremely good temperature characteristics. COG/NPO types can have 0-30ppm/^{o}C. These capacitors are typically made by combining TiO_2 with additives in order to adjust its temperature characteristics[19]. Additinally, class 1 ceramics have comparitively poor volumetric efficiency, and will tend to come in larger packages than class 2 ceramics of the same capacitance value. Class 2 types typically have worse temperature coefficients than type 1 types, but they have a much higher volumetric efficiency.They are constructed with a ferroelectric base material, typically Barium Titanate.[19]. Class 2 ceramic capacitors are the most common type of ceramics used. Class 3 types have very high capacitance, but a working voltage of several volts.[6][1, Ch 3 Sec VI][5]. They were originally developed as a potential replacement for liquid electrolytics, but have fallen out of favor due to the advances in Class 2 ceramics to the point where the gap between these two in terms of maximum capacitance is no longer viable[30].

Bell labs invented the first solid tantalum capacitor in 1956. They created it in conjuncture, and for, transistors.[3, f. 56-64] Tantalum capacitors typically have better characteristics than aluminum electrolytics, but have a lower maximum capacitance and working voltage.[14]

Sprague patented the first commercially viable solid tantalum capacitor in 1960. It offered an increased capacitance per unit volume and greater reliability.[24] In the 1970s, Sprague released the first surface mount tantalum capacitor.[26]

One of the historical problems with tantalum capacitors has been a limited supply of tantalum in the world market. This has occasionally caused price spikes in the material, hurting the tantalum capacitor market. As a result of the price spike around 1980, manufacturers created finer grain tantalum powders. This allowed a unit to be made with less overall tantalum, reducing price and package size.[9, ch 3.1]

3 Capacitor Parameters

3.1 Comments

*In Section 3.1 you could mention what characteristics are important for that application. And capacitors for switching power supplies are conspicuously absent. *Do you want to get into capacitor parameters such as stability, temperature operating range, working voltage, peak or surge current, etc

3.2 Practical Capacitor Uses

Before getting into the individual capacitor parameters, I will explain some of the basic uses for capacitors. Each of the individual parameters will be important and have a direct effect on the uses described here. One should be careful to remember that any model consisting of the parameters listed in this section (and others) only describes an approximation of what is happening inside of a capacitor. Models and capacitor parameters will never be 100% correct, but can be made with fairly high accuracy. As long as the designer understands the circumstances in which the models are accurate, he can use them to make a better circuit.

The most basic reason for wanting to use a capacitor is that it has the ability to store charge, which is close to the same thing as saying that it has the ability to store energy. It can store and release energy quickly to be able to react to the needs of the circuit.

3.2.1 Power Supply Bypassing

One of the most common uses of capacitors in bypassing a DC power supply (see Figure: 1). Without a bypass capacitor, a portion of the noise or any voltage spikes on the input to a power supply is passed to the output. A capacitor from the input to ground acts as a local charge reservoir to smooth out any non-DC components on
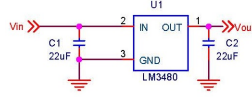
Figure 1: Power Supply Bypassing Circuit
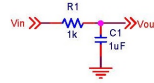
Figure 2: Analog Filtering Circuit

the input voltage. Putting a bypass capacitor on the output of a supply prevents load surge currents from causing the output voltage to dip. This is especially important with digital chips, as their high frequency switching can result in glitching if the supply is not properly bypassed.

3.2.2 Analog Filtering

Another use for capacitors is in analog filtering. The lowpass filter in Figure: 2 attenuates frequencies above a cutoff point, set by the values of the resistor and capacitor. Low pass filters are needed in many applications, such as anti-aliasing, clock filtering, and integration.
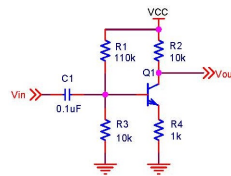
Figure 3: DC Blocking Capacitor

[20][ch 2.08 fig 2.27 pg 77]
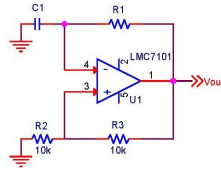
Figure 4: Oscillator Circuit

[20][ch 5.13 fig 5.29 pg 285]
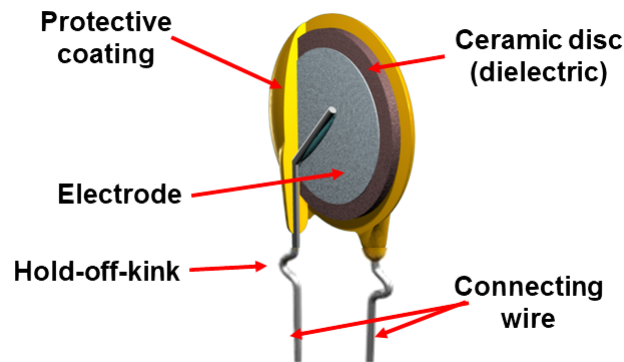
Figure 5: Power Factor Correction Circuit

3.2.3 DC Blocking

Designers often take advantage of capactors' characteristic of passing AC current while blocking DC current. As in Figure: 3, a capacitor can be used to block a DC offset before an amplifier.

3.2.4 Oscillators

Capacitors are also used in oscillator circuits. The relaxation circuit in Fig: 4 generates a square wave output at a frequency determined by the RC time constant of the passives.

3.2.5 Power Factor Correction

The inductors in modern DC-DC switching supplies have required increased attention to the engineering phenomenon know as power factor. Any electrical load with an inductive component causes the supplied current phase to lag the voltage phase. This effect decreases the efficiency of the power distribution and also has the ability to cause stability issues. A capacacitor can be used as a simple, passive way to move the power factor back towards the ideal state (See Figure: 5). [21]

3.3 Capacitance

There is a distinct difference between a capacitor and capacitance. While a capacitor's dominant characteristic is capacitance, it cannot be modeled entirely as such in most practical applications. There are also various inductive and resistive components to a capacitor that are important in various circumstances.

$$C = \frac{Q}{V} \tag{1}$$

Capacitance is the ability to store electrical charge. Equation: (1) says that capacitance is stored charge that is spread throughout a volume. A device that can store a lot of charge in a small area has a large capacitance.The basic equation for a commercial capacitor is seen in Equation: (2).

$$C = \frac{\epsilon_0 A}{d} \tag{2}$$

When using a capacitor in a single-pole low-pass filter, the cutoff frequency can be determined by Equation: (3). The circuit designer will choose a value for C and R in order to meet the cutoff frequency restraint.

$$f = \frac{1}{2\pi RC} \tag{3}$$
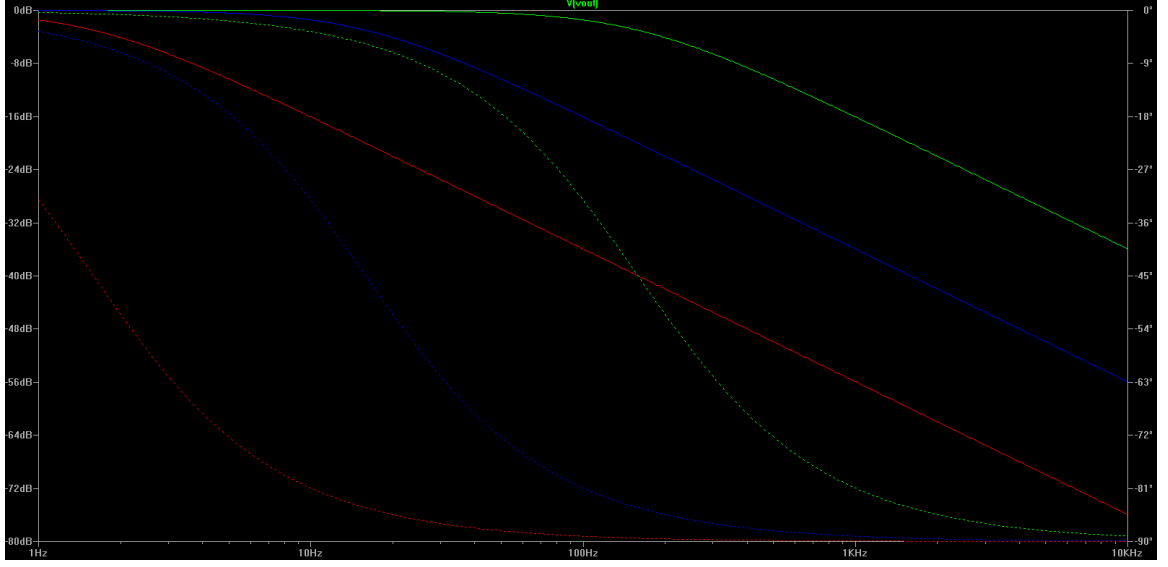
Figure 6: Low Pass Filter – Varying C

Varying the capacitance used in the filter will move the cutoff frequency and consequently get a different response in the filter. The effect of this can be seen in Figure: 6.

3.4 Impedance

The impedance of a capacitor is the "AC resistance" of the device. It determines the AC current that will flow when an ac voltage is applied to the capacitor via Ohm's law (Equation: (4)). An ideal capacitor has only a single capacative element and its impedance can be described via Equation: (5). The two main things to notice are that the impedance is frequency dependent and it is purely imaginary (reactive).

$$\vec{V} = \vec{I}\vec{Z} \tag{4}$$

$$\vec{Z} = \frac{1}{j\omega C} \tag{5}$$

Figure 7: Capacitor Magnitude Over Frequency

$$Z = |\vec{Z}| = \frac{1}{\omega C} \tag{6}$$

In most AC applications we look at the magnitude of the impedance. Real capacitors have a more complicated impedance, but with an ideal capacitor we can simplify the magnitude equation down to Equation (6)

When capacitors are used in bypassing power supplies, the idea is to have a low impedance for common or expected noise frequencies. One may be tempted to choose a large valued capacitor to use for bypassing a wide range of frequencies. This turns out to backfire in practical situations, due to other parasitics in a real capacitor. For any capacitor, the impedance equation is more complicated, and the impedance value will begin to increase with frequency after some point. This will cause the designer to choose several different valued capacitors in parallel when bypassing a power supply or sensitive component. We will see later that the frequency plot of a capacitor will end up being more complicated than the simplified version seen in Figure: 7.

3.5 Phase

The phase of a combination of resistive and reactive components can be written as in Equation: (7).

$$\phi = tan^{-1}[\frac{X_c}{R_c}] \tag{7}$$

For an ideal capacitor, having no resistance and only capacitance, the phase angle can be simplified to:

$$\phi = -i = -90^0 \tag{8}$$

The practical implication of this can be seen in the phase response of a low pass filter (Figure: 6). The capacitor introduces a phase lag relative to the input signal's frequency. If you would compare the input and output signals in time, the output's peak would lag behind the input's by the phase amount predicted in the phase response.

3.6 ESL

The Equivalent Series Inductance (ESL) of a capacitor is a lumped estimate of all of the inductive components of a capacitor. It is typically modeled as an inductor in series with the bulk capacitance (See Figure 8).

Adding ESL to the capacitive model creates a new impedance equation (Equation: (9)). Note that for L<<C, this equation simplifies to Equation: (5) for low frequencies. In otherwords, the ideal impedance equation can be reasonably used for "low" frequencies.

$$\vec{Z_c} = j\frac{\omega^2 LC - 1}{\omega C} \tag{9}$$

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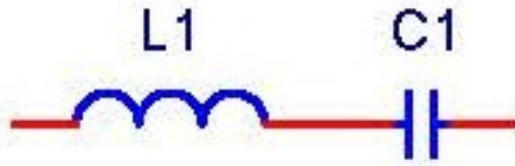
Figure 8: ESL Capacitor Model
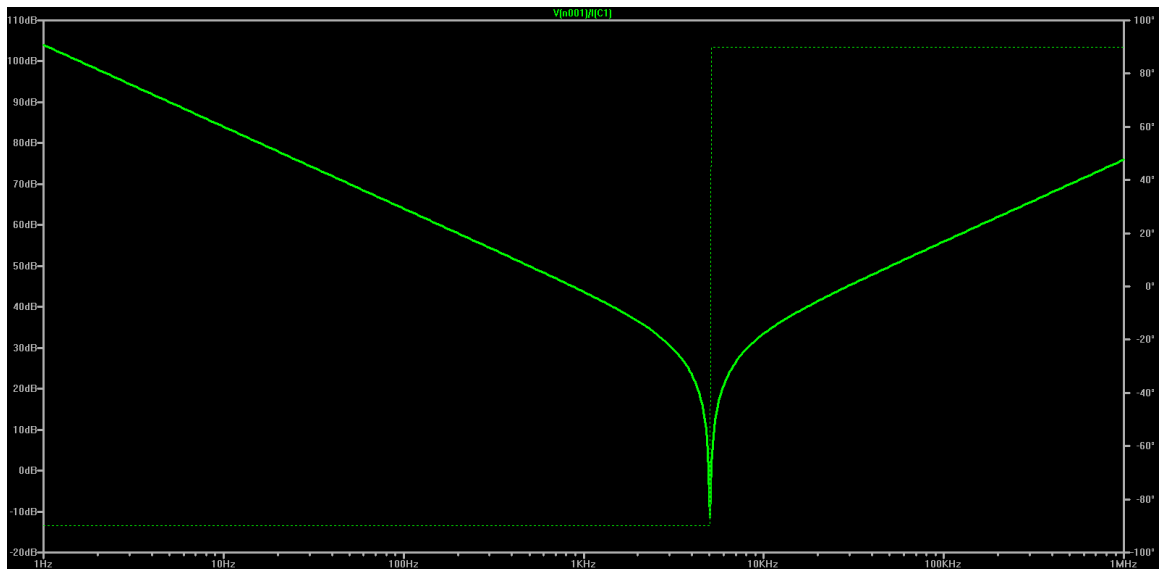
Figure 9: Capacitor Impedance with ESL

Figure: 9 shows a graphical representation of a capacitor's magnitude and phase once ESL is considered. This plot shows that after a resonance point, the impedance of the inductor (which increases with frequency) will begin to dominate. This makes the capacitor uneffective as a bypass element at frequencies higher than its resonance point. Typically, this frequency point and the capacitor's value have an inverse relationship. This is why you will see power supplies and sensitive chips being bypassed by a range of different valued capacitors.
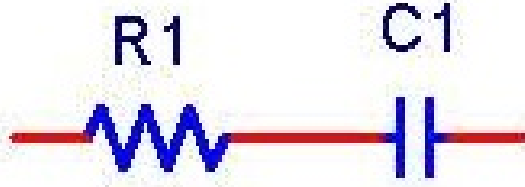
Figure 10: ESR Capacitor Model

3.7 ESR

The Equivalent Series Resistance (ESR) is the practical result of the fact that the materials used to create a capacitor have resistance. In simple cases, this can be approximated by a resistance in series with a capacitor (See figure: 10).

ESR becomes is important when thinking about DCDC switch mode power supplies. In this situation, a bypass capacitor is used to reduce the ripple voltage on the output of the converter. The AC current will pass through the ESR and dissipate heat as per Equation: (10)

$$P_{ESR} = I^2_{C,RMS} * ESR [16]$$ (10)

Another important thing to note about ESR is that even though it is modeled as a resistance, it is not constant across all frequencies. It is a simplification of the resistive and capacitive elements in a capacitor that are dominated by resistance (Equation (11).

$$\vec{Z_c} = ESR + j * (\omega L - \frac{1}{\omega C}) [16]$$ (11)

3.8 Resonance Frequency

Once C, ESL, and ESR are included into the capacitor model, a parameter know as the self-resonant frequency becomes evident. Equation: (11) shows that when
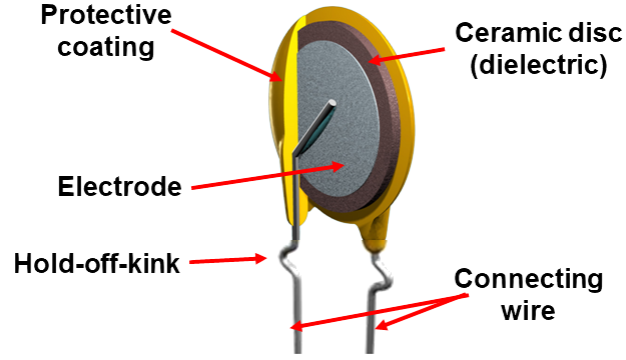
Figure 11: Dissipation Factor Plot

$Z_{ESL} == Z_C$, the capacitor is at its resonance point. At this frequency, the capacitor's impedance is determined solely by the ESR at that frequency. This frequency can be calculated by Equation: (12).

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

3.9 Dissipation Factor

Dissipation factor, otherwise known as the loss-tangent, is a measure of the energy stored to the energy dissipated per cycle. It is a measurement of the efficiency of the capacitor. The DF can be quantified through Equation: (13).

$$D = \frac{ESR}{Xc} \tag{13}$$

The loss tangent can be seen in Figure: 11. The greater the angle, the more efficient the capacitor will be.

3.10 Quality Factor

$$Q = \frac{1}{D} \tag{14}$$

Figure 12: Dielectric Absorption

The Quality Factor, Q, of a capacitor is found by taking the reciprocal of the dissipation factor, Equation: (14). It is defined as the ratio of the energy stored to the energy dissipated per cycle.

3.11   Insulation Resistance

Every capacitor will have some DC leakage resistance associated with it. This measurement is attenuated by the insulation resistance of the capacitor. A high insulation resistance in a capacitor will increase its ability to store charge. This characteristic is especially important in sample and hold circuits.

3.12   Dielectric Absorption

Dielectric Absorption, DA, in a capacitor is a characteristic which describes the unit's ability to "regenerate" a charge after being shorted to ground for a brief time.

As seen in Figure: 12, a capacitor can be modeled with multiple RC element, of a much greater time constant, in parallel with the bulk capacitance. When the main capacitor is shorted to ground, and then released, the other capacitors may not have released their energy. After several minutes, they can recharge the main capacitance

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to a significant portion of its original charge. This is why large valued electrolytic capacitors get shipped with a resistor across their terminals.

3.13 Old

This section will list and explain a large number of capacitor parameters. It will not deal with any analysis or measurement.

1. Impedance

2. Phase

3. Capacitance

4. Reactance

5. Equivalent Series Resistance (ESR)

6. Equivalent Series Inductance (ESI)

7. Leakage current

8. Dissipation factor

9. Quality factor

10. Dielectric absorption

11. Loss Tangent

4 Capacitor Modeling

Many designers have a need to simulate the response of the individual components in their systems to impulse and steady state inputs. When dealing with passive

electronic components, the device is typically modeled as a combination of various resitors, capacitors, and inductors. The model chosen is often due to either the required accuracy or a specific characteristic of the component that needs to be modeled. When characterizing a new component, the complex frequency response is recorded and then fit to a model. In this section, a progression of regression techniques will be evaluated for their ability to fit the measured frequency response of a capacitor to a polynomial equation. Then the accuracy of various capacitor models will be explored in regards to the fit. All models will attempt to fit the data from Figure: 13.

Figure 13: GRM31MR71H105KA88 Capacitor Data

4.1 Regression Analysis

4.1.1 Basic LSE

At its core, regression analysis is an optimization problem whose purpose is to fit the equation of a line to a data set. A commonly use regression analysis technique is called the Least Equares Estimate (LSE). It attempts to find a model which minimizes the squared error between an emperical set of data and itself.

The first step in applying an LSE is to choose the form of the equation that best represents the data. The equation of a line, Equation: (15), is chosen when only a simple linear fit is needed. Then the squared error equation is generated, as in Equations: (16) & (17).

$$y = a_0 + a_1 x \tag{15}$$

$$E^2 = \sum_{i=1}^{n} (y_i - y)^2 \tag{16}$$

$$E^2 = \sum_{i=1}^{n} (y_i - (a_0 + a_1 x_i))^2 \tag{17}$$

In order to minimize the squared error over the data set, one needs to take the partial derivate of Equation: (17) with respect to each of the unknown parameters, the coefficients, seperately. While a_0 and a_1 will be constants in the final equation, they are treated as variables here until they are known. Conversely, all x_i values are treated as constants. This results in Equations: (18) & (19).

$$\frac{\partial E^2}{\partial a_0} = 0 = \sum_{i=1}^{n} (-2y_i + 2a_0 + 2a_1 x_i) \tag{18}$$

$$\frac{\partial E^2}{\partial a_1} = 0 = \sum_{i=1}^{n} (-2y_i x_i + 2a_0 x_i + 2a_1 x_i^2) \tag{19}$$

Up to this point most LSE analyses follow the same basic path. But the rest of the steps depend upon the complexity of the model and solution techniques. The following steps in the basic LSE use transformations and substitutions to solve for the unknown variables. In our case, we can use Equation: (20) to remove the summation terms from the equation.

$$\sum_{i=1}^{n} y_i = \bar{y}n \tag{20}$$

This results in Equations: (21) & (22) with solutions shown in Equations: (23) & (24). The empirical data is then used to find the values of a_0 and a_1. At this point, the line can be used to estimate new points on the plot or to compare against other data sets.

$$0 = \bar{y} - (a_0 + 2a_1\bar{x}) \tag{21}$$

$$0 = \bar{xy} - (a_0\bar{x} + 2a_1\bar{x^2}) \tag{22}$$

$$a_0 = \bar{y} - a_1\bar{x} \tag{23}$$

$$a_1 = \frac{\bar{xy} - \bar{x}\bar{y}}{\bar{x^2} - \bar{x}^2} \tag{24}$$

An example of this type of fit can be seen in Figure: 14.

4.1.2 Levy's Technique - Complex Curve Fitting

While the basic LSE technique is sufficient for many circumstances, it is not directly applicable in situations where one needs to fit a complex line, such as a transfer function. Levy [15] shows an extension of the simple LSE example that is valid for a genaric polynomial transfer function. This method is important because it not only
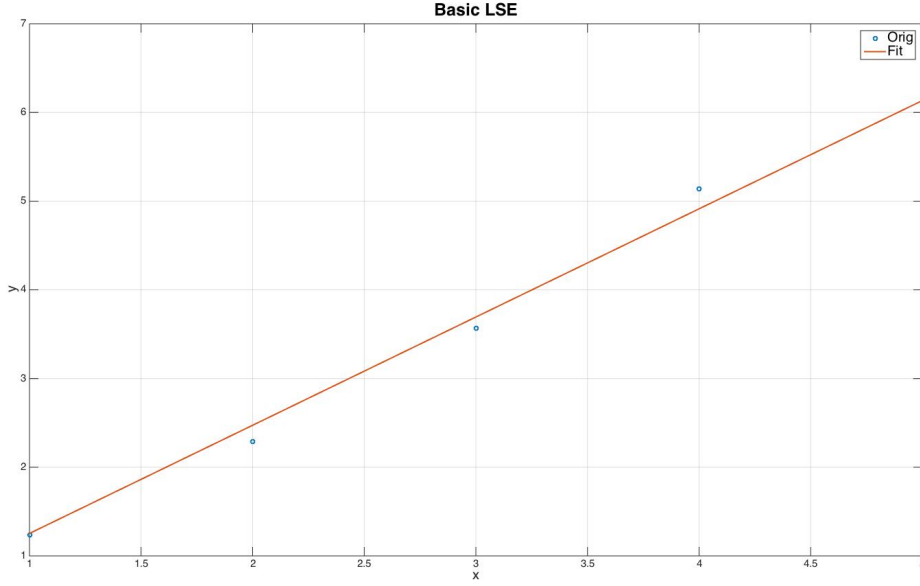
Figure 14: Basic LSE

allows for a complex-valued transfer functions, but it also prevents the nececcity of needing to rederive the system of equations for each new model.

$$G(s) = \frac{A_0 + A_1 s + A_2 s^2 + ... + A_n s^n}{B_0 + B_1 s + B_2 s^2 + ... + B_m s^m} \; [15][Eq.\ 3] \tag{25}$$

Using Equation: (25) as the genaric model, Levy shows that you can use Equations: (26), (27), (28), & (29) to simplify the series of partial derivates into a single matrix mtiplication equation shown in (30), (31), (32), & (33).

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h \; [15][Eq.\ 15] \tag{26}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k \; [15][Eq.\ 16] \tag{27}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k \; [15][Eq.\ 17] \tag{28}$$

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$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) \ [15][Eq. \ 18] \tag{29}$$

$$MN = C \ [15][Eq. \ 20] \tag{30}$$

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & \lambda_4 & \cdots & T_1 & S_2 & -T_3 & -S_4 & T_5 & \cdots \\ 0 & \lambda_2 & 0 & -\lambda_4 & 0 & \cdots & -S_2 & T_3 & S_4 & -T_5 & -S_6 & \cdots \\ \lambda_2 & 0 & -\lambda_4 & 0 & \lambda_6 & \cdots & T_3 & S_4 & -T_5 & -S_6 & T_7 & \cdots \\ 0 & \lambda_4 & 0 & -\lambda_6 & 0 & \cdots & -S_4 & T_5 & S_6 & -T_7 & -S_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots & \vdots & \vdots \\ T_1 & -S_2 & -T_3 & S_4 & T_5 & \cdots & U_2 & 0 & -U_4 & 0 & U_6 & \cdots \\ S_2 & T_3 & -S_4 & -T_5 & S_6 & \cdots & 0 & U_4 & 0 & -U_6 & 0 & \cdots \\ T_3 & -S_4 & -T_5 & S_6 & T_7 & \cdots & U_4 & 0 & -U_6 & 0 & U_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \end{bmatrix} \ [15][Eq. \ 21a]$$

$$\tag{31}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \\ \vdots \\ B_1 \\ B_2 \\ B_3 \\ \vdots \end{bmatrix} \ [15][Eq. \ 21b] \tag{32} \qquad C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ T_3 \\ \vdots \\ 0 \\ U_2 \\ 0 \\ \vdots \end{bmatrix} \ [15][Eq. \ 21c] \tag{33}$$

Levy's technique works well for applications where there is a small dynamic

frequency range and a small number of coefficients, but there a several problems with it. The first problem is that for models with a wide bandwidth, the solution to Equation: (30), involves an ill-conditioned matrix. This means that the ratio of the "largest to smallest singular value in the singular value decomosition of a matrix is ... $>= log^{-1}$(input precision). In other words, it estimates a worse case loss of precision." The second problem is that this technique favors the magnitude plot at the high frequency range.
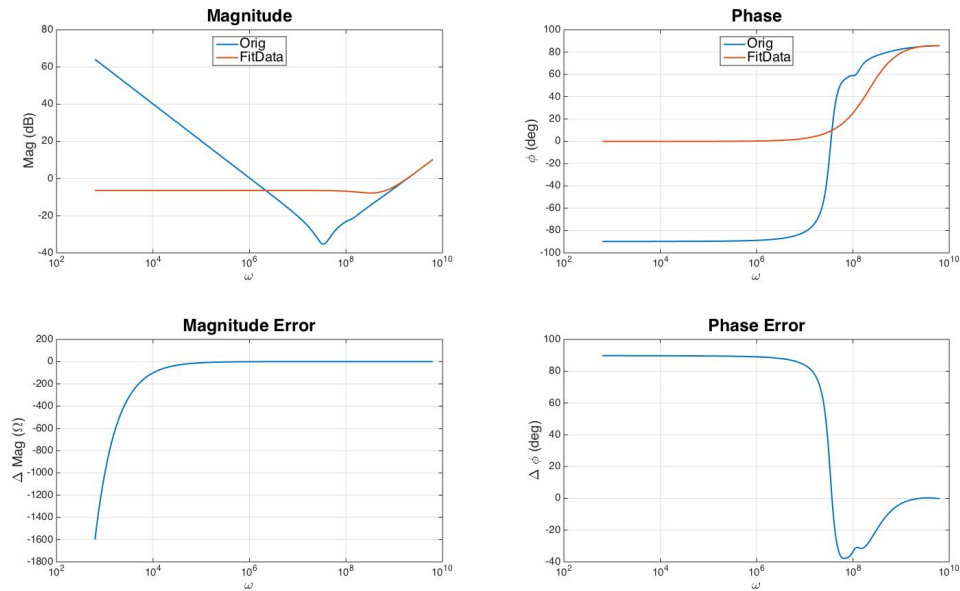
Figure 15: Levy's Technique

4.1.3   Weighted LSE

One improvement that can be made upon Levy's method is to iterate with a frequency dependent weighting function untill the error term is minimized[25]. By multiplying Levy's error function by the weighting term in Equation: (34), we get Equation: (35), which can be minimized to obtain a new system of equations. The L subscript stands

for the current iteration, while $L - 1$ stands for the previous iteration.

$$W_{kL} = \frac{1}{|Q(jw_k)_{L-1}|^2} \text{ [25]} \tag{34}$$

$$E = \sum_{k=1}^{n} |\epsilon_k'|^2 W_{kL} \text{ [25][Eq. 7]} \tag{35}$$

Equations (30), (31), (32), & (33) are the same, with Equations (26), (27), (28), & (29) being replaced with Equations: (36), (37), (38), & (39).

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h W_{kL} \text{ [25][Eq. 9]} \tag{36}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k W_{kL} \text{ [25][Eq. 10]} \tag{37}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k W_{kL} \text{ [25][Eq. 11]} \tag{38}$$

$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) W_{kL} \text{ [25][Eq. 12]} \tag{39}$$

This particular iteration method is not gauranteed to converge. Figure: 16 shows that, for this data set, the squared error of the magnitude and phase do not converge after a particular number of iterations. Furthermore, they do not reach their minimums at the same iteration. In order to select the desired iteration, the magnitude and phase squared plots are normalized as in Equation: (40). The index of the minium of Figure: 16 is selected as the best fit.

$$n = min(Emag/max(eMag) + Epha/max(ePha)) \tag{40}$$

Figure: 18 shows that this method can result in a much improved result over the Levy's original method, as seen in Figure: 15.

25
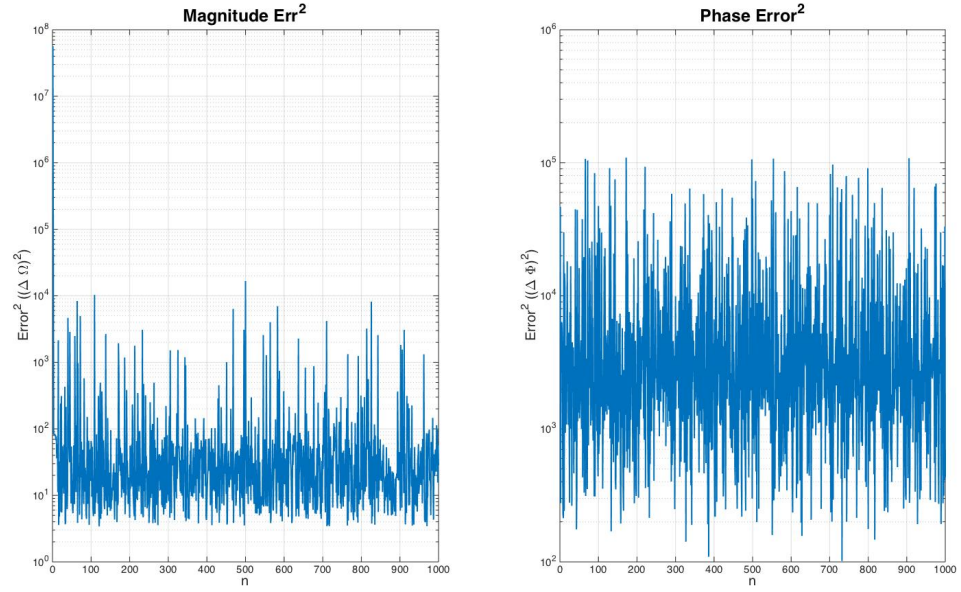
Figure 16: LSE + Iteration – Magnitude and Phase Error
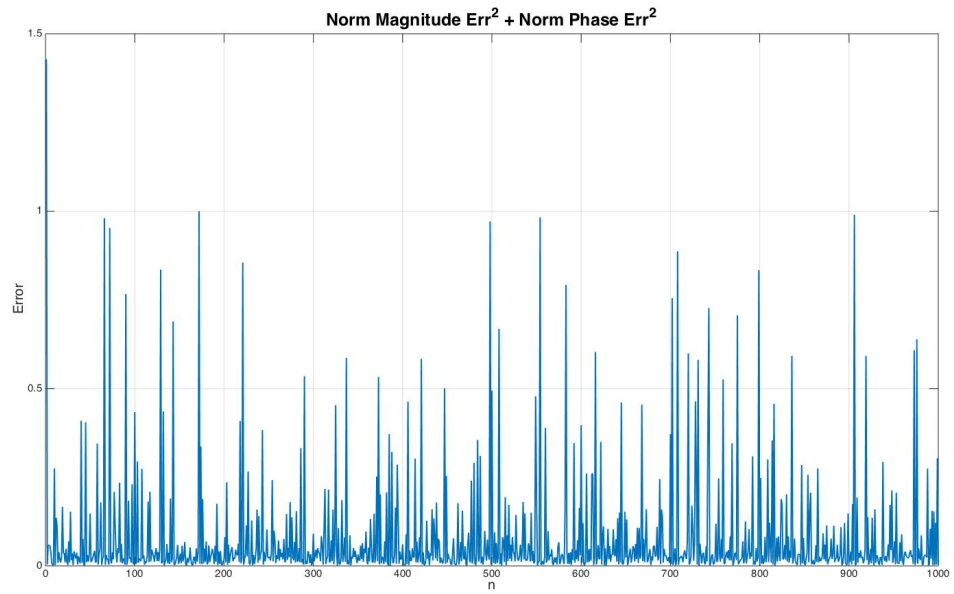
Figure 17: LSE + Iteration – Combined Error

26
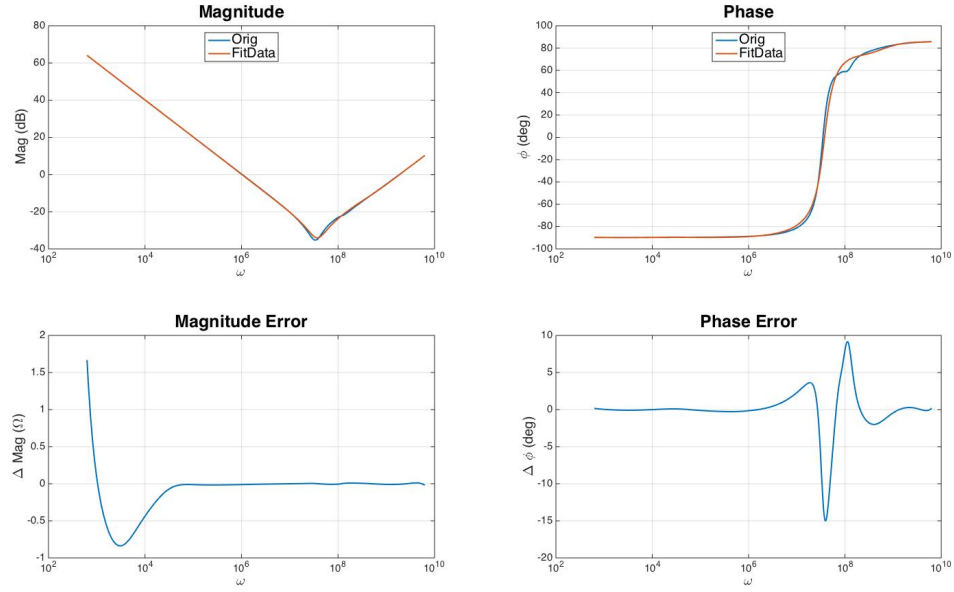
Figure 18: LSE + Iteration

4.2 Modeling

This section will investigate several of the most common capacitor models. It will show how to fit them to a data set with Levy's method described in Section: 4.1, and will describe their effectiveness and limitations in doing so.

4.2.1 6 Term Model

Figure 19: 6 Term Model

27

The model shown in Figure: 19 shows several of the most important parameters for a capacitor. It's impedance, shown in Equation: (41), can be used as the basis for a regression analysis.

$$\bar{Z}(s) = \frac{(R_E + R_L) + (L_E + C_D R_D R_E + C_D R_D R_L + C R_E R_L + C_D R_E R_L)s}{1 + (C_D R_D + C R_L + C_D R_L)s + C C_D R_D R_L s^2}$$
$$+ \frac{(C_D L_E R_D + C L_E R_L + C_D L_E R_L + C C_D R_D R_E R_L)s^2 + C C_D L_E R_D R_L s^3}{1 + (C_D R_D + C R_L + C_D R_L)s + C C_D R_D R_L s^2} \tag{41}$$

$$\bar{Z}(s) = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3}{b_0 + b_1 s + b_2 s^2} \tag{42}$$

For this model Equations: (31), (32), & (33) simplify down to Equations: (43), (44), & (45).

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & T_1 & S_2 \\ 0 & \lambda_2 & 0 & -\lambda_4 & -S_2 & T_3 \\ \lambda_2 & 0 & -\lambda_4 & 0 & T_3 & S_4 \\ 0 & \lambda_4 & 0 & -\lambda_6 & -S_4 & T_5 \\ T_1 & -S_2 & -T_3 & S_4 & U_2 & 0 \\ S_2 & T_3 & -S_4 & -T_5 & 0 & U_4 \end{bmatrix} \tag{43}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \\ B_1 \\ B_2 \end{bmatrix} \tag{44} \qquad C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ T_3 \\ 0 \\ U_2 \end{bmatrix} \tag{45}$$

Using this model, the regression analysis output described in Section: 4.1.3 can be seen in Figure: 20. The fit tracks the original data well, except for low frequencies and near resonance.

28
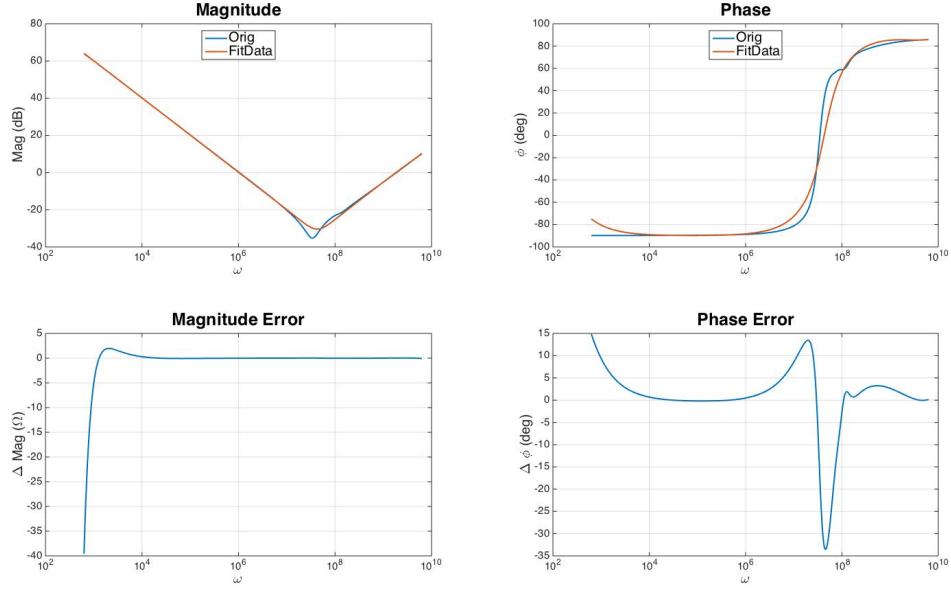
Figure 20: 6 Term Model: Bad Initilization

Equations: (53) shows solution for the polynomial coefficients. Using Equations: (42) and (42), the circuit parameters can be found through Equations: (46)-(52), with the solution as seen in Equations: (53) & (54). Even though the polynomial coefficients gave an acceptable fit to the data, it resulted in unaceptable circuit parameters. Since C and R_D are negative, this model is not physically realizable.

$$a_0 = R_E + R_L \tag{46}$$

$$a_1 = L_E + C_D R_D R_E + C_D R_D R_L + C R_E R_L + C_D R_E R_L \tag{47}$$

$$a_2 = C_D L_E R_D + C L_E R_L + C_D L_E R_L + C C_D R_D R_E R_L \tag{48}$$

$$a_3 = C C_D L_E R_D R_L \tag{49}$$

$$b_0 = 1 \tag{50}$$

$$b_1 = C_D R_D + C R_L + C_D R_L \tag{51}$$

$$b_2 = C C_D R_D R_L \tag{52}$$

$$a_0 = 5.9991E^{+03}$$

$$a_1 = 1.7934E^{-04} \qquad\qquad C = -8.2563E^{-10}$$

$$a_2 = 3.3158E^{-12} \qquad\qquad R_E = 3.1886E^{-01}$$

$$a_3 = 6.8295E^{-22} \qquad (53) \qquad L_E = 4.8551E^{-10}$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad (54)$$

$$b_0 = 1.0000 \qquad\qquad R_L = 4.8551E^{-10}$$

$$b_1 = 5.9057E^{-03} \qquad\qquad C_D = 9.8536E^{-07}$$

$$b_2 = 1.4067E^{-12} \qquad\qquad R_D = -2.8824E^{-01}$$

The problem comes with the author's [25] suggestion that the initial guess for $Q(jw_k) == 1$. While an initial guess is required to calculate the weighting function during the first iteration, it causes the stated problem for this application. Equations: (55) & (56) show that this initial condition does not yield a rational solution for the circuit parameters.

$$a_0 = 1$$

$$a_1 = 1 \qquad\qquad C = INF$$

$$a_2 = 1 \qquad\qquad R_E = INF$$

$$a_3 = 1 \qquad (55) \qquad L_E = INF$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad (56)$$

$$b_0 = 1 \qquad\qquad R_L = IND$$

$$b_1 = 0 \qquad\qquad C_D = IND$$

$$b_2 = 0 \qquad\qquad R_D = IND$$

If we instead start with the rational set of circuit parameters seen in Equation: (58), the starting coefficients are as seen in Equation: (57).

$$a_0 = 2$$

$$a_1 = 5 \qquad\qquad C = 1$$

$$a_2 = 4 \qquad\qquad R_E = 1$$

$$a_3 = 1 \qquad (57) \qquad L_E = 1$$

$$b_0 = 1 \qquad\qquad R_L = 1 \qquad (58)$$

$$b_1 = 3 \qquad\qquad C_D = 1$$

$$b_2 = 1 \qquad\qquad R_D = 1$$
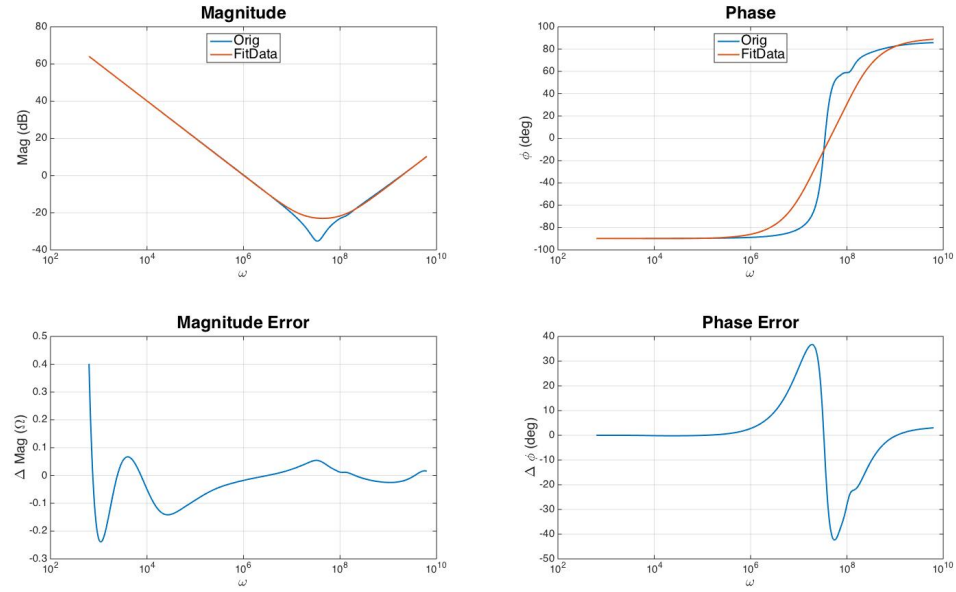
Figure 21: 6 Term Model: Good Initilization

Figure: 21 shows a good fit across the frequency spectrum for both magnitude and phase. The model does deviate at resonance, but that is insurprising, as the number of parameters in the model is fairly low.

Input Scale	0 to +10V for 0 to 5kV
Input Impedance	1 MΩ
Accuracy	±0.2% of full scale
Update Rate	15 Hz
Output Slew Rate	<0.3s for 0 to full scale (full load)

Table 1: SRS PS350 External Voltage Control Characteristics

[28] [27]

5 Measurement Circuitry

This section describes the schematic design used to meet the goals set out in the Abstract (Section: 0.2). The schematic can be found in the Appendix section: 7.

5.1 DC Bias

A DC bias is needed to conduct AC measurements as well as to allow for measuring discharge curves of the DUT. In order to determine the effect of the DC bias on the DUT, it is necessary to conrol that quantity. This section describes the circuitry (Schematic Page: 3) used to provide a means to programatically control the DC bias from 0 to 500V. The supply used is a Stanford Research Supply (SRS) PS350. It accepts a DC control signal, which is supplied by the circuit through a DAC. If different supply characteristics are needed, it can be swapped out with any supply. A genaric RS232 bi-directional port (Schematic Page: 10) is provide to control the supply in this situation.

The SRS Supply's specifications can be seen in Table: 1. The output of the PS350 can either be set manually or with a 0-10V control voltage. This circuitry will take advantage of this analog input at a gain of 500.

The analog control uses an AD7391, 14-bit DAC with an internally generated

reference. It is controlled via a SPI bus connected to a microcontroller. The update rate of this device is not important to this application because it will be set infrequently and only when the system is not actively collecting data. The output signal of the DAC is fed into an op amp which acts as a voltage limiter for safety. This clamps the control signal at 1.5V and the PS350's output at 750V.These numbers are theoretical and will degrade from ideal due to the SRS's response to the control signal, the noise levels in the system, and various other factors, such as temperature.

The DAC has a 2.5V internal reference. With 14 bits, that gives the control signal an ideal resolution of $150\mu V$ and the PS350 an output resolution of $76mV$.

5.2   Current Measurement

Each of the tests utilize the low-side current measurement circuit. The AC measurement tests provide a known voltage across the DUT and then the current is used to construct the impedance. The discharge tests use the current measurement circuit to capture the current through the DUT over time as its energy drains.

Refdes	Value	Range	
R5	5	Hi	1A - 1mA
R6	5k	Med	1mA - 1uA
R7	5M	Low	1uA - 1nA

Table 2: Current Measurement Ranges

The current measurement circuit utilizes a transimpedance amplifier designed from the reference circuit in [4]. It utilizes 3 switched, feedback stages to measure 9 decades of current (See Table: 2). The circuit creates a virtual ground at the negative terminal of the DUT and then uses one of the feedback paths to create a voltage for a digitizer. Using a low-side current measurement circuit is beneficial in this circumstance because it allows low voltage circuitry to condition and measure

a signal without needing to see the high DC voltage on the postive terminal of the DUT. The output voltage is calculated by Equation: (59).

$$Vo = I * R_f \tag{59}$$

*Add transitor in increase the Op Amp's current drive capability. *Change capacitors in feedback loop. *Add Salen-key filter to output *Exlain difference in two buffering stages

The output will be buffered and then filtered and digitized dependent of the specific test of interest.

5.3 Charge

This section of the circuitry is meant as a preperation stage for the other tests. It operates by setting the current measurement to High, closing the Charging Relay (LS4), and then ramping the DC Bias voltage with the high current measurement stage open. LS4 can be opened or left closed, dependent on the needs of the test.

5.4 Discharge Circuitry

The discharge circuitry provides a means to determine the bulk capacitance value of the DUT from the RC time constant. Once the DUT is charged to the desired voltage, the charging relay will open and then the high-current discharge relay will close. The current through the DUT will be measured as it decays.

There are 3 switched discharge stages that allow for the decay rate to be regulated. Each stage allows for a range of voltages and capacitances needed to stay within safety and operational constraints. As seen in Figure: 22, there are two constrainsts on both the voltage and capacitance. The lowest valued resistor constrains the maximum voltage when using that stage due to its power rating. The other two stages are

constrained by the overall safety limit of 500VDC. The minimum capacitance for each stage is determined by setting a requirement of at least 100 ADC samples per time constant with a sampling rate of $250KSPS$. The maximum capacitance for each stage is determined by setting a maximum time constant.
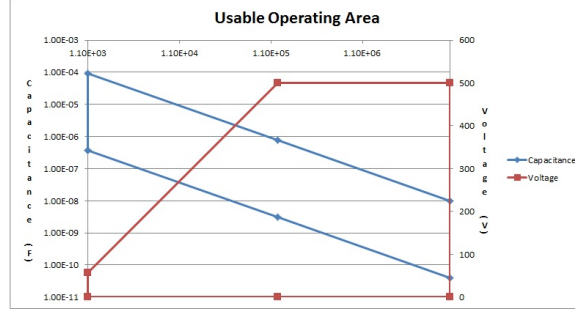
Figure 22: Operating Area

5.5   Magnitude

The magitude section takes the sinusoidal current measurement and creates a DC output by with a dual difference amplifier package. This technique as seen in [18] provides a method to measure the rms value of the AC current through the DUT. The first difference ampliflier is configured as a voltage follower. Since this circuit operates only from a single power rail, it passes the positive going portions of the waveform and clamps to ground for th negative going portions of the waveform. The second difference amplifier operates in different modes, based upon the output of the first differential amplifier. During the negative going portions of the waveform, its positive terminal is held at ground, and it operates as a unity gain, inverting amplifier. This rectifies the input signal to the output. During the positive going portions of the waveform, positive input terminal is held at the value of the input terminal. This forces the second difference amplifier to act as a voltage follower. In this manner, the circuit performs a full-wave rectification on the signal, which is then filtered and fed

35

to the ADC for digitization.

5.6   Phase

This section explains the circuitry used to measure the phase difference between the input voltage and the output current. This measurement, combined with the magnitude measurement, will allow for a complete impedance measurement at each frequency step of a test. The comparator circuit is configured as a sine to square wave converter. The two square wave signals will be fed directly into a timer input of the MCU. The MCU will measure the time between the two signals to determine their phase difference.

5.7   Communications

This section will describe the circuitry used to communicate to off-board processors.

5.7.1   USB

The USB section is used to communicate with a PC for data logging and data post processing. This circuitry centers around a FTDI FT232H serial to USB chip. It allows seemless USB communication to a PC's com port with the MCU only needing to use a UART port. This significantly lowers the complexity of the communication bus, as the MCU is not repsonible for running the USB stack.

5.7.2   RS-232

The board also has two, bidirectional RS-232 ports. They are able to be used for general purposes, but will most often be used for communicating with a sine-wave generator and an alternate DC Bias supply.

6 Conclusion

This section will summerize the methodologies used to solve the stated problem.

7 Future Work

This section will describe the future work needed to be accomplished in order to complete and further the stated goals of this thesis. It will mostly focus on the practical circuitry implementation and other aspects needed to make it a viable tool.

Appendix

TABLE OF CONTENTS

Title		
	TABLE OF CONTENTS	
Size	Document Number	
B	DELIBERO_THESIS	
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POWER SUPPLIES

D

C

B

A

5 4 3 2 1

DC BIAS CONTROL

5V   1.5V   DCBIAS_CTRL

C1   C2   C3   C4   C5   C6
10uF 0.1uF 10uF 0.1uF 10uF 0.1uF

1.5V

U1
5V
1 VDD   VOUT 4
DCBIAS_CS 5 SYNC   VFB 3
DCBIAS_SCLK 6 SCLK VREFOUT 2
DCBIAS_MOSI 7 DIN
8 GND
AD5640

U2
DCBIAS_CTRL
TLV341

J1
1
2
BNC

J2
DCBIAS
1
2
BNC

DC BIAS CONTROL

Title	DC BIAS CONTROL
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DISCHARGE CIRCUITRY

Title	DISCHARGE CIRCUITRY
Size B	Document Number DELIBERO_THESIS
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5V   -5V

C10 10uF | C11 0.1uF | C12 10uF | C13 0.1uF | C14 10uF | C15 0.1uF | C16 10uF | C17 0.1uF | C18 10uF | C19 0.1uF | C20 10uF | C21 0.1uF | C22 10uF | C23 0.1uF | C24 10uF | C25 0.1uF | C26 10uF | C27 0.1uF | C28 10uF | C29 0.1uF | C30 10uF | C31 0.1uF | C32 10uF | C33 0.1uF

C34 1nF
DISCHG_CUR
R16 4.64k   R17 6.49k   C37 910pF   U4 OPA365   5V   -5V
C35 2.2nF
R18 2.87k   R19 5.36k   C38 910pF   U5 OPA365   5V   -5V
C36 15nF
R20 1.4k   R21 1.62k   C39 910pF   U6 OPA365   5V   -5V
ADC_IN_DISCHG_CUR

C40 100pF
ACMEAS_CUR
R22 11.8k   R23 16.2k   C44 91pF   U7 OPA365   5V   -5V
C41 200pF
R24 7.15k   R25 13.3k   C43 91pF   U8 OPA365   5V   -5V
C42 1.5nF
R26 3.48k   R27 4.02k   C45 91pF   U9 OPA365   5V   -5V
ACMEAS_CUR_FILT

FILTERING

Title: FILTERING
Size: B
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REFCAP_A   REFCAP_B   REFCAP_C   REFOUT

PLACE NEAR VSS PIN
PLACE NEAR VDD PIN
PLACE NEAR DVCC PIN
PLACE NEAR AVCC PIN

PLACE NEAR REFCAP PIN
PLACE NEAR REFCAP PIN
PLACE NEAR REFCAP PIN
PLACE NEAR REFOUT PIN

3.3V

R28 10k   R29 10k   R30 10k   R31 10k

-5V_A 5V_A 5V 5V_A

U10

5V

R32 10k   R33 10k   R34 10k   R35 10k

Pin	Signal
48	V6
45	V5
42	V4
39	V3
36	V2
33	V1

ADC_IN6
ADC_IN_CUR_MAG
ADC_IN_SINE_IN_MAG
ADC_IN_DISCHG_CUR
ADC_IN_ACMEAS_CUR
ADC_IN_TEMP

30 VSS
31 VDD
26 DVCC
34 35 40 41 46 47 50 60 AVCC

WR/REF EN/DIS 63
REFCAP C 58 REFCAP_C
REFCAP B 56 REFCAP_B
REFCAP A 54 REFCAP_A
REFIN/REFOUT 51 REFOUT

ADC_CS 19 CS
        61 SER/PAR/SEL
        9 VDRIVE
        24 STBY

ADC_CONV_A 21 CONVST C
ADC_CONV_B 22 CONVST B
ADC_CONV_C 23 CONVST A
            62 H/S SEL

ADC_RESET 29 W/B
           28 RESET
           20 RD
           27 RANGE
ADC_BUSY   18 BUSY

R36 10k   R37 10k

DB15 64
DB14/REFBUF EN/DIS 1
DB13 2
DB12 3
DB11 4
DB10/DOUT C 5 ADC_MISO_C
DB9/DOUT B   6 ADC_MISO_B
DB8/DOUT A   7 ADC_MISO_A
DB9/HBEN/DCEN 10
DB6/SCLK 11 ADC_SCLK
DB5/DCIN A 12
DB4/DCIN B 13
DB3/DCIN C 14
DB2/SEL C 15
DB1/SEL B 16
DB0/SEL A 17

R38 10k

AD7656

AGND 32 37 38 43 44 49 52 53 55 57 59
DGND 8 25

ADC

5   4   3   2   1

C76 C77 C78 C79   C80
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF
                         DCBIAS

PLACE DECOUPLING CAPACITORS
NEAR IC POWER PINS

OPTOCOUPLER
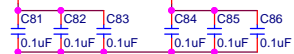
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NEAR IC POWER PINS
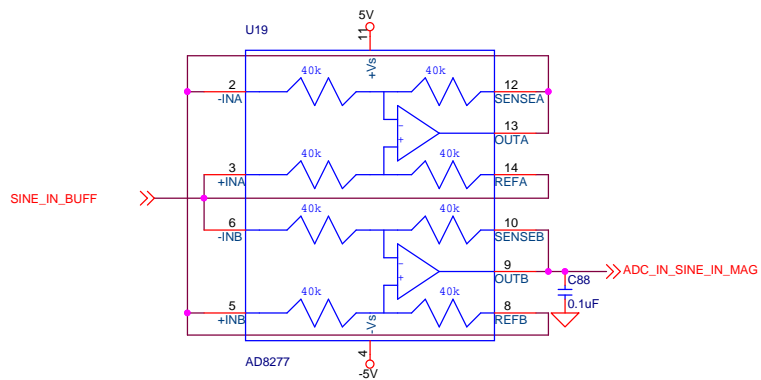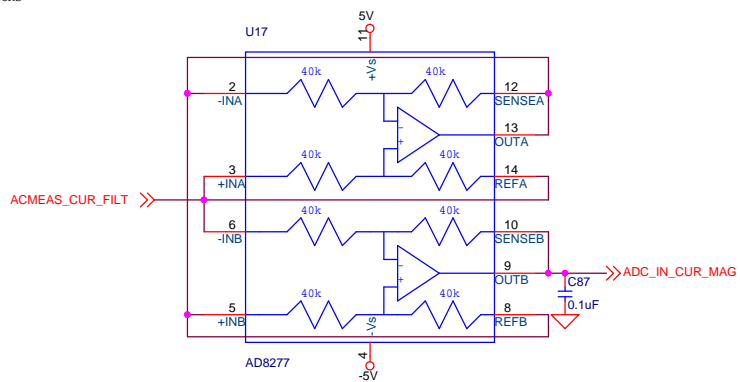
MAGNITUDE
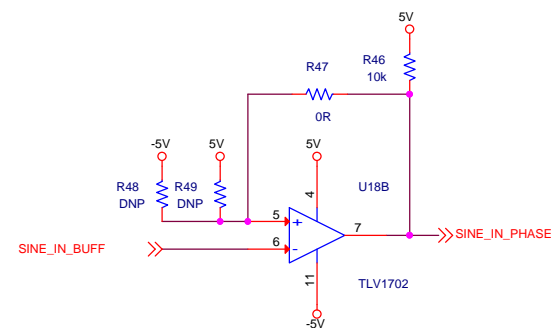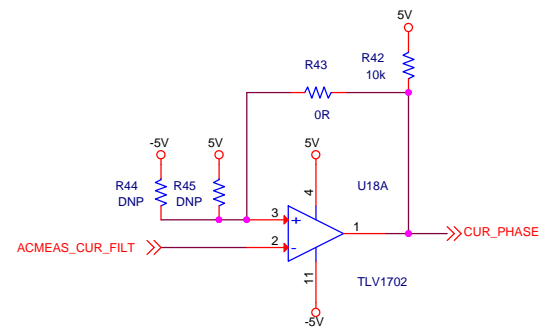
PHASE

IMPEDANCE / PHASE

5V
C89
0.1uF

5V_A
C90
0.1uF

TEMPERATURE

5V_A

U21
3 GND VDD 1
2 VOUT
MCP9700AT
R50
10k
C91
10uF
ADC_IN_TEMP

BUFFER

5V

U20

IMEAS_RELAY_1	2 A0	B0 18	BUFF_IMEAS_RELAY_1
IMEAS_RELAY_2	3 A1	B1 17	BUFF_IMEAS_RELAY_2
IMEAS_RELAY_3	4 A2	B2 16	BUFF_IMEAS_RELAY_3
DISCHG_RELAY_1	5 A3	B3 15	BUFF_DISCHG_RELAY_1
DISCHG_RELAY_2	6 A4	B4 14	BUFF_DISCHG_RELAY_2
DISCHG_RELAY_3	7 A5	B5 13	BUFF_DISCHG_RELAY_3
CHG_RELAY	8 A6	B6 12	BUFF_CHG_RELAY
OPTO_SIGNAL_RELAY	9 A7	B7 11	BUFF_OPTO_SIGNAL_RELAY

VCC 20

1 OE1
19 OE2
GND 10
74AC245
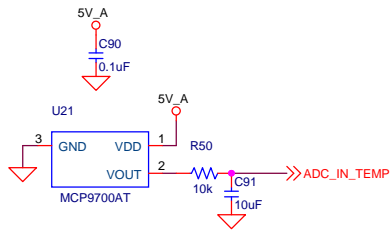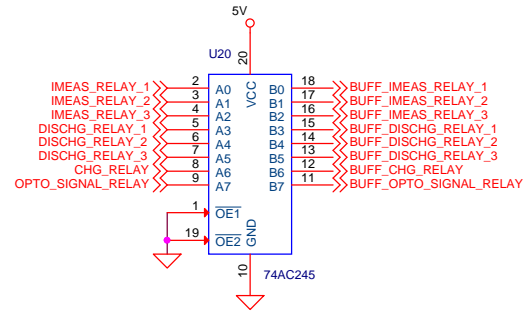
MISCELLANEOUS

Title	MISCELLANEOUS
Size	Document Number
B	DELIBERO_THESIS
Date:	Tuesday, February 17, 2015	Sheet

MCU I/O

U22
STM32F401

3.3V

Pin	Signal
1	PE2
2	PE3
3	PE4
4	PE5 — ADC_MISO_A
5	PE6
6	VBAT
7	PC13
8	PC14
9	PC15
10	VSS
11	VDD
12	OSC_IN
13	OSC_OUT
14	NRST
15	PC0
16	PC1
17	PC2
18	PC3
19	VDD
20	VREF-
21	VREF+
22	VDDA
23	PA0
24	PA1
25	PA2 — COM2_TX
26	PA3 — COM2_RX
27	VSS
28	VDD
29	PA4 — ADC_RESET
30	PA5-SPI1_SCK — CUR_PHASE
31	PA6-SPI1_MISO — ADC_MISO_A
32	PA7 — ADC_BUSY
33	PC4 — ADC_CONV_A
34	PC5 — ADC_CONV_B
35	PB0 — ADC_CONV_C
36	PB1
37	PB2-BOOT1
38	PE7
39	PE8
40	PE9
41	PE10
42	PE11-SPI4_NSS — CHARGE_CS
43	PE12-SPI4_SCK — CHARGE_SCLK
44	PE13-SPI4_MISO — CHARGE_MISO
45	PE14-SPI4_MOSI — CHARGE_MOSI
46	PE15
47	PB10 — DCBIAS_SCLK
48	VCAP1
49	VSS
50	VDD

Pin	Signal
100	VDD
99	VSS
98	PE1
97	PE0
96	PB9
95	PB8
94	BOOT0
93	PB7 — COM1_RX
92	PB6 — COM1_TX
91	PB5
90	PB4 — NJTRST
89	PB3-SPO — SWO
88	PD7
87	PD6 — DISCHG_RELAY_2
86	PD5 — DISCHG_RELAY_1
85	PD4 — CHG_RELAY
84	PD3 — OPTO_SIGNAL_RELAY
83	PD2 — IMEAS_RELAY_3
82	PD1 — IMEAS_RELAY_2
81	PD0 — IMEAS_RELAY_1
80	PC12-SPI3_MOSI — ADC_DRDY
79	PC11-SPI3_MISO — ADC_MISO_B
78	PC10-SPI3_SCLK — ADC_SCLK
77	PA15-SPI1_NSS — ADC_CS
76	PA14-SWCLK — SWCLK
75	VDD
74	VSS
73	VCAP2
72	PA13-SWDIO — SWDIO
71	PA12
70	PA11
69	PA10-USART1_RX — MCU_RX
68	PA9-USART1_TX — MCU_TX
67	PA8
66	PC9
65	PC8
64	PC7
63	PC6
62	PD15
61	PD14
60	PD13
59	PD12
58	PD11
57	PD10
56	PD9
55	PD8
54	PB15-SPI2_MOSI — DCBIAS_MOSI
53	PB14-SPI2_MISO
52	PB13-SPI2_SCK — DCBIAS_CS
51	PB12-SPI2_NSS

Y1 16MHz
C92 18pF
C93 18pF
R51 549R
NRST

C94 2.2uF
C95 2.2uF
R58 10k
R52 10k

J5 JTAG
NJTRST
JTDI
SWDIO
SWCLK
SWO
NRST
SW1
R57 10k
R53 10k
R54 10k
R55 10k
R56 10k

C96 0.1uF
C97 0.1uF
C98 0.1uF
C99 0.1uF
C100 0.1uF
C101 0.1uF
C102 0.1uF
PLACE DECOUPLING CAPACITORS NEAR
PINS 11, 19, 28, 50, 75, 100, & VBAT

C103 1uF
C104 10nF
PLACE DECOUPLING
CAPACITORS NEAR VREF+ PIN

COMMUNICATIONS

VPHY VPLL VCCIO

VREGIN 3.3V   VCORE 3.3V

U23

3.3V
C105
0.1uF

VBUS

R59
39K

VBUS

L1
100uH

J6

C109

10nF

R62 0R
R64 0R

U24

COM1_RX_EXT   RIN1   VCC   3.3V
COM2_RX_EXT   RIN2

COM1_TX   DIN1   DOUT1   COM1_TX_EXT
COM2_TX   DIN2   DOUT2   COM2_TX_EXT

C107   C1+   ROUT1   COM1_RX
0.1uF   C1-   ROUT2   COM2_RX

C108   C2+
0.1uF   C2-

C110   GND
0.1uF   V-

SN65C3232

Pin	Signal
40	VREGIN
39	VCCD
38	VCCCORE
37	VCCA
6	DM
7	DP
34	RESET
5	REF
45	EECS
44	EECLK
43	EEDATA
1	XCSI
2	XCSO
42	TEST

ADBUS0 13 MCU_RX
ADBUS1 14 MCU_TX
ADBUS2 15
ADBUS3 16
ADBUS4 17
ADBUS5 18
ADBUS6 19
ADBUS7 20

ACBUS0 21
ACBUS1 25
ACBUS2 26
ACBUS3 27
ACBUS4 28
ACBUS5 29
ACBUS6 30
ACBUS7 31
ACBUS8 32
ACBUS9 33

FT232H

D9 LED   D10 LED
VCCIO

R61 220R   R63 220R

R60 10k

USB-MICRO-B

CR1 CR2

R65 0R

U25
3.3V
VCC   CS
CLK
DI
VSS   DO

C111 0.1uF

93LC56BT-I/OT

R69 2K

R66 10k R67 10k R68 10k

3.3V

SW2

R70 12k C112 10nF C113 0.1uF

Y2
C114 18pF   12MHz   C115 18pF   R71 549R

VREGIN   3.3V   VCCIO

J8
COM1_RX_EXT
COM1_TX_EXT

COM1

J7
COM2

COM2

VREGIN
C116 4.7uF C117 0.1uF

3.3V L2 100uH VPHY C118 4.7uF C119 0.1uF

3.3V L3 100uH VPLL C120 4.7uF C121 0.1uF

3.3V C122 4.7uF C123 0.1uF

VCORE C124 0.1uF

VCCIO C125 0.1uF C126 0.1uF C127 0.1uF

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References

[1] Relva C. Buchanan, editor. *Ceramic Materials for Electronics.* Marcel Dekker, 3 edition, June 2004.

[2] What are mica capacitors?, 2014.

[3] G W A Dummer. *Electronics Inventions and Discoveries.* Institute of Physics Publishing, 1997.

[4] Steven Ehret. *Instrumentation For Anodization and In-Situ Testing of Titanium Alloys for Capacitor Anodes.* Masters thesis, Case Western Reserve University, January 2012.

[5] Richard Fore. Understanding temperature coefficients of ceramics, January 2005.

[6] S. Fujishima. The history of ceramic filters. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, 47(1):1–7, Jan 2000.

[7] James M. Gleason. Steatite for high frequency insuation. In *Journal of the British Institution of Radio Engineers.* Institute of Radio Engineers, 1945.

[8] J. Ho, T.R. Jow, and S. Boggs. Historical introduction to capacitor technology. *Electrical Insulation Magazine, IEEE*, 26(1):20–25, January 2010.

[9] Brian Holman. *The Electrical Characterization of Tantalum Capacitors as MIS Devices.* ProQuest LLC, 2008.

[10] Capacitors.

[11] B. Jaffe, W.R Cook Jr., and H. Jaffe. *Piezoelectric Ceramics.* Adacemic Press Ince (London) Ltd, 1971.

[12] J.M.Herbert. *Ceramic Dielectrics in Capacitors.* Gordon and Breach Scientific Publishers, 1985.

[13] Jill Jonnes. *Empires of Light.* Random House, 2003.

[14] Learning about electronics.

[15] E. C. Levy. Complex-curve fitting. *Automatic Control, IRE Transactions on,* AC-4(1):37–44, 1959.

[16] An efficiency primer for switch-mode, dcdc converter power supplies, December 2008.

[17] Francis Merat Michael DeLibero, Steven Ehret. Instrumentation for the anodization and characterization of titanium electrodes for electrolytic capacitors. In *Energytech, 2012 IEEE.* IEEE, May 2012.

[18] Reem Malik Moshe Gerstenhaber. More value from your absolute value circuit. *Back Burner,* 44(04), 2010.

[19] Ming-Jen Pan and Clive A. Randall. A brief introduction to ceramic capacitors. *Electrical Insulation Magazine, IEEE,* 26(3):44–50, May 2010.

[20] Winfield Hill Paul Horowitz. *The Art of Electronics.* Cambridge University Press, 2 edition, 1989.

[21] Power factor and power factor correction.

[22] Ian Poole. Silver mica capacitor.

[23] S. Pooranchandra, B. Sasikala, and Afzal Khan. *Introduction to Electrical , Electronics and Communication Engineering.* FireWall Media, 2005.

[24] Krik K. Reed. Characterization of tantalum polymer capacitors, 2005.

[25] C.K. Sanathanan and J. Koerner. Transfer function synthesis as a ratio of two complex polynomials. *Automatic Control, IEEE Transactions on*, 8(1):56–58, Jan 1963.

[26] Sprague 50 year timeline.

[27] High voltage power supplies.

[28] Series ps300 high voltage power supplies.

[29] Electronic components - dipped mica capacitors.

[30] Ceramic capacitor, November 2014.

[31] Electrolytic capacitor.

[32] Silver mica capacitor, January 2014.