DESIGN CONSIDERATIONS FOR CHARACTERIZATION OF CAPACITORS

by

MICHAEL DELIBERO

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Thesis Advisor: Dr. Merat

Department of Electrical Engineering
& Computer Science

CASE WESTERN RESERVE UNIVERSITY

TBD

CASE WESTERN RESERVE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

We hereby approve the master of science of

Michael DeLibero

candidate for the Master of Science degree*.

*We also certify that written approval has been obtained for any proprietary material contained herein.

Dedication

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Abstract

0.1 Previous Abstract

This paper presents an analysis of capacitor performance at up to 600VDC bias. The analysis is accomplished through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. All tests are recorded by means of multiple ADCs and computer analysis.

0.2 Current Abstract

This paper presents an analysis of capacitor performance degradation at up to a 600VDC bias. It proposes a testing method through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. Circuit analysis and initial prototypes will be discussed.

1 Background

The following is a list of the questions that I will be answering in my background section.

1. Where are capacitors used with a high DC bias?
    (a) What characteristics are the most important there?
    (b) What are the main failure modes?
    (c) What are the current specifications of the parts in use now?
    (d) What research is being done to develop better capacitors for this use case?
    (e) How do they currently evaluate the capacitors?
    (f) How would they benefit from my research?
2. What is the state of the art in capacitance measurement?
    (a) Impedance analyzers
    (b) Capacitance bridges
    (c) Hi pot testers
    (d) What are the good and bad points of each of these technologies?
    (e) Why do they not solve the problem that I stated?
    (f) Why does this technology not currently exist?
3. What work has been done similar to this in the past?
4. What are the important characteristics of capacitors?
5. Is there any evidence that a capacitor's properties will change over DC bias?

2 History of Capacitors

This section will chronolog the history of capacitors. It will link various introductions in the technology to advances in industry, and it will map the driving forces behind capacitor development.

Capacitors have their origin in the invention of the Leyden jar by Peter van Musschenbroek of Leiden University in 1745.[16] Before this point, scientists were able to generate static electricity through electrostatic machines, but had a very limited ability to store this electrical energy. [13] The most common design for the Leyden jar was to use a glass jar with metal foil lining the inside and out. The inner foil was typically charged via an electrostatic generator, while the outer foil was connected to ground. The charge would stay on the metal foil until a short or small resistance was connected between them. Charge could be stored this way, allowing scientists and showmen, to use greater amounts of current than they could generate at any one moment. Since the Leyden jar, many different types of capacitors have risen and fallen in prominence in the market. This section will cover the historical introduction of some of the major types.

In 1876 Fitzgerald introduced wax impregnated paper dielectric capacitors with foil electrodes.[5, ch. 11][19] They were typically used for power supply filtering in radios. By the early 1920s, they existed as tubes encapsulated in plain, Bakelite cardboard, with bitman sealing the ends and waxed paper as a dielectric.[5, ch 3] Paper capacitors were upgraded to impregnated paper capacitors, which used paper that was soaked in mineral oil. They were interleaved with metal foil and then rolled to make the capacitor.[29, ch. 8.2.1.1] During WW2, paper capacitors were upgraded with metal-cased tubes with a rubber end.[29, ch. 8.1] These metalized paper capacitors were constructed similarly with the improvement that one side of the paper dielectric was sprayed with metal.[9]

Karol (Charles) Pollak discovered the principle of the electrolytic capacitor in 1886 while he was researching the anodizing of metals, and received a patent for the borax-solution aluminum electrolytic capacitor in 1897. In 1936 Cornell-Dubilier opened a factory to produce aluminum electrolytic capacitors. After the start of WW2, increased funding and effort was applied to the cause of electrolytic capacitors and techniques such as "etching and pre-anodizing" greatly increased their reliability.[11][38]

The science of electrolytic capacitors was extending into what is now know as electrochemical capacitors in 1957 by GE. This technology, also known as electric double layer capacitors, was not commercialized until NEC licensed Standard Oil's patent in 1978.[23] This "supercapacitor" formed the basis of today's EC capacitors. They are characterized by a large capacitance in the range of kilo farads, but with a working voltage of only 2.7V.[23] Some of today's typical applications for EC capacitors are in battery replacement, electric vehicle, and regenerative breaking.

M. Bauer of Germany invented the mica capacitor in 1874. The original mica capacitor was a "clamped" style capacitor, which was used through the 1920s[39] and then replaced by silver mica capacitors.[19] Mica's inherent inertness and reliability allowed for extreme reliability and efficiency in a packaged capacitor.[35] Mica capacitors were heavily used in the radio industry due to their superb stability at RF frequencies and their physical robustness.[28] Capacitors created with mica allowed a comparatively smaller product[5, f. 37-41] which had the ability to survive shock from weapons better than its glass counterpart. Consequently, mica capacitors began to be produced in large quantities during WWI.

In light of mica supply chain problems and the emergence of ceramic capacitors during WW2, mica capacitors fell from prominence to a niche market.[2, Ch 3, Sec II]

The first glass ceramic dielectric capacitor was the Leyden jar. While this early capacitor was used mainly for scientific experiments, commercial glass capacitors

came later. Glass tubular capacitors, known as Moscicki tubes, appeared in 1904 and were used in Marconi's experiments in wireless transmission. They continued to be used in wireless communication until about WWI.[5, p. 102]

Scientists in Germany created the first steatite ceramic capacitor in 1920.[2, Ch 3 Sec II][15] Also known as talc, this ceramic capacitor variant was able to closely match the temperature coefficient of mica.[10] Rutile was later introduced into ceramic capacitor technology. It was able to produce a dielectric constant of 10 times that of steatite, but the two were typically blended to get a better temperature coefficient.

A ceramic composition with barium titanate (BaTiO3) was first discovered in 1941. Barium titanate was quickly found to be able to exhibit a dielectric constant over 1000; an order of magnitude greater the best at this time (rutile - $Ti0_2$). It was not until 1947, that barium titanate appeared in its first commercial devices, phonograph pickups.[14][9][2, Ch 3 Sec III] Barium titanate is still used today in certain types of multi-layer ceramic capacitors.

Thanks to the semiconductor industry, MLCCs grew to dominate the capacitor market and by 1979, AVX alone reached $95 million in MLCC sales.[1] MLCCs are divided up into three classes. Class 1 type MLCCs are known for their extremely good temperature characteristics. COG/NPO types can have 0-30ppm/^{o}C. These capacitors are typically made by combining TiO_2 with additives in order to adjust its temperature characteristics.[25] Additionally, class 1 ceramics have comparatively poor volumetric efficiency, and will tend to come in larger packages than class 2 ceramics of the same capacitance value. Class 2 types typically have worse temperature coefficients than type 1 types, but they have a much higher volumetric efficiency. They are constructed with a ferroelectric base material, typically Barium Titanate.[25]. Class 2 ceramic capacitors are the most common type of ceramics used. Class 3 types have very high capacitance, but a working voltage of several volts.[9][2, Ch 3 Sec VI][8]. They were originally developed as a potential replacement for liquid

electrolytics, but have fallen out of favor due to the advances in Class 2 ceramics to the point where the gap between these two in terms of maximum capacitance is no longer viable[37].

Bell labs invented the first solid tantalum capacitor in 1956. They created it in conjuncture with, and for, transistors.[5, f. 56-64] Tantalum capacitors typically have better characteristics than aluminum electrolytics, but have a lower maximum capacitance and working voltage.[19] Sprague patented the first commercially viable solid tantalum capacitor in 1960. It offered an increased capacitance per unit volume and greater reliability.[30] In the 1970s, Sprague released the first surface mount tantalum capacitor.[32] One of the historical problems with tantalum capacitors has been a limited and volatile supply of tantalum in the world market. As a result of a price spike around 1980, manufacturers created finer grain tantalum powders. This allowed a unit to be made with less overall tantalum, reducing price and package size.[12, ch 3.1] Over time, this volatility has decreased the popularity of tantalum capacitors and has led to a desire for a suitable replacement.

One of the possible alternatives to tantalum capacitors is a titanium based capacitor. Some of the instrumental work in titanium alloys was done in 1939 by Fast[7] and more recently in 1995 by Kobayashi.[18][4] Early work on titanium based capacitors resulted prohibitively high leakage currents[17], but research done by Welsch[36] with titanate (TiO_2) promises a capacitor with a much higher energy and power density when compared with tantalum.[6]

3 Capacitor Parameters

This section will begin by describing some of the practical uses of capacitors and then transition into the various parameters that are used to describe capacitors. Section: 4 will show a method which allows these parameters to be extrapolated from empirical

data.

3.1 Practical Capacitor Uses

The most basic reason for wanting to use a capacitor is that it has the ability to store charge; it has the ability to store electrical energy. Capacitors have the ability to store and release electrical energy quickly, in order to be able to react to the needs of the circuit. This section will describe some of the most common uses for capacitors.

3.1.1 Bypassing

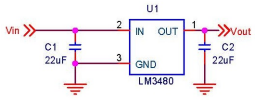

Figure 1: Power Supply Bypassing Circuit

One of the most common uses of capacitors is in power supply bypassing. Capacitors are nearly always attached from a power rail to ground on an supply or IC. They provide a resevior of charge that limits inductive voltage spikes, such as when a digital circuit switches, and limits voltage dips, caused by things such as a current surge when a processor boots. Both LDOs (Figure: 1) and switchers use bypass capacitors on their input and output voltage rails. Input capacitors are divided up into two main catagories, ripple reduction and bulk. Ripple reduction capacitors need to have a low ESR (Section: 3.6) and are meant to decrease the magnitude of any AC signals that ride ontop of the input DC voltage. Bulk capacitors are meant to deliver surge currents. Ouput capacitors have much the same purpose as the input capacitors. The main difference is in the case of switching power supplies. In that application, the output capacitor is a major component in the feedback loop. It contributes to both the transient and stability properties of the switcher.

3.1.2 Analog Filtering

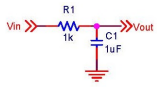

Figure 2: Analog Filtering Circuit

Another use for capacitors is in analog filtering. The low-pass filter in Figure: 2 attenuates frequencies above a cutoff point, set by the values of the resistor and capacitor. Low pass filters are needed in many applications, such as anti-aliasing, clock filtering, and integration.

3.1.3 DC Blocking

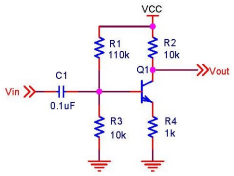

Figure 3: DC Blocking Capacitor

[26][ch 2.08 fig 2.27 pg 77]

Designers often take advantage of capacitors' characteristic of passing AC current while blocking DC current. As in Figure: 3, a capacitor can be used to block a DC offset before an amplifier.

3.1.4 Oscillators

Stable capacitors of a very specific value are required to make a parallel resonant oscillator function properly (Fig: 4). These oscillators provide the clock base for most modern digital circuits using microcontrollers.

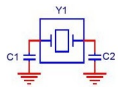

Figure 4: Oscillator Circuit

[26][ch 5.13 fig 5.29 pg 285]

3.2 Capacitance

There is a distinct difference between a capacitor and capacitance. While a capacitor's dominant characteristic is capacitance, it cannot be modeled entirely as such in most practical applications. There are also various inductive and resistive components to a capacitor that are important in various circumstances.

$$C = \frac{Q}{V} \tag{1}$$

Capacitance is the ability to store electrical charge. Equation: (1) shows that capacitance is stored charge that is spread throughout a volume. A device that can store a lot of charge in a small space has a large capacitance. The basic equation for a commercial capacitor is seen in Equation: (2).

$$C = \frac{\epsilon_0 A}{d} \tag{2}$$

When using a capacitor in a single-pole low-pass filter, the cutoff frequency can be determined by Equation: (3). The circuit designer will choose a value for C and R in order to meet the cutoff frequency restraint.

$$f = \frac{1}{2\pi RC} \tag{3}$$

Varying the capacitance used in the filter will move the cutoff frequency and consequently get a different response in the filter. The effect of this can be seen in Figure: 5.

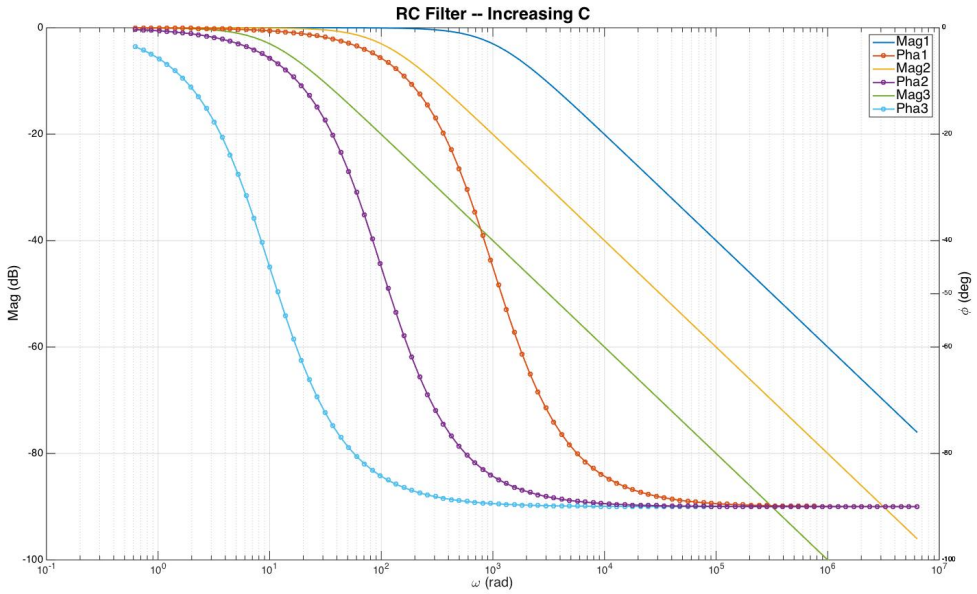

Figure 5: Low Pass Filter – Varying C

3.3 Impedance

The impedance of a capacitor is the "AC resistance" of the device. It determines the AC current that will flow when an ac voltage is applied to the capacitor via Ohm's law (Equation: (4)). An ideal capacitor has only a single capacitive element and its impedance can be described via Equation: (5). The two main things to notice are that the impedance is frequency dependent and it is purely imaginary (reactive).

$$\vec{V} = \vec{I}\vec{Z} \tag{4}$$

$$\vec{Z} = \frac{1}{j\omega C} \tag{5}$$

$$Z = |\vec{Z}| = \frac{1}{\omega C} \tag{6}$$

In most AC applications we look at the magnitude of the impedance. Real capacitors

have a more complicated impedance, but with an ideal capacitor we can simplify the magnitude equation down to Equation (6)

When capacitors are used in bypassing power supplies, the idea is to have a low impedance for common or expected noise frequencies. One may be tempted to choose a large valued capacitor to use for bypassing a wide range of frequencies. This turns out to backfire in practical situations, due to other parasitics in a real capacitor. For any capacitor, the impedance equation is more complicated, and the impedance value will begin to increase with frequency after some point. This will cause the designer to choose several different valued capacitors in parallel when bypassing a power supply or sensitive component. We will see later that the frequency plot of a capacitor will end up being more complicated than the simplified version seen in Figure: 6.

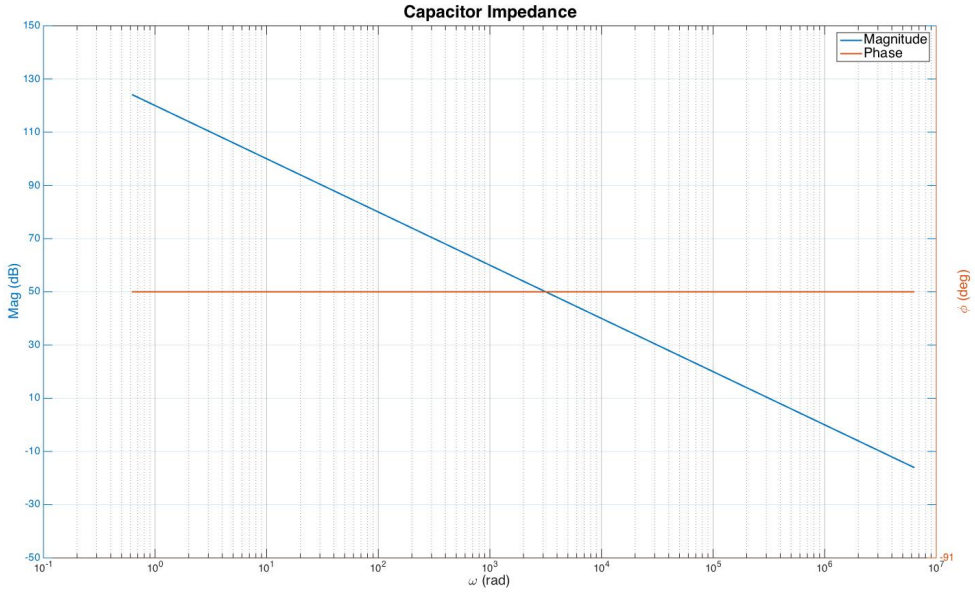

Figure 6: Capacitor Magnitude Over Frequency

3.4 Phase

The phase of a combination of resistive and reactive components can be written as in Equation: (7).

$$\phi = tan^{-1}[\frac{X_c}{R_c}] \tag{7}$$

For an ideal capacitor, having no resistance and only capacitance, the phase angle can be simplified to:

$$\phi = -i = -90^0 \tag{8}$$

The practical implication of this can be seen in the phase response of a low pass filter (Figure: 5). The capacitor introduces a phase lag relative to the input signal's frequency. If you would compare the input and output signals in time, the output's peak would lag behind the input's by the phase amount predicted in the phase response.

3.5 ESL

The Equivalent Series Inductance (ESL) of a capacitor is a lumped estimate of all of the inductive components of a capacitor. It is typically modeled as an inductor in series with the bulk capacitance (See Figure 7).

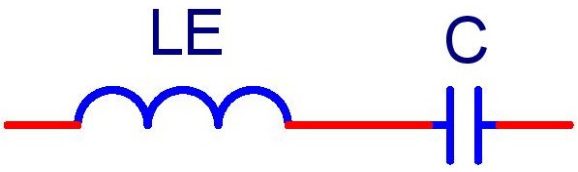

Figure 7: ESL Capacitor Model

Adding ESL to the capacitive model creates a new impedance equation (Equation: (9)). Note that for L<<C, this equation simplifies to Equation: (5) for low

frequencies. In other words, the ideal impedance equation can be reasonably used for low frequencies.

$$\vec{Z}_c = j\frac{\omega^2 LC - 1}{\omega C} \tag{9}$$

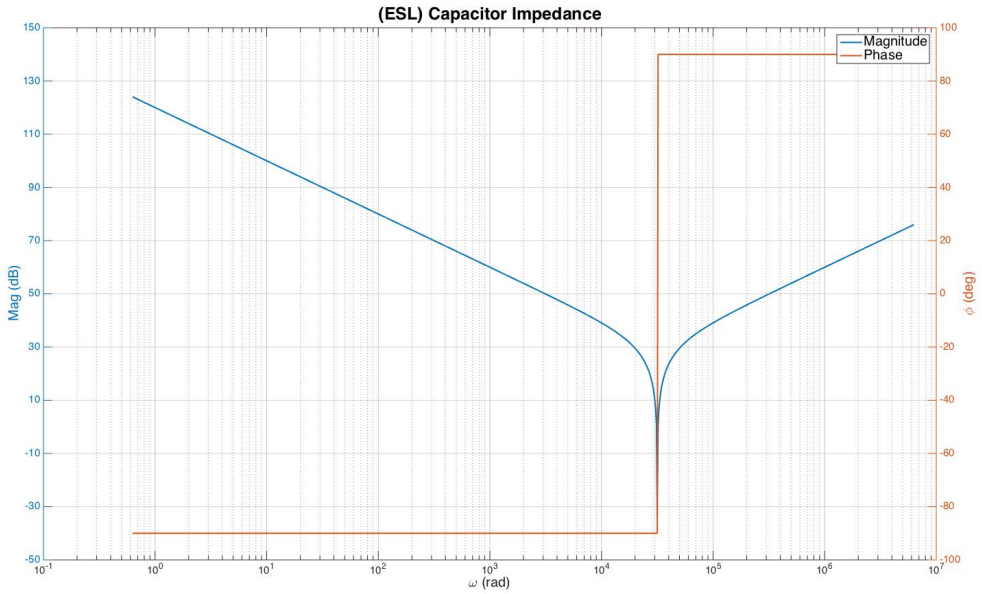

Figure 8: Capacitor Impedance with ESL

Figure: 8 shows a graphical representation of a capacitor's magnitude and phase once ESL is considered. This plot shows that after a resonance point, the impedance of the inductor (which increases with frequency) will begin to dominate. This makes the capacitor ineffective as a bypass element at frequencies higher than its resonance point. Typically, this frequency point and the capacitor's value have an inverse relationship. This is why you will see power supplies and other chips being bypassed by a range of different valued capacitors.

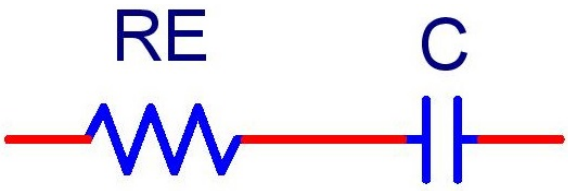

Figure 9: ESR Capacitor Model

3.6 ESR

The Equivalent Series Resistance (ESR) is the practical result of the fact that the materials used to create a capacitor have resistance. In simple cases, this can be approximated by a resistance in series with the main capacitor (See figure: 9).
ESR becomes is important when thinking about DCDC switch mode power supplies. The output ripple voltage of the converter will cause a rripple current to pass through the ESR and dissipate heat as per Equation: (10). It is important to choose a low ESR capacitor in order to reduce failures.

$$P_E = I_{C,RMS}^2 * R_E[21] \tag{10}$$

Another important thing to note about ESR is that even though it is shown as a resistance in simple models, it is not constant across all frequencies. It is a simplification of the resistive and capacitive elements in a capacitor that are dominated by resistance. That said, it is sufficient for a basic understanding of a capacitor's impedance (Equation (11).

$$\vec{Z_c} = \frac{1 + j\omega R_E C + (j\omega)^2 L_E C}{j\omega C} \tag{11}$$

3.7 Resonance Frequency

Once C, ESL, and ESR are included into the capacitor model (Figure: 10, a parameter known as the self-resonant frequency becomes evident. Equation: (11) shows that

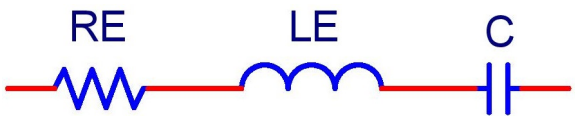

Figure 10: RLC Capacitor Model

when $Z_{ESL} == Z_C$, the capacitor is at its resonance point. At this frequency, the capacitor's impedance is determined solely by the ESR at that frequency. This frequency can be calculated by Equation: (12).

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

3.8 Dissipation Factor

The dissipation factor, otherwise known as the loss-tangent, is a measure of the energy stored to the energy dissipated per cycle. It is a measurement of the efficiency of the capacitor. The DF can be quantified through Equation: (13).

$$D = \frac{R_E}{X_C} \tag{13}$$

The loss tangent can be seen in Figure: 11. The greater the angle, the more efficient the capacitor will be.

3.9 Quality Factor

$$Q = \frac{1}{D} \tag{14}$$

The Quality Factor, Q, of a capacitor is found by taking the reciprocal of the dissipation factor, Equation: (14). It is defined as the ratio of the energy stored to the energy dissipated per cycle.

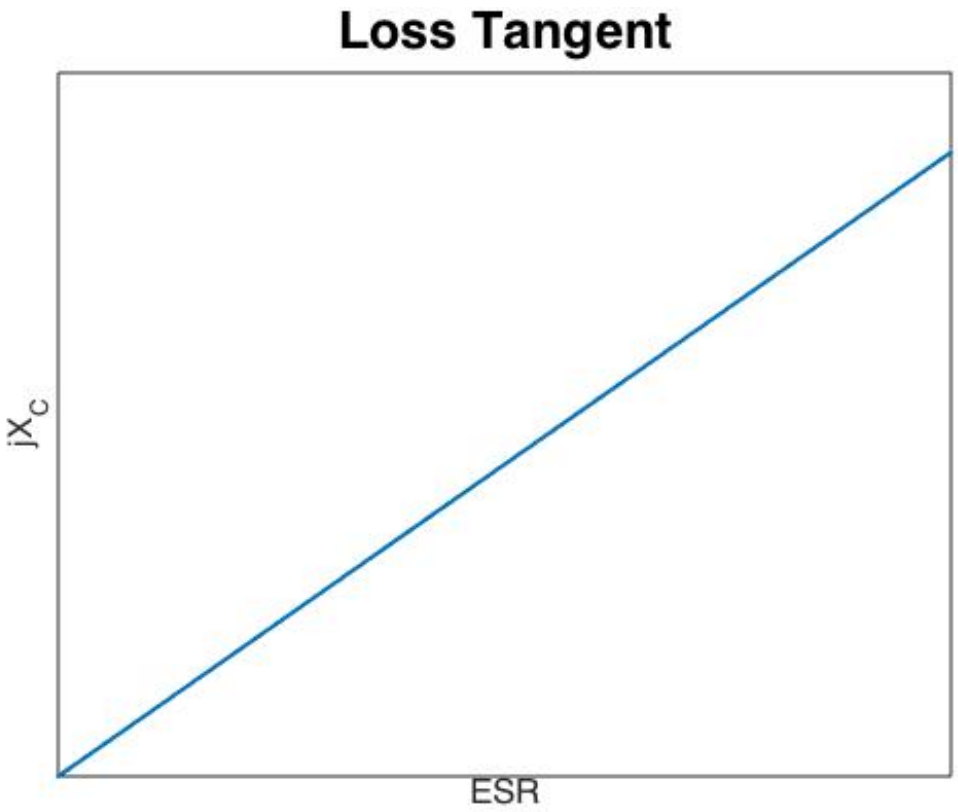

Figure 11: Loss Tangent

3.10 Leakage Resistance

Every capacitor will have some DC leakage resistance associated with it. This resistance affects the capacitor's ability to store charge. A high leakage resistance results in a capacitor with low self-discharge. This characteristic is especially important in sample and hold circuits.

3.11 Dielectric Absorption

Dielectric Absorption, DA, in a capacitor is a characteristic which describes the unit's ability to "regenerate" a voltage after being shorted to ground for a brief time.

As seen in Figure: 12, a capacitor can be modeled with multiple RC elements in

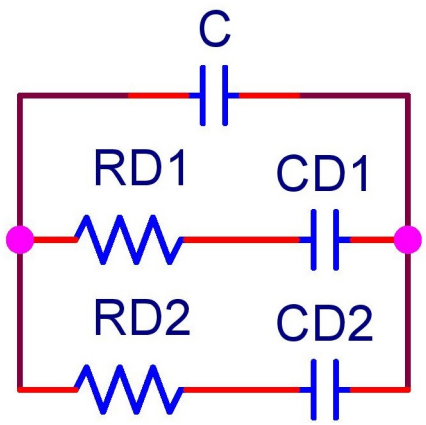

Figure 12: Dielectric Absorption

parallel with the bulk capacitance. When the main capacitor is shorted to ground for a short time, and then released, the other capacitors are not gauranteed to have been fullly discharged. After several minutes, they can recharge the main capacitance to a significant portion of its original charge. This is why large valued electrolytic capacitors get shipped with a resistor across their terminals.

4 Capacitor Modeling

Many designers have a need to simulate the response of the individual components in their systems to impulse and steady state inputs. When dealing with passive electronic components, the device is typically modeled as a combination of various resistors, capacitors, and inductors. The model chosen is often due to either the required accuracy or a specific characteristic of the component that needs to be modeled. When characterizing a new component, the complex frequency response is recorded and then fit to a model. In this section, a progression of regression techniques will be evaluated for their ability to fit the measured frequency response of a capacitor to a polynomial equation. Then the accuracy of various capacitor models will be explored in regards to the fit. All models will attempt to fit the data

from Figure: 13.

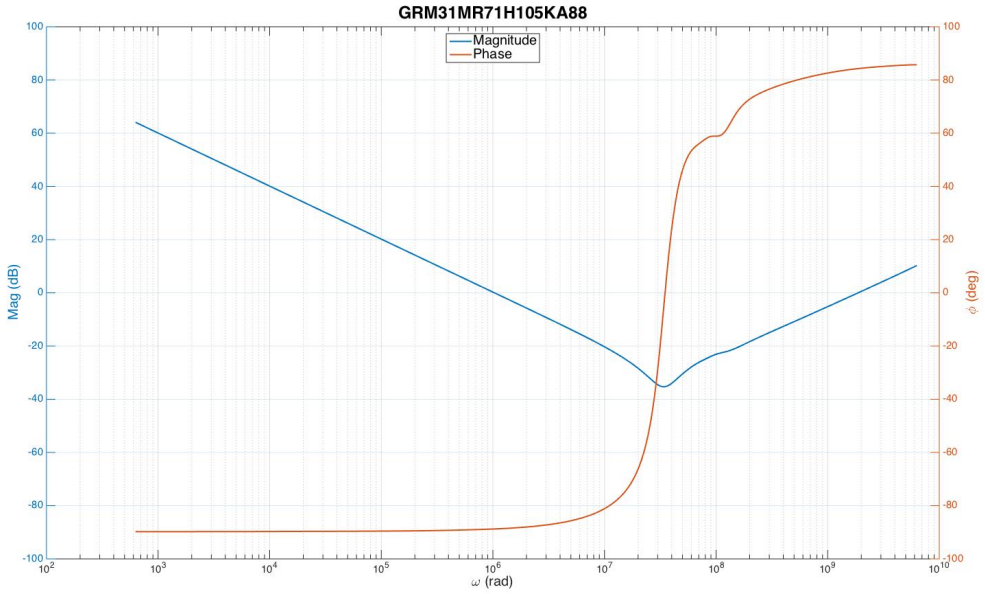

Figure 13: GRM31MR71H105KA88 Capacitor Data

4.1 Regression Analysis

4.1.1 Basic LSE

At its core, regression analysis is an optimization problem whose purpose is to fit the equation of a line to a data set. A commonly use regression analysis technique is called the Least Squares Estimate (LSE). It attempts to find a model which minimizes the squared error between an empirical set of data and itself.

The first step in applying an LSE is to choose the form of the equation that best represents the data. The equation of a line, Equation: (15), is chosen when only a simple linear fit is needed. Then the squared error equation is generated, as in

Equations: (16) & (17).

$$y = a_0 + a_1 x \tag{15}$$

$$E^2 = \sum_{i=1}^{n} (y_i - y)^2 \tag{16}$$

$$E^2 = \sum_{i=1}^{n} (y_i - (a_0 + a_1 x_i))^2 \tag{17}$$

In order to minimize the squared error over the data set, one needs to take the partial derivate of Equation: (17) with respect to each of the unknown parameters, the coefficients, separately. While a_0 and a_1 will be constants in the final equation, they are treated as variables here until they are known. Conversely, all x_i values are treated as constants. This results in Equations: (18) & (19).

$$\frac{\partial E^2}{\partial a_0} = 0 = \sum_{i=1}^{n} (-2y_i + 2a_0 + 2a_1 x_i) \tag{18}$$

$$\frac{\partial E^2}{\partial a_1} = 0 = \sum_{i=1}^{n} (-2y_i x_i + 2a_0 x_i + 2a_1 x_i^2) \tag{19}$$

Up to this point most LSE analyzes follow the same basic path. But the rest of the steps depend upon the complexity of the model and solution techniques. The following steps in the basic LSE use transformations and substitutions to solve for the unknown variables. In our case, we can use Equation: (20) to remove the summation terms from the equation.

$$\sum_{i=1}^{n} y_i = \bar{y} n \tag{20}$$

This results in Equations: (21) & (22) with solutions shown in Equations: (23) & (24). The empirical data is then used to find the values of a_0 and a_1. At this point,

the line can be used to estimate new points on the plot or to compare against other data sets.

$$0 = \bar{y} - (a_0 + 2a_1\bar{x}) \tag{21}$$

$$0 = \bar{xy} - (a_0\bar{x} + 2a_1\bar{x^2}) \tag{22}$$

$$a_0 = \bar{y} - a_1\bar{x} \tag{23}$$

$$a_1 = \frac{\bar{xy} - \bar{x}\bar{y}}{\bar{x^2} - \bar{x}^2} \tag{24}$$

An example of this type of fit can be seen in Figure: 14.

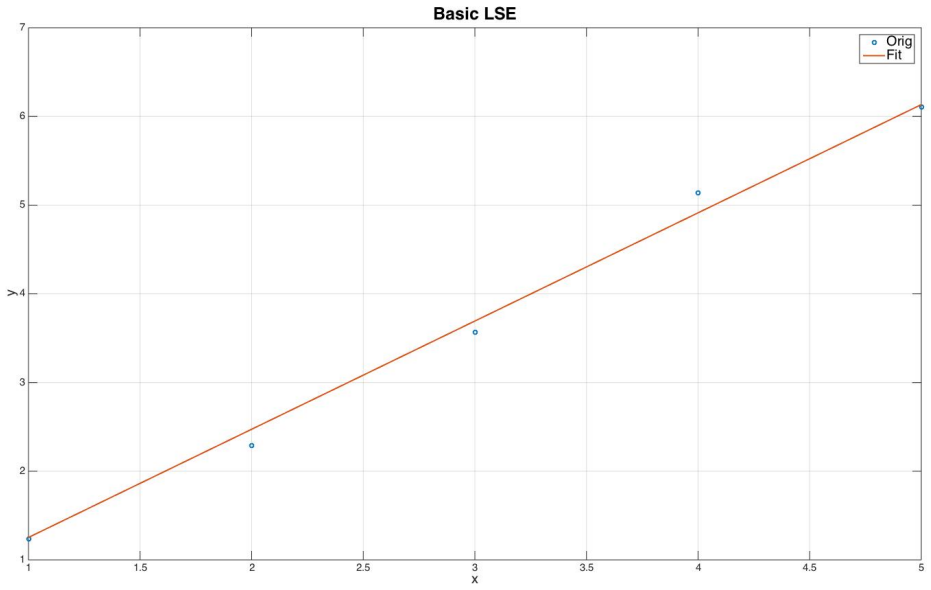

Figure 14: Basic LSE

4.1.2 Levy's Technique - Complex Curve Fitting

While the basic LSE technique is sufficient for many circumstances, it is not directly applicable in situations where one needs to fit a complex line, such as a transfer function. Levy [20] shows an extension of the simple LSE example that is valid for a generic polynomial transfer function. This method is important because it not only allows for a complex-valued transfer functions, but it also prevents the necessity of needing to rederive the system of equations for each new model.

$$G(s) = \frac{A_0 + A_1 s + A_2 s^2 + ... + A_n s^n}{B_0 + B_1 s + B_2 s^2 + ... + B_m s^m} \text{ [20][Eq. 3]} \tag{25}$$

Using Equation: (25) as the generic model, Levy shows that you can use Equations: (26), (27), (28), & (29) to simplify the series of partial derivatives into a single matrix multiplication equation shown in (30), (31), (32), & (33).

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h \text{ [20][Eq. 15]} \tag{26}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k \text{ [20][Eq. 16]} \tag{27}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k \text{ [20][Eq. 17]} \tag{28}$$

$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) \text{ [20][Eq. 18]} \tag{29}$$

$$MN = C \text{ [20][Eq. 20]} \tag{30}$$

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & \lambda_4 & \cdots & T_1 & S_2 & -T_3 & -S_4 & T_5 & \cdots \\ 0 & \lambda_2 & 0 & -\lambda_4 & 0 & \cdots & -S_2 & T_3 & S_4 & -T_5 & -S_6 & \cdots \\ \lambda_2 & 0 & -\lambda_4 & 0 & \lambda_6 & \cdots & T_3 & S_4 & -T_5 & -S_6 & T_7 & \cdots \\ 0 & \lambda_4 & 0 & -\lambda_6 & 0 & \cdots & -S_4 & T_5 & S_6 & -T_7 & -S_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots & \vdots & \vdots & \\ T_1 & -S_2 & -T_3 & S_4 & T_5 & \cdots & U_2 & 0 & -U_4 & 0 & U_6 & \cdots \\ S_2 & T_3 & -S_4 & -T_5 & S_6 & \cdots & 0 & U_4 & 0 & -U_6 & 0 & \cdots \\ T_3 & -S_4 & -T_5 & S_6 & T_7 & \cdots & U_4 & 0 & -U_6 & 0 & U_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \end{bmatrix} \quad [20][Eq.\ 21a] \tag{31}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \\ \vdots \\ B_1 \\ B_2 \\ B_3 \\ \vdots \end{bmatrix} \quad [20][Eq.\ 21b] \tag{32}$$

$$C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ T_3 \\ \vdots \\ 0 \\ U_2 \\ 0 \\ \vdots \end{bmatrix} \quad [20][Eq.\ 21c] \tag{33}$$

Levy's technique works well for applications where there is a small dynamic frequency range and a small number of coefficients, but there a several problems with it. The first problem is that for models with a wide bandwidth, the solution to Equation: (30), involves an ill-conditioned matrix. This means that the ratio of the "largest to smallest singular value in the singular value decomposition of a matrix is ... >= log^{-1}(input precision). In other words, it estimates a worse case loss of precision."

The second problem is that this technique favors the magnitude plot at the high frequency range.

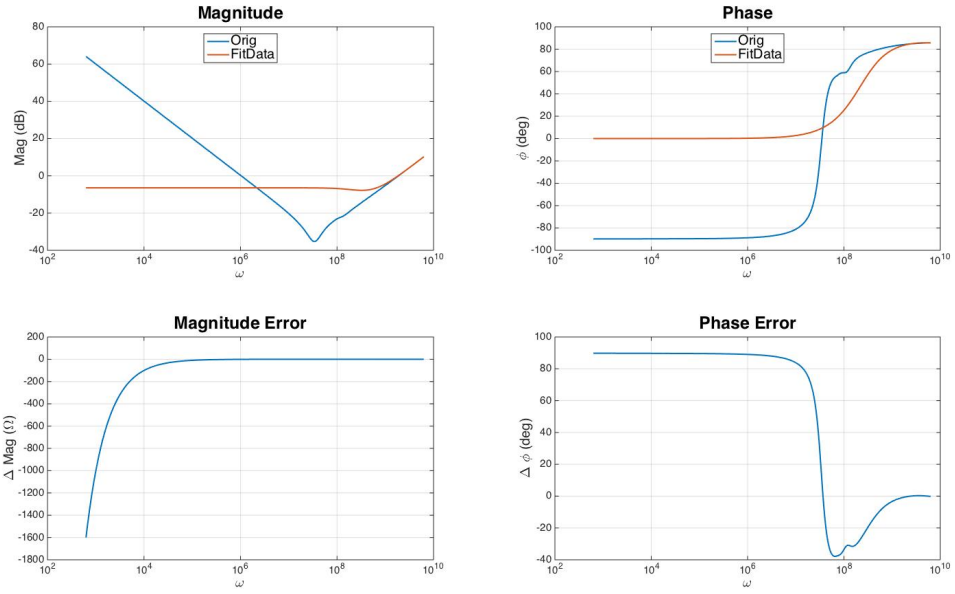

Figure 15: Levy's Technique

4.1.3 Weighted LSE

One improvement that can be made upon Levy's method is to iterate with a frequency dependent weighting function until the error term is minimized[31]. By multiplying Levy's error function by the weighting term in Equation: (34), we get Equation: (35), which can be minimized to obtain a new system of equations. The L subscript stands for the current iteration, while $L-1$ stands for the previous iteration.

$$W_{kL} = \frac{1}{|Q(jw_k)_{L-1}|^2} \text{ [31]} \tag{34}$$

$$E = \sum_{k=1}^{n} |\epsilon_k'|^2 W_{kL} \text{ [31][Eq. 7]} \tag{35}$$

Equations (30), (31), (32), & (33) are the same, with Equations (26), (27), (28), & (29) being replaced with Equations: (36), (37), (38), & (39).

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h W_{kL} \text{ [31][Eq. 9]} \tag{36}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k W_{kL} \text{ [31][Eq. 10]} \tag{37}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k W_{kL} \text{ [31][Eq. 11]} \tag{38}$$

$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) W_{kL} \text{ [31][Eq. 12]} \tag{39}$$

This particular iteration method is not guaranteed to converge. Figure: 16 shows that, for this data set, the squared error of the magnitude and phase do not converge after a particular number of iterations. Furthermore, they do not reach their minimums at the same iteration. In order to select the desired iteration, the magnitude and phase squared plots are normalized as in Equation: (40). The index of the minimum of Figure: 16 is selected as the best fit.

$$n = min(Emag/max(eMag) + Epha/max(ePha)) \tag{40}$$

Figure: 18 shows that this method can result in a much improved result over the Levy's original method, as seen in Figure: 15.

4.2 Modeling

This section will investigate several of the most common capacitor models. It will show how to fit them to a data set with Levy's method described in Section: 4.1, and will describe their effectiveness and limitations in doing so.

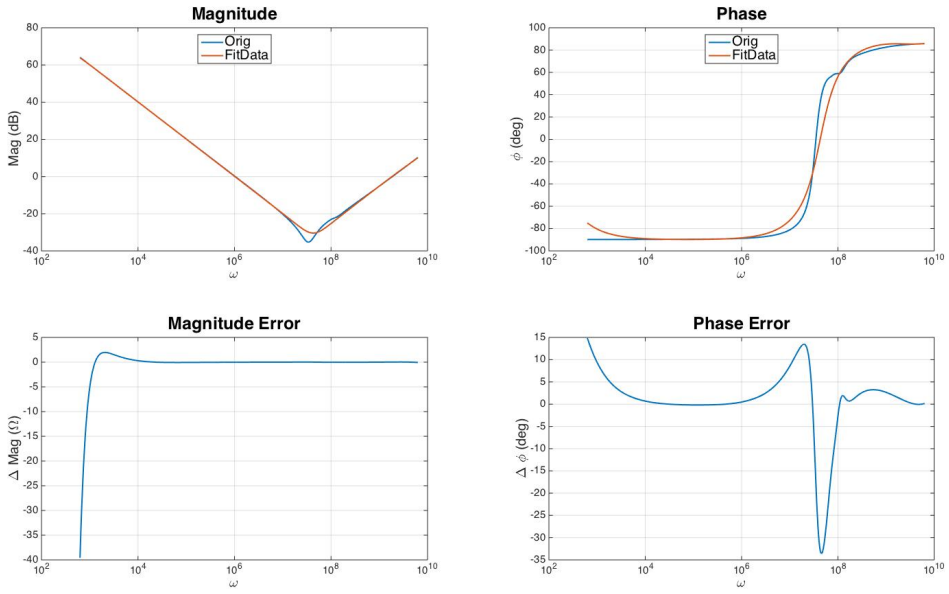

Figure 16: LSE + Iteration – Magnitude and Phase Error

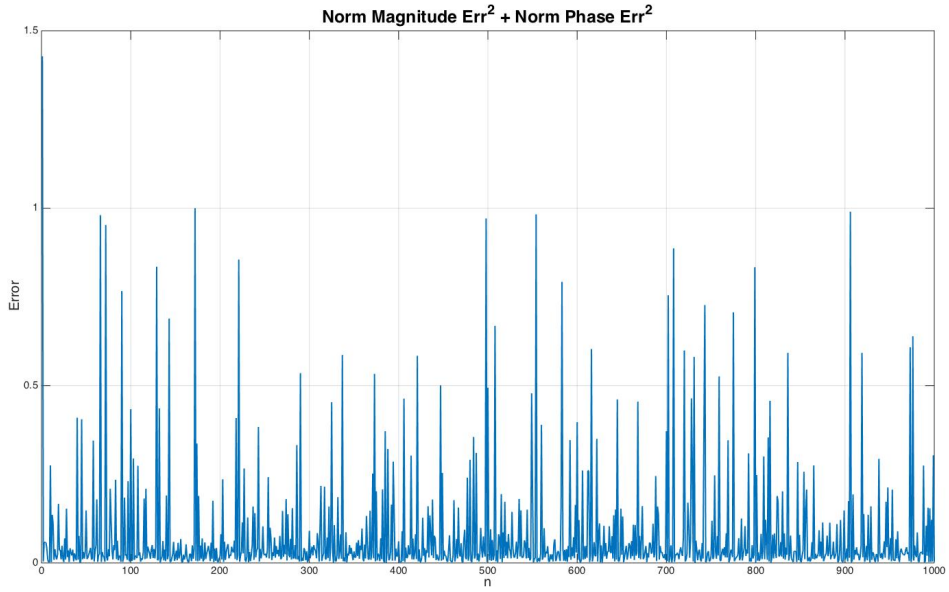

Figure 17: LSE + Iteration – Combined Error

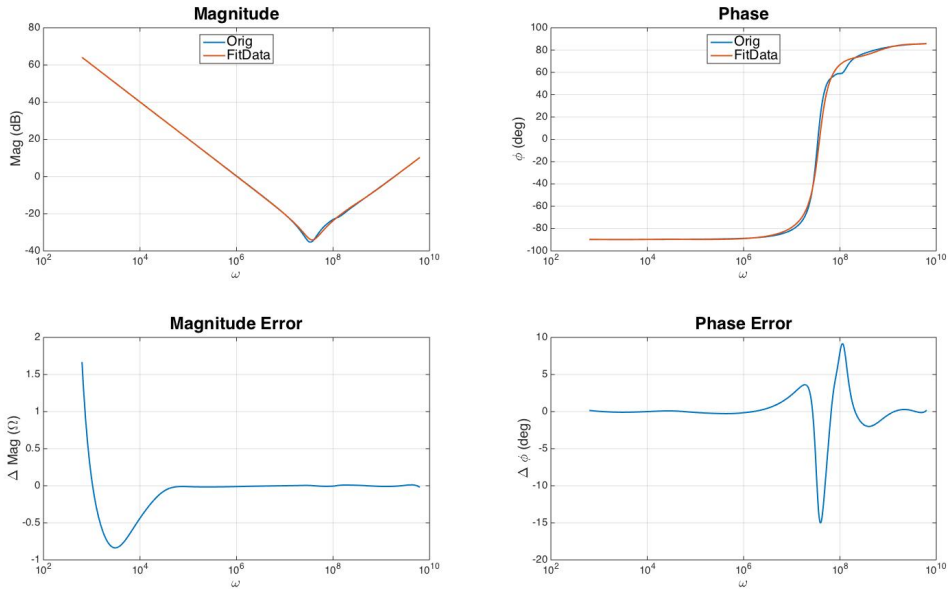

Figure 18: LSE + Iteration

4.2.1 6 Term Model

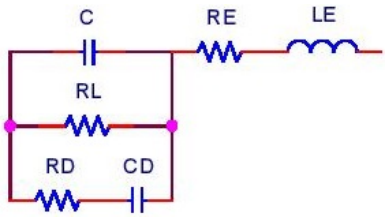

Figure 19: 6 Term Model

The model shown in Figure: 19 shows several of the most important parameters for a capacitor. It's impedance, shown in Equation: (41), can be used as the basis for a regression analysis.

$$\begin{aligned}\bar{Z}(s) = &\frac{(R_E + R_L) + (L_E + C_D R_D R_E + C_D R_D R_L + C R_E R_L + C_D R_E R_L)s}{1 + (C_D R_D + C R_L + C_D R_L)s + C C_D R_D R_L s^2} \\ &+ \frac{(C_D L_E R_D + C L_E R_L + C_D L_E R_L + C C_D R_D R_E R_L)s^2 + C C_D L_E R_D R_L s^3}{1 + (C_D R_D + C R_L + C_D R_L)s + C C_D R_D R_L s^2}\end{aligned} \tag{41}$$

$$\bar{Z}(s) = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3}{b_0 + b_1 s + b_2 s^2} \tag{42}$$

For this model, Equations: (31), (32), & (33) simplify down to Equations: (43), (44), & (45).

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & T_1 & S_2 \\ 0 & \lambda_2 & 0 & -\lambda_4 & -S_2 & T_3 \\ \lambda_2 & 0 & -\lambda_4 & 0 & T_3 & S_4 \\ 0 & \lambda_4 & 0 & -\lambda_6 & -S_4 & T_5 \\ T_1 & -S_2 & -T_3 & S_4 & U_2 & 0 \\ S_2 & T_3 & -S_4 & -T_5 & 0 & U_4 \end{bmatrix} \tag{43}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \\ B_1 \\ B_2 \end{bmatrix} \tag{44}$$

$$C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ T_3 \\ 0 \\ U_2 \end{bmatrix} \tag{45}$$

Using this model, the regression analysis output described in Section: 4.1.3 can be seen in Figure: 20. The fit tracks the original data well, except for low frequencies and near resonance.

Equations: (53) shows solution for the polynomial coefficients. Using Equations: (42) and (42), the circuit parameters can be found through Equations: (46)-(52), with the solution as seen in Equations: (53) & (54). Even though the polynomial coefficients gave an acceptable fit to the data, it resulted in unacceptable circuit parameters. Since C and R_D are negative, this model is not physically realizable.

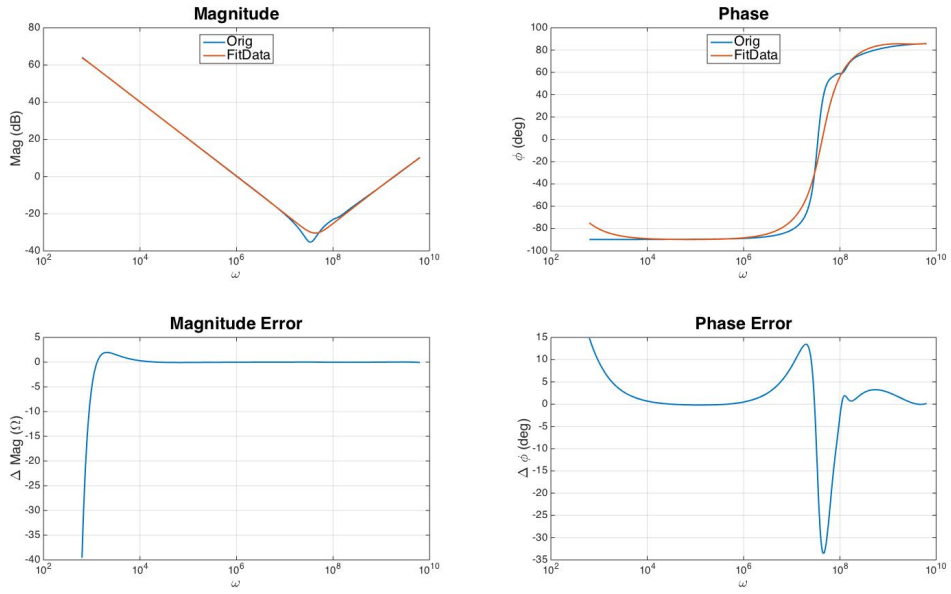

Figure 20: 6 Term Model: Bad Initilization

$$a_0 = R_E + R_L \tag{46}$$

$$a_1 = L_E + C_D R_D R_E + C_D R_D R_L + C R_E R_L + C_D R_E R_L \tag{47}$$

$$a_2 = C_D L_E R_D + C L_E R_L + C_D L_E R_L + C C_D R_D R_E R_L \tag{48}$$

$$a_3 = C C_D L_E R_D R_L \tag{49}$$

$$b_0 = 1 \tag{50}$$

$$b_1 = C_D R_D + C R_L + C_D R_L \tag{51}$$

$$b_2 = C C_D R_D R_L \tag{52}$$

$$\begin{aligned} a_0 &= 5.9991E^{+03} \\ a_1 &= 1.7934E^{-04} \\ a_2 &= 3.3158E^{-12} \\ a_3 &= 6.8295E^{-22} \\ b_0 &= 1.0000 \\ b_1 &= 5.9057E^{-03} \\ b_2 &= 1.4067E^{-12} \end{aligned} \tag{53}$$

$$
\begin{aligned}
C &= -8.2563E^{-10} \\
R_E &= 3.1886E^{-01} \\
L_E &= 4.8551E^{-10} \\
R_L &= 4.8551E^{-10} \\
C_D &= 9.8536E^{-07} \\
R_D &= -2.8824E^{-01}
\end{aligned}
\tag{54}
$$

The problem comes with the author's [31] suggestion that the initial guess for $Q(jw_k) == 1$. While an initial guess is required to calculate the weighting function during the first iteration, this particular choice causes the problem seen in Equations: (55) & (56). They show that this initial condition does not yield a rational solution for the circuit parameters.

$$
\begin{aligned}
a_0 &= 1 \\
a_1 &= 1 \\
a_2 &= 1 \\
a_3 &= 1 \\
b_0 &= 1 \\
b_1 &= 0 \\
b_2 &= 0
\end{aligned}
\tag{55}
$$

$$
\begin{aligned}
C &= INF \\
R_E &= INF \\
L_E &= INF \\
R_L &= IND \\
C_D &= IND \\
R_D &= IND
\end{aligned}
\tag{56}
$$

If we instead start with the rational set of circuit parameters seen in Equation: (58), the starting coefficients are as seen in Equation: (57).

$$
\begin{aligned}
a_0 &= 2 \\
a_1 &= 5 \\
a_2 &= 4 \\
a_3 &= 1 \\
b_0 &= 1 \\
b_1 &= 3 \\
b_2 &= 1
\end{aligned}
\tag{57}
$$

$$
\begin{aligned}
C &= 1 \\
R_E &= 1 \\
L_E &= 1 \\
R_L &= 1 \\
C_D &= 1 \\
R_D &= 1
\end{aligned}
\tag{58}
$$

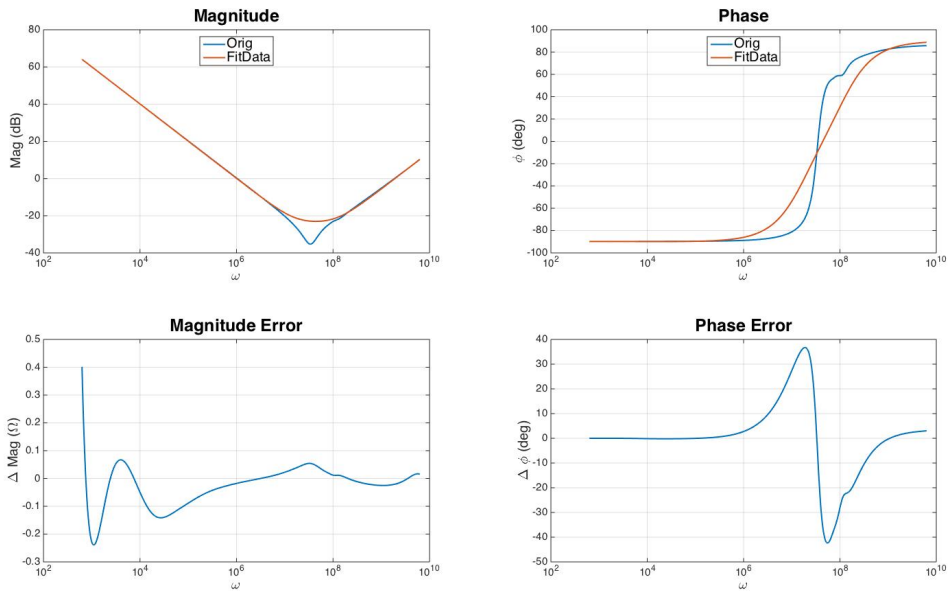

Figure 21: 6 Term Model: Good Initilization

Figure: 21 shows a good fit across the frequency spectrum for both magnitude and phase. The model does deviate at resonance, but that is unsurprising, as the number of parameters in the model is fairly low.

Input Scale	0 to +10V for 0 to 5kV
Input Impedance	1 MΩ
Accuracy	±0.2% of full scale
Update Rate	15 Hz
Output Slew Rate	<0.3s for 0 to full scale (full load)

Table 1: SRS PS350 External Voltage Control Characteristics

[34] [33]

5 Measurement Circuitry

This section describes the schematic design used to meet the goals set out in the Abstract (Section: 0.2). The schematic can be found in the Appendix section: 7.

5.1 DC Bias

A DC bias is needed to conduct AC measurements as well as to allow for measuring discharge curves of the DUT. In order to determine the effect of the DC bias on the DUT, it is necessary to control that quantity. This section describes the circuitry (Schematic Page: 3) used to provide a means to programatically control the DC bias from 0 to 500V. The supply used is a Stanford Research Supply (SRS) PS350. It accepts a DC control signal, which is supplied by the circuit through a DAC. If different supply characteristics are needed, it can be swapped out with any supply. A generic RS232 bi-directional port (Schematic Page: 10) is provide to control the supply in this situation.

The SRS Supply's specifications can be seen in Table: 1. The output of the PS350 can either be set manually or with a 0-10V control voltage. This circuitry will take advantage of this analog input at a gain of 500.

The analog control uses an AD7391, 14-bit DAC with an internally generated

reference. It is controlled via a SPI bus connected to a microcontroller. The update rate of this device is not important to this application because it will be set infrequently and only when the system is not actively collecting data. The output signal of the DAC is fed into an op amp which acts as a voltage limiter for safety. This clamps the control signal at 1.5V and the PS350's output at 750V.These numbers are theoretical and will degrade from ideal due to the SRS's response to the control signal, the noise levels in the system, and various other factors, such as temperature.
The DAC has a 2.5V internal reference. With 14 bits, that gives the control signal an ideal resolution of $150\mu V$ and the PS350 an output resolution of $76mV$.

5.2 Current Measurement

Each of the tests utilize the low-side current measurement circuit. The AC measurement tests provide a known voltage across the DUT and then the current is used to construct the impedance. The discharge tests use the current measurement circuit to capture the current through the DUT over time as its energy drains.

Refdes	Value	Range	
R5	5	Hi	1A - 1mA
R6	5k	Med	1mA - 1uA
R7	5M	Low	1uA - 1nA

Table 2: Current Measurement Ranges

The current measurement circuit utilizes a transimpedance amplifier designed from the reference circuit in [6]. It utilizes 3 switched, feedback stages to measure 9 decades of current (See Table: 2). The circuit creates a virtual ground at the negative terminal of the DUT and then uses one of the feedback paths to create a voltage for a digitizer. Using a low-side current measurement circuit is beneficial in this circumstance because it allows low voltage circuitry to condition and measure a signal without needing to

see the high DC voltage on the positive terminal of the DUT. The output voltage is calculated by Equation: (59).

$$Vo = I * R_f \tag{59}$$

*Add transistor in increase the Op Amp's current drive capability. *Change capacitors in feedback loop. *Add Sallen-key filter to output *Explain difference in two buffering stages

The output will be buffered and then filtered and digitized dependent of the specific test of interest.

5.3 Charge

This section of the circuitry is meant as a preparation stage for the other tests. It operates by setting the current measurement to High, closing the Charging Relay (LS4), and then ramping the DC Bias voltage with the high current measurement stage open. LS4 can be opened or left closed, dependent on the needs of the test.

5.4 Discharge Circuitry

The discharge circuitry provides a means to determine the bulk capacitance value of the DUT from the RC time constant. Once the DUT is charged to the desired voltage, the charging relay will open and then the high-current discharge relay will close. The current through the DUT will be measured as it decays.

There are 3 switched discharge stages that allow for the decay rate to be regulated. Each stage allows for a range of voltages and capacitances needed to stay within safety and operational constraints. As seen in Figure: 22, there are two constraints on both the voltage and capacitance. The lowest valued resistor constrains the maximum voltage when using that stage due to its power rating. The other two stages are

constrained by the overall safety limit of 500VDC. The minimum capacitance for each stage is determined by setting a requirement of at least 100 ADC samples per time constant with a sampling rate of $250KSPS$. The maximum capacitance for each stage is determined by setting a maximum time constant.

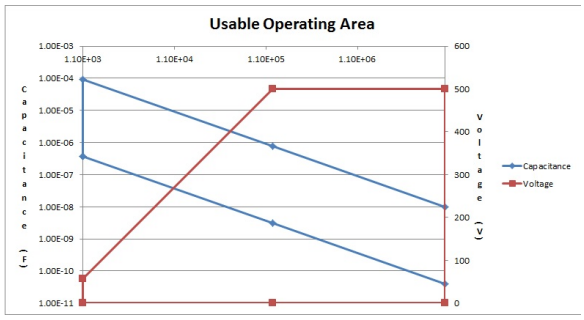

Figure 22: Operating Area

5.5 Magnitude

The magnitude section takes the sinusoidal current measurement and creates a DC output by with a dual difference amplifier package. This technique as seen in [24] provides a method to measure the RMS value of the AC current through the DUT. The first difference amplifier is configured as a voltage follower. Since this circuit operates only from a single power rail, it passes the positive going portions of the waveform and clamps to ground for th negative going portions of the waveform. The second difference amplifier operates in different modes, based upon the output of the first differential amplifier. During the negative going portions of the waveform, its positive terminal is held at ground, and it operates as a unity gain, inverting amplifier. This rectifies the input signal to the output. During the positive going portions of the waveform, positive input terminal is held at the value of the input terminal. This forces the second difference amplifier to act as a voltage follower. In this manner, the circuit performs a full-wave rectification on the signal, which is then filtered and fed

to the ADC for digitization.

5.6 Phase

This section explains the circuitry used to measure the phase difference between the input voltage and the output current. This measurement, combined with the magnitude measurement, will allow for a complete impedance measurement at each frequency step of a test. The comparator circuit is configured as a sine to square wave converter. The two square wave signals will be fed directly into a timer input of the MCU. The MCU will measure the time between the two signals to determine their phase difference.

5.7 Communications

This section will describe the circuitry used to communicate to off-board processors.

5.7.1 USB

The USB section is used to communicate with a PC for data logging and data post processing. This circuitry centers around a FTDI FT232H serial to USB chip. It allows seamless USB communication to a PC's com port with the MCU only needing to use a UART port. This significantly lowers the complexity of the communication bus, as the MCU is not responsible for running the USB stack.

5.7.2 RS-232

The board also has two, bidirectional RS-232 ports. They are able to be used for general purposes, but will most often be used for communicating with a sine-wave generator and an alternate DC Bias supply.

6 Conclusion

This section will summarize the methodologies used to solve the stated problem.

7 Future Work

This section will describe the future work needed to be accomplished in order to complete and further the stated goals of this thesis. It will mostly focus on the practical circuitry implementation and other aspects needed to make it a viable tool.

Appendix

TABLE OF CONTENTS

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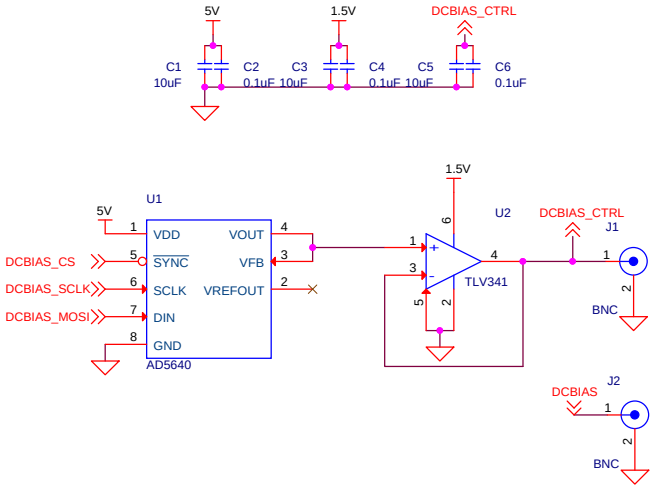

DC BIAS CONTROL

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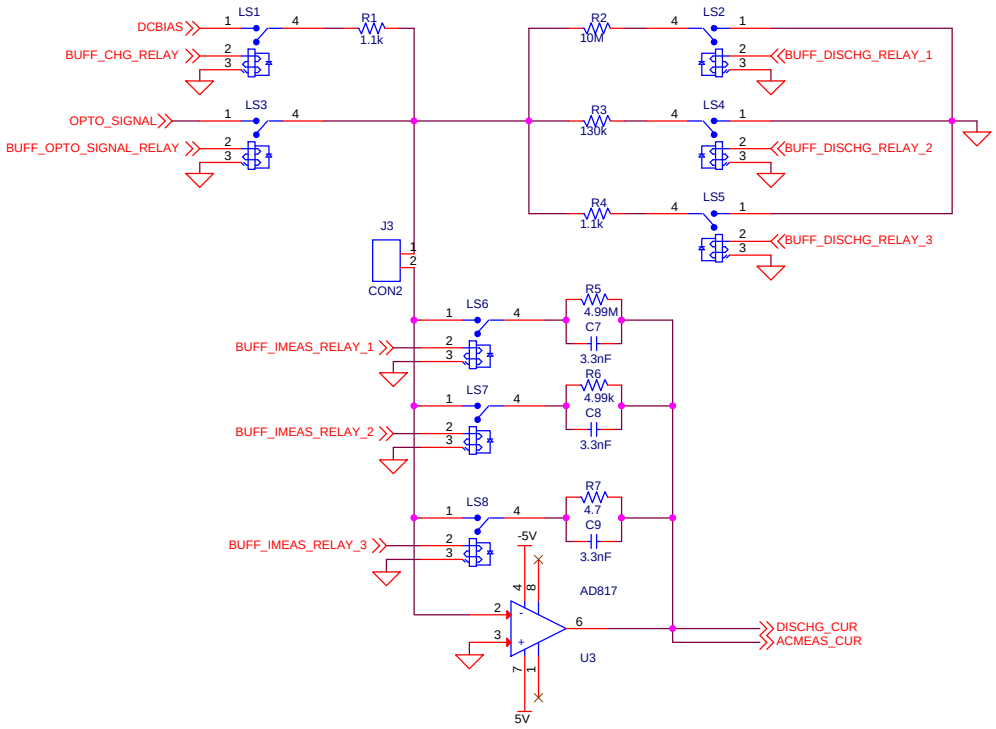

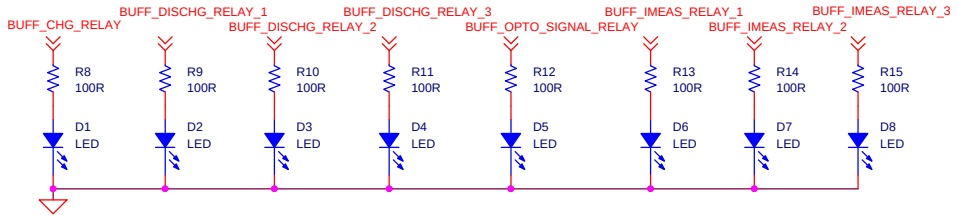

DISCHARGE CIRCUITRY

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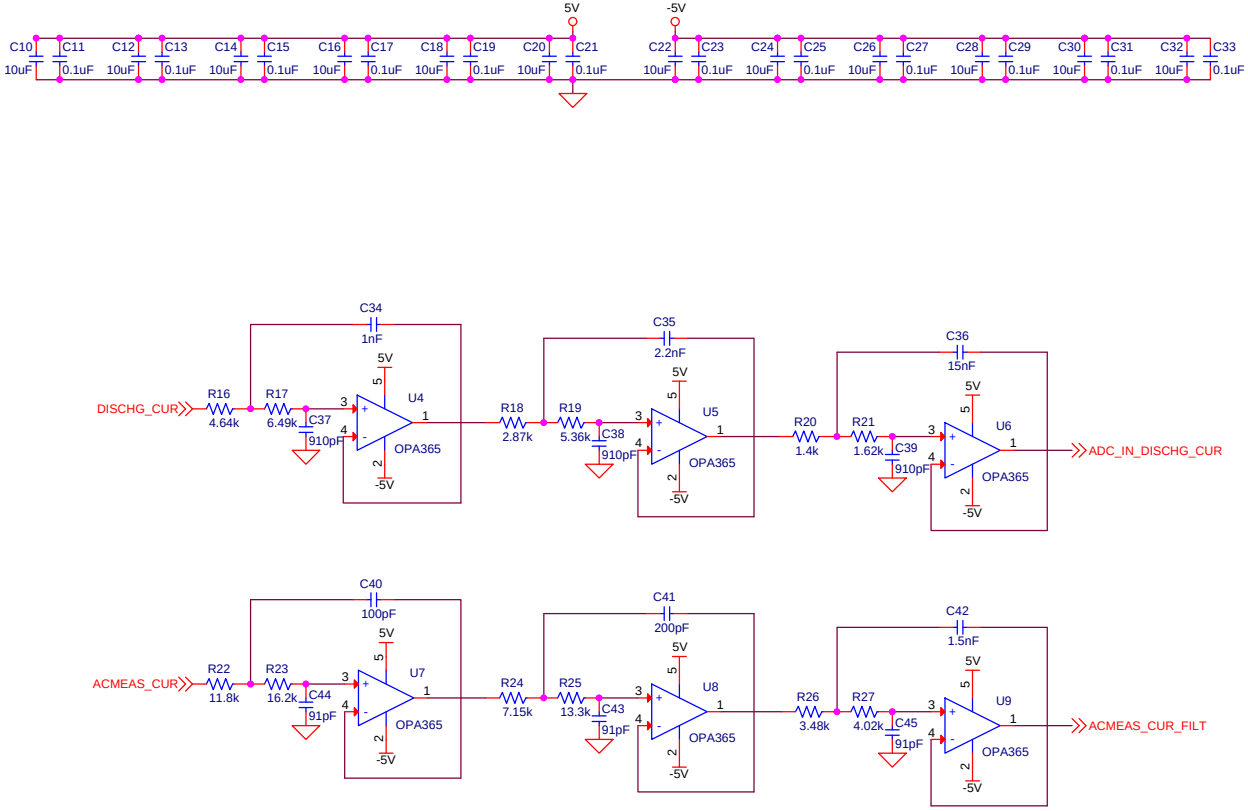

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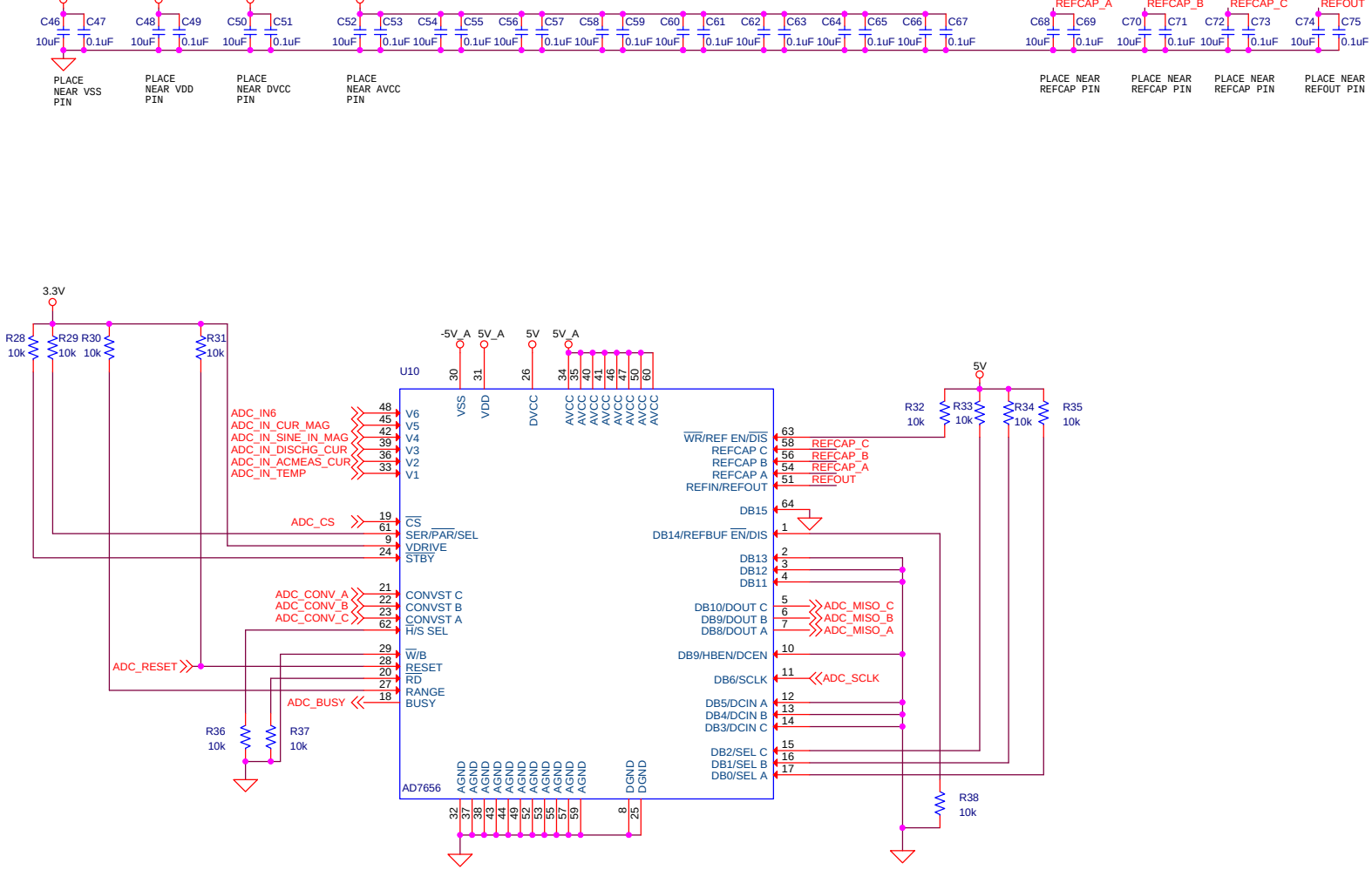

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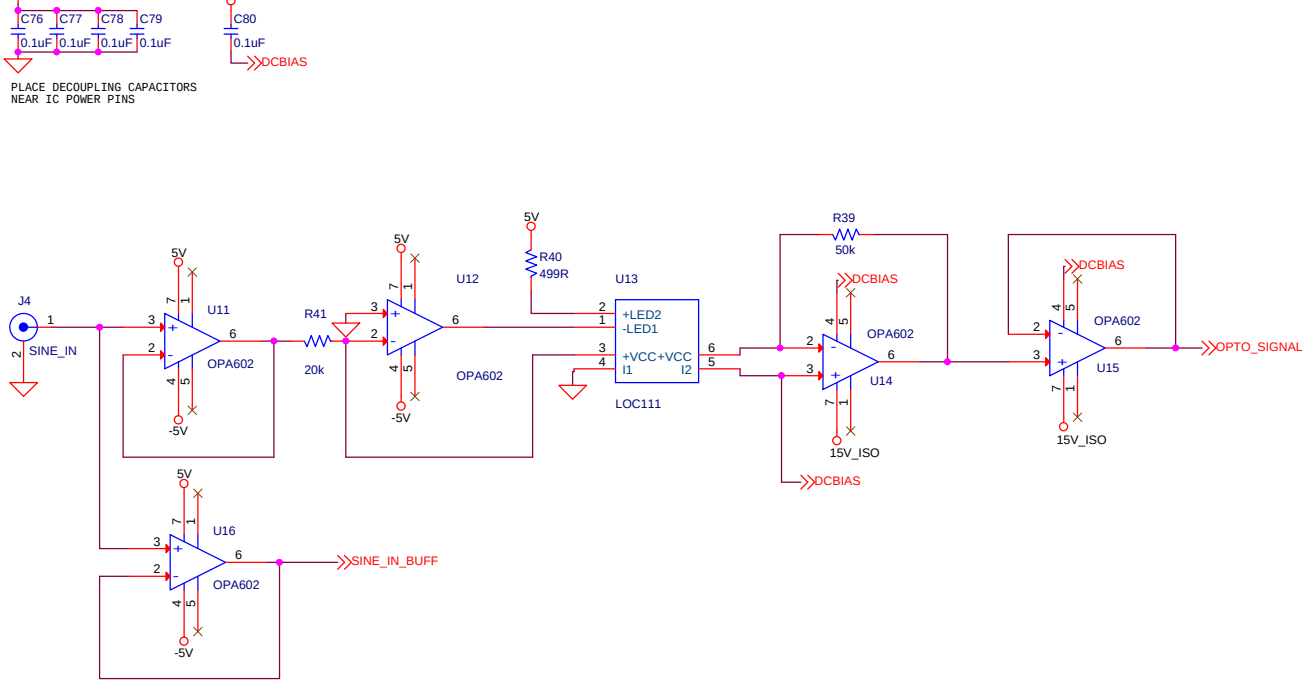

OPTOCOUPLER

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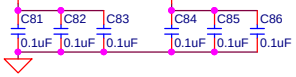
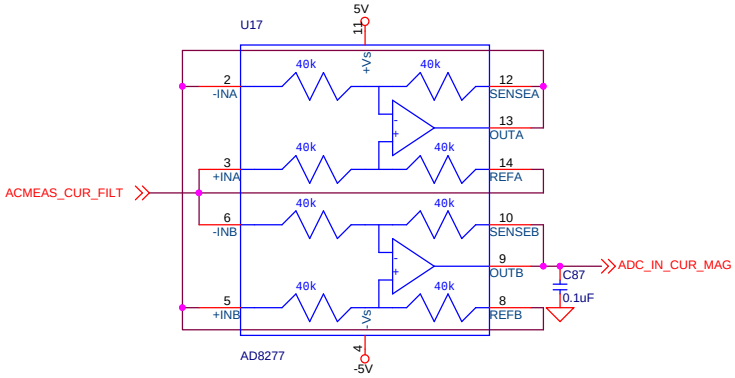
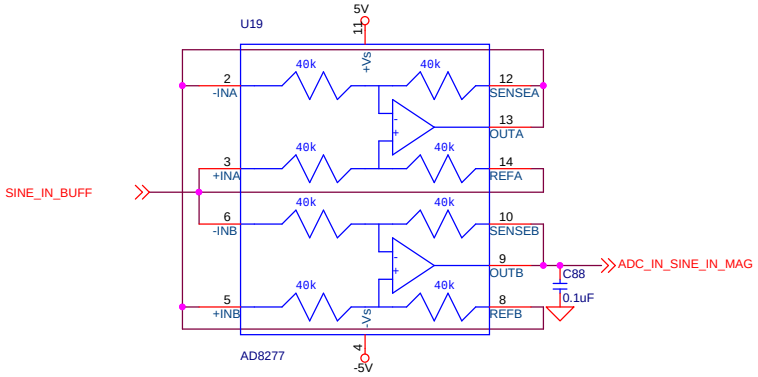


PLACE DECOUPLING CAPACITORS
NEAR IC POWER PINS





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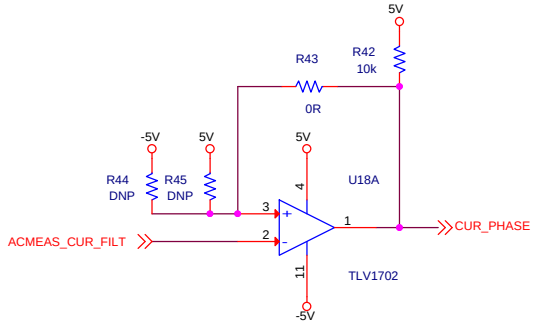

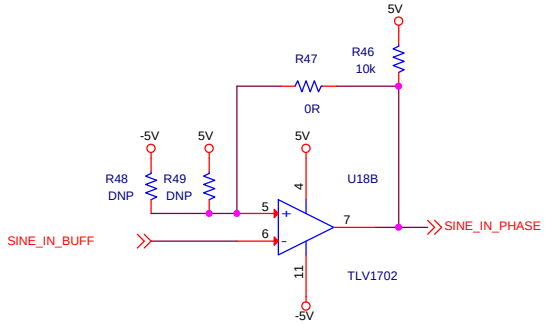

PHASE

IMPEDANCE / PHASE

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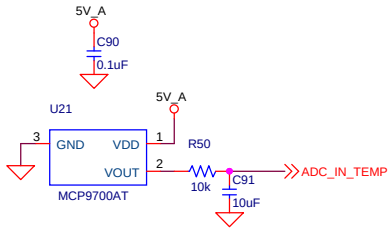

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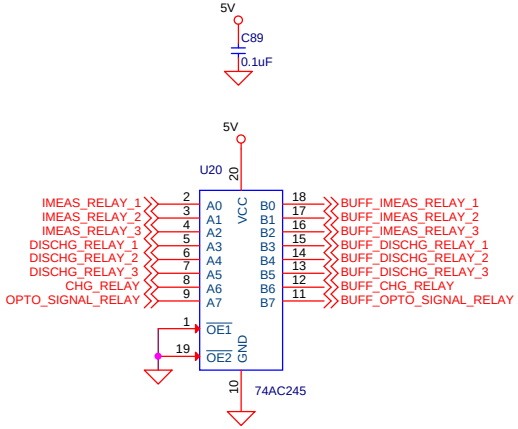

BUFFER

MISCELLANEOUS

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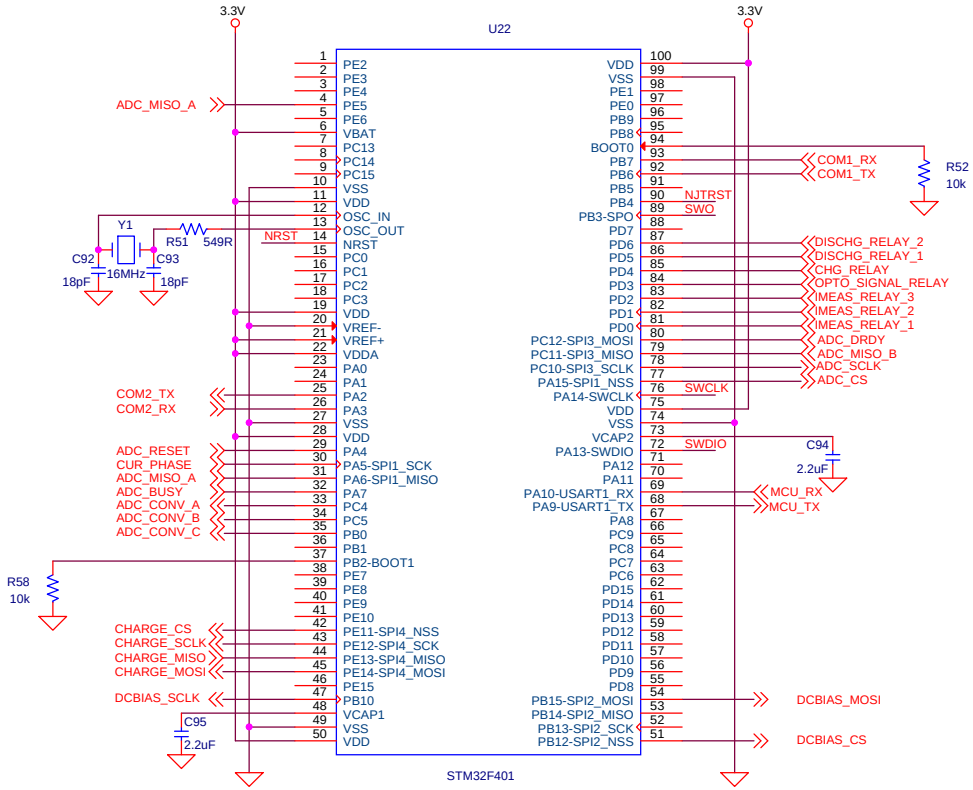

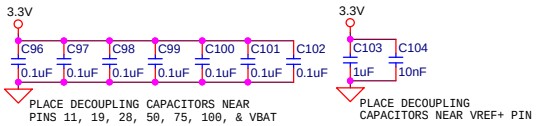

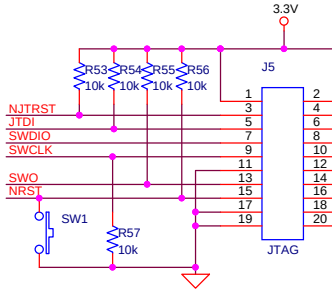

MCU I/O

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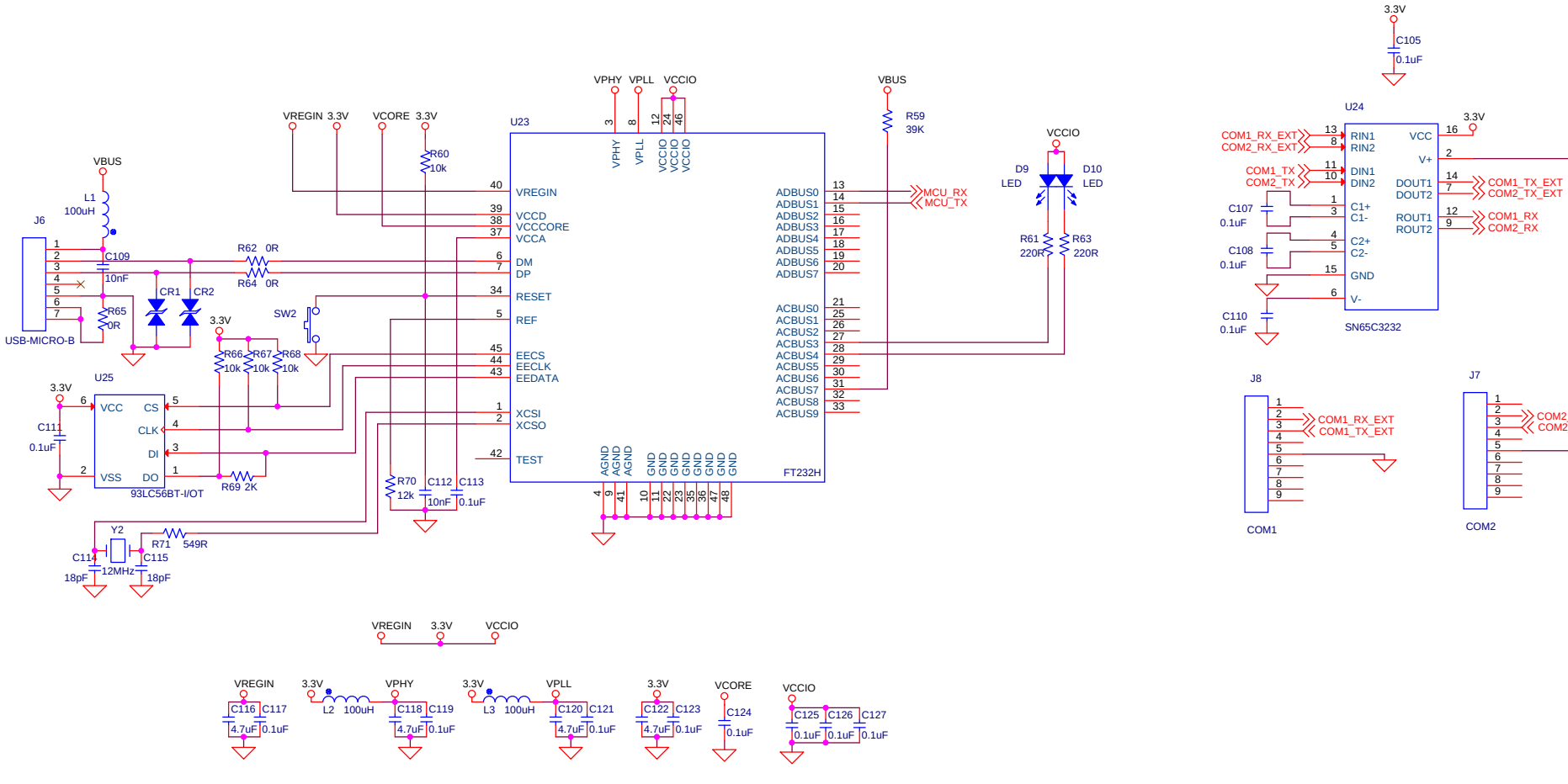

COMMUNICATIONS

Title	USB COMMUNICATIONS
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