DESIGN CONSIDERATIONS FOR CHARACTERIZATION OF CAPACITORS

by

MICHAEL DELIBERO

Submitted in partial fulfillment of the requirements for
the degree of Master of Science

Thesis Advisor: Dr. Merat

Department of Electrical Engineering
& Computer Science

CASE WESTERN RESERVE UNIVERSITY

TBD

CASE WESTERN RESERVE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

We hereby approve the master of science of

Michael DeLibero

candidate for the Master of Science degree*.

*We also certify that written approval has been obtained for any proprietary material contained herein.

Dedication

Dedication text

Table of Contents

List of Figures

List of Tables

Preface

Preface text

Acknowledgments

This should be the acknowlegement

List of Abbreviation

List of Abbreviations text

Glossary

List of Abbreviations text

Abstract

0.1 Previous Abstract

This paper presents an analysis of capacitor performance at up to 600VDC bias. The analysis is accomplished through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. All tests are recorded by means of multiple ADCs and computer analysis.

0.2 Current Abstract

This paper presents an analysis of capacitor performance degredation at up to a 600VDC bias. It proposes a testing method through small-signal impedance testing, charge and discharge time constant measurements, and leakage current measurements. Circuit analysis and itinial prototypes will be discussed.

1 Background

The following is a list of the questions that I will be answering in my background section.

1. Where are capacitors used with a high DC bias?
    (a) What characteristics are the most important there?
    (b) What are the main failure modes?
    (c) What are the current specifications of the parts in use now?
    (d) What research is being done to develope better capacitors for this use case?
    (e) How do they currently evaluate the capacitors?
    (f) How would they benefit from my research?
2. What is the state of the art in capacitance measurement?
    (a) Impedance analyzers
    (b) Capacitance bridges
    (c) Hi pot testers
    (d) What are the good and bad points of each of these technologies?
    (e) Why do they not solve the problem that I stated?
    (f) Why does this technology not currently exist?
3. What work has been done similar to this in the past?
4. What are the important characteristics of capacitors?
5. Is there any evidence that a capacitor's properties will change over DC bias?

2 History of Capacitors

This section will chronolog the history of capacitors. It will link various introductions in the technology to advances in industry, and it will map the driving forces behind capacitor development.

Types of capacitors:

1. Leyden jars
2. ceramic
3. aluminum electrolytic
4. tantalum
5. polymer
6. metalized film
7. foil film
8. titanium

Driving forces for development:

1. scientific study
2. military
3. radio industry
4. consumer electronics

Significant players:

1. ...

2.1 Comments

*You talk about the different types of MLCCs but are not very clear as to how the differences are achieved. *The only company you mention is Sprague but Cornell Dublier is also a big and I would need to think about others such as Aerovox. I am sure there are others. *You said very little about electrolytics in your discussion and the latest are low-voltage supercapacitors.

2.2 History

Capacitors have their origin in the invention of the Leyden jar by Peter van Musschenbroek of Leiden University in 1745. [13] It allowed for the storage of electrical energy for the first time in known history.

The Leyden jar was typically made from a glass jar with metal sheets spread on the inside and outside. Electricity could be stored by charging the jar with an electrostatic device and the removing the jar. This breakthrough in the study of electricity was exremely important to scientists, as it allowed electricity to be stored and then used later. [10]

The most common design for the Leyden jar was to use a glass jar with metal foil lining the inside and out. Then inner surface was typically charged via an electrostatic generator, while the outer surface was connected to ground. The charge would stay on the metal foil until a short or small resistance was connected between them. Charge could be stored this way, allowing scientists and showmen, to use greater amounts of charge than they could generate at any one moment.

Since the Leyden jar, many different types of capacitors have risen and fallen in prominence in the market. This section will cover the historical introduction of some of the major types.

Paper capacitors use waxed paper as a dielectric. They are primarily used in high

voltage applications. But they are not preferred for much due to their high leakage and tolerances.[14] In 1876 Fitzgerald introduced wax impregnated paper dielectric capacitors with foil electrodes.[3, ch. 11] [14] They were typically used for power supply filtering in radios. In the early 1920s, they existed as tubes encapsulated in plain, bakalized cardboard, with bitman sealing the ends.[3, ch 3]

Impregnated paper capacitors used paper that was soaked in mineral oil. It was interleaved with metal foil and then rolled to make the capacitor.[23, ch. 8.2.1.1] During WW2, paper capacitors were upgraded with metal-cased tubes with a rubber end.[23, ch. 8.1] Metalized paper capacitors were created as a replacement for impregnated paper capacitors. They were constructed similarly with the improvement that one side of the paper dielectric was sprayed with metal.[6]

Karol Pollak discovered the principle of the electrolytic capacitor in 1886 while he was researching the anodization of metals. In 1897, he received a patent for the borax-solution aluminum electrolytic capacitor. In 1926, Julius Lilienfeld patented an electrolytic capacitor containing electrolyte soaked paper. Ralph D. Mershon developed the first practical, commercially available radio electrolytic capacitor. After the start of WW2, increased funding and effort was applied to the cause of electrolytic capacitors and technics such as "etching and pre-anodizing" greatly increased their reliability. [31]

In 1897, Charles Pollak received a patent for the borax electrolyte aluminum electrolytic capacitor. In 1936 Cornell-Dubilier opened a factory to produce aluminum electrolytic capacitors. These capacitors became more reliable after WW2, when the industry applied additional resources to develope the technology.[8]

M. Bauer of Germany invented the mica capacitor in 1874. The original mica capacitor was a "clamped" style capacitor, which was used through the 1920s.[32] Clamped style mica capacitors were eventually replaced by silver mica capacitors, which greatly increased mica capacitors' characteristics.[14].

Mica's inherent inertness and reliability allowed for extreme reliability and efficiency in a packaged capacitor.[29] The mica capacitor was heavily used in the radio industry due to its superb stability at RF frequencies and physical robustness.[22]

During WWI, mica capacitors began to be produced in large quantities. This was mainly due to it being able to survive shock from weapons better than its glass counterpart. Also, it allowed the capacitors to be shrunk to achieve the same purpose. [3, f. 37-41]

In light of mica supply chain problems and the emergence of ceramic capacitors during WW2, mica capacitors fell from prominence to a niche market.[1, Ch 3, Sec II]

The first glass dielectric capacitor was, in fact, the Leyden jar. While this early capacitor was used mainly for scientific experiments, commercial glass capacitors came later.

Glass tubular capacitors appeared in 1904 and were used in Marconi's experiments in wireless transmission. They were know as Moscicki tubes. They continued to be used in wireless communication until about WWI. [3, p. 102]

Scientists in Germany created the first steatite ceramic capacitor in 1920. [1, Ch 3 Sec II] [12] Also known as talc, this ceramic capacitor variant was able to closely match the temperature coefficient of mica.[7]

Rutile ceramic capacitors were introduced with a dielectric constant of 10 times that of steatite. It was typically blended with steatite to get a better temperature coefficient.

A ceramic composition wth barium titanate (BaTiO3) was first discovered in 1941. Barium titanate was quickly found to be able to exhibit a dielectric constant over 1000; an order of magnitude greater the best at this time (rutile - $Ti0_2$). It was not until 1947, that barium titanate appeared in its first commercial device, phonograph pickups.[11][6][1, Ch 3 Sec III] Today barium titanate is still seen in multi layer ceramic capacitors.

Multi-layer ceramic capacitors are the current leading technology in commercially

produced units. They are divided up into three classes. Class 1 type MLCCs are known for their extremely good temperature characteristics. COG/NPO types can have 0-30ppm/^{o}C. These capacitors are typically made by combining TiO_2 with additives in order to adjust its temperature characteristics[19]. Additinally, class 1 ceramics have comparitively poor volumetric efficiency, and will tend to come in larger packages than class 2 ceramics of the same capacitance value. Class 2 types typically have worse temperature coefficients than type 1 types, but they have a much higher volumetric efficiency.They are constructed with a ferroelectric base material, typically Barium Titanate.[19]. Class 2 ceramic capacitors are the most common type of ceramics used. Class 3 types have very high capacitance, but a working voltage of several volts.[6][1, Ch 3 Sec VI][5]. They were originally developed as a potential replacement for liquid electrolytics, but have fallen out of favor due to the advances in Class 2 ceramics to the point where the gap between these two in terms of maximum capacitance is no longer viable[30].

Bell labs invented the first solid tantalum capacitor in 1956. They created it in conjuncture, and for, transistors.[3, f. 56-64] Tantalum capacitors typically have better characteristics than aluminum electrolytics, but have a lower maximum capacitance and working voltage.[14]

Sprague patented the first commercially viable solid tantalum capacitor in 1960. It offered an increased capacitance per unit volume and greater reliability.[24] In the 1970s, Sprague released the first surface mount tantalum capacitor.[26]

One of the historical problems with tantalum capacitors has been a limited supply of tantalum in the world market. This has occasionally caused price spikes in the material, hurting the tantalum capacitor market. As a result of the price spike around 1980, manufacturers created finer grain tantalum powders. This allowed a unit to be made with less overall tantalum, reducing price and package size.[9, ch 3.1]

3 Capacitor Parameters

3.1 Comments

*In Section 3.1 you could mention what characteristics are important for that application. And capacitors for switching power supplies are conspicuously absent. *Do you want to get into capacitor parameters such as stability, temperature operating range, working voltage, peak or surge current, etc

3.2 Practical Capacitor Uses

Before getting into the individual capacitor parameters, I will explain some of the basic uses for capacitors. Each of the individual parameters will be important and have a direct effect on the uses described here. One should be careful to remember that any model consisting of the parameters listed in this section (and others) only describes an approximation of what is happening inside of a capacitor. Models and capacitor parameters will never be 100% correct, but can be made with fairly high accuracy. As long as the designer understands the circumstances in which the models are accurate, he can use them to make a better circuit.

The most basic reason for wanting to use a capacitor is that it has the ability to store charge, which is close to the same thing as saying that it has the ability to store energy. It can store and release energy quickly to be able to react to the needs of the circuit.

3.2.1 Power Supply Bypassing

One of the most common uses of capacitors in bypassing a DC power supply (see Figure: 1). Without a bypass capacitor, a portion of the noise or any voltage spikes on the input to a power supply is passed to the output. A capacitor from the input to ground acts as a local charge reservoir to smooth out any non-DC components on

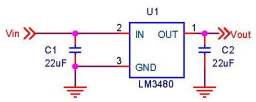


Figure 1: Power Supply Bypassing Circuit

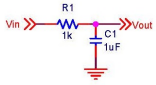


Figure 2: Analog Filtering Circuit

the input voltage. Putting a bypass capacitor on the output of a supply prevents load surge currents from causing the output voltage to dip. This is especially important with digital chips, as their high frequency switching can result in glitching if the supply is not properly bypassed.

3.2.2 Analog Filtering

Another use for capacitors is in analog filtering. The lowpass filter in Figure: 2 attenuates frequencies above a cutoff point, set by the values of the resistor and capacitor. Low pass filters are needed in many applications, such as anti-aliasing, clock filtering, and integration.

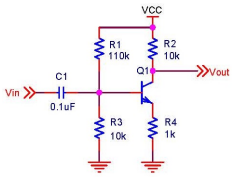


Figure 3: DC Blocking Capacitor

[20][ch 2.08 fig 2.27 pg 77]

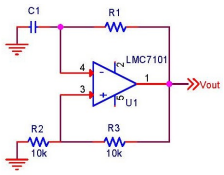


Figure 4: Oscillator Circuit

[20][ch 5.13 fig 5.29 pg 285]

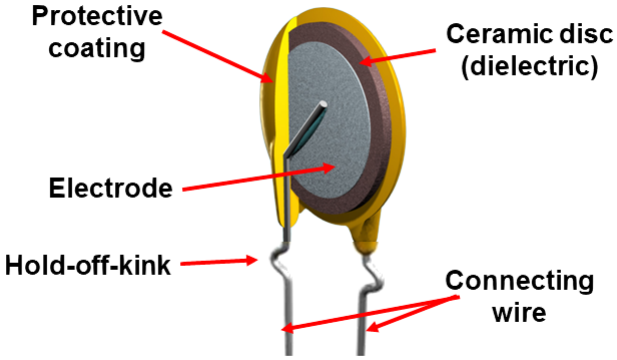


Figure 5: Power Factor Correction Circuit

3.2.3 DC Blocking

Designers often take advantage of capactors' characteristic of passing AC current while blocking DC current. As in Figure: 3, a capacitor can be used to block a DC offset before an amplifier.

3.2.4 Oscillators

Capacitors are also used in oscillator circuits. The relaxation circuit in Fig: 4 generates a square wave output at a frequency determined by the RC time constant of the passives.

3.2.5 Power Factor Correction

The inductors in modern DC-DC switching supplies have required increased attention to the engineering phenomenon know as power factor. Any electrical load with an inductive component causes the supplied current phase to lag the voltage phase. This effect decreases the efficiency of the power distribution and also has the ability to cause stability issues. A capacacitor can be used as a simple, passive way to move the power factor back towards the ideal state (See Figure: 5). [21]

3.3 Capacitance

There is a distinct difference between a capacitor and capacitance. While a capacitor's dominant characteristic is capacitance, it cannot be modeled entirely as such in most practical applications. There are also various inductive and resistive components to a capacitor that are important in various circumstances.

$$C = \frac{Q}{V} \tag{1}$$

Capacitance is the ability to store electrical charge. Equation: (1) says that capacitance is stored charge that is spread throughout a volume. A device that can store a lot of charge in a small area has a large capacitance.The basic equation for a commercial capacitor is seen in Equation: (2).

$$C = \frac{\epsilon_0 A}{d} \tag{2}$$

When using a capacitor in a single-pole low-pass filter, the cutoff frequency can be determined by Equation: (3). The circuit designer will choose a value for C and R in order to meet the cutoff frequency restraint.

$$f = \frac{1}{2\pi RC} \tag{3}$$

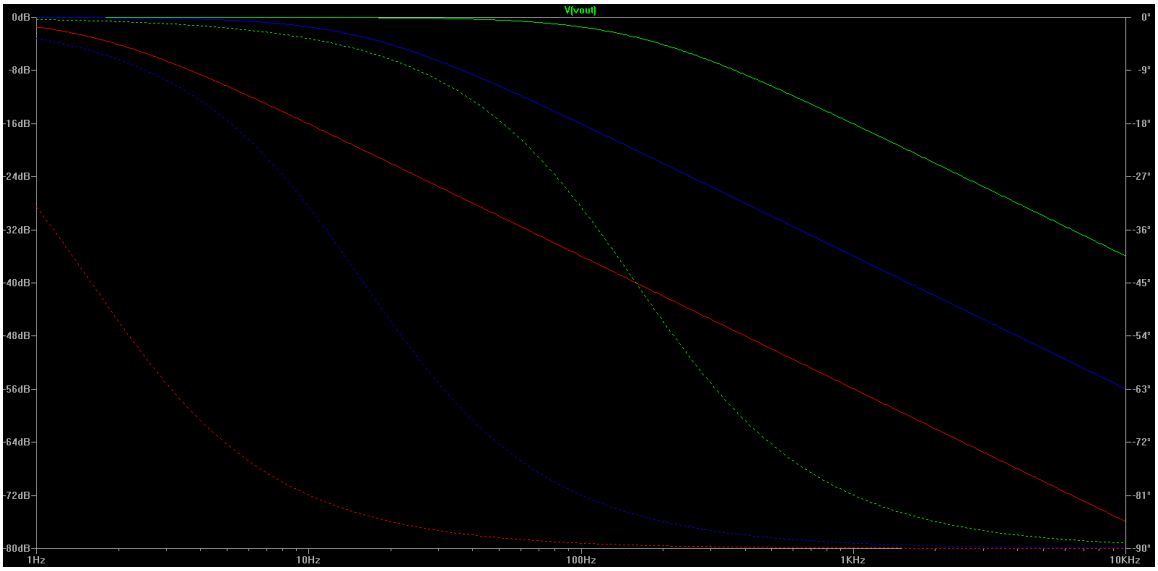


Figure 6: Low Pass Filter – Varying C

Varying the capacitance used in the filter will move the cutoff frequency and consequently get a different response in the filter. The effect of this can be seen in Figure: 6.

3.4 Impedance

The impedance of a capacitor is the "AC resistance" of the device. It determines the AC current that will flow when an ac voltage is applied to the capacitor via Ohm's law (Equation: (4)). An ideal capacitor has only a single capacative element and its impedance can be described via Equation: (5). The two main things to notice are that the impedance is frequency dependent and it is purely imaginary (reactive).

$$\vec{V} = \vec{I}\vec{Z} \tag{4}$$

$$\vec{Z} = \frac{1}{j\omega C} \tag{5}$$

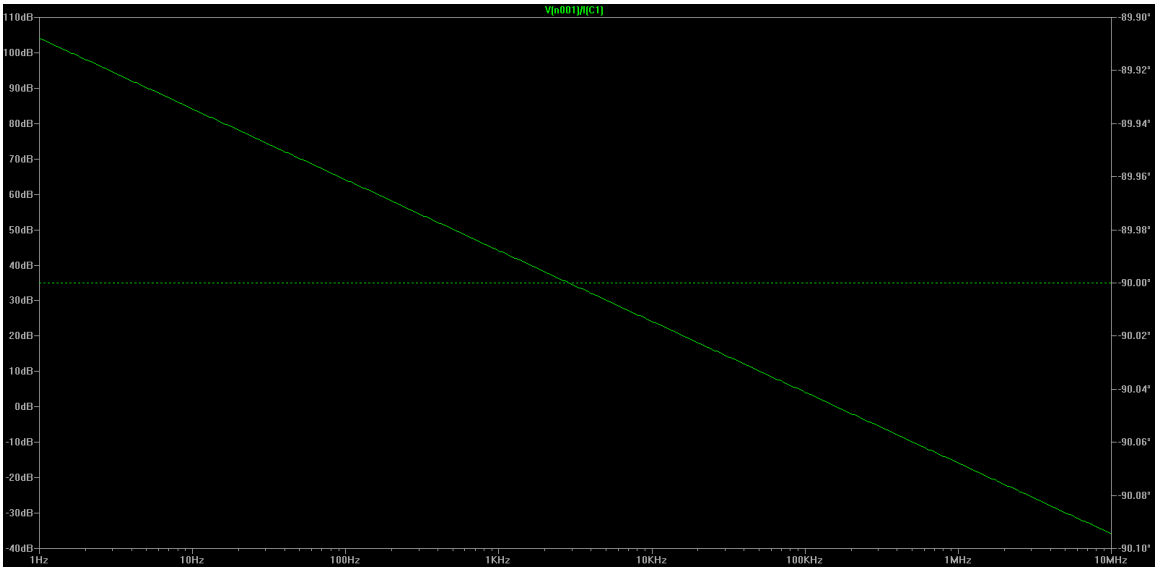


Figure 7: Capacitor Magnitude Over Frequency

$$Z = |\vec{Z}| = \frac{1}{\omega C} \tag{6}$$

In most AC applications we look at the magnitude of the impedance. Real capacitors have a more complicated impedance, but with an ideal capacitor we can simplify the magnitude equation down to Equation (6)

When capacitors are used in bypassing power supplies, the idea is to have a low impedance for common or expected noise frequencies. One may be tempted to choose a large valued capacitor to use for bypassing a wide range of frequencies. This turns out to backfire in practical situations, due to other parasitics in a real capacitor. For any capacitor, the impedance equation is more complicated, and the impedance value will begin to increase with frequency after some point. This will cause the designer to choose several different valued capacitors in parallel when bypassing a power supply or sensitive component. We will see later that the frequency plot of a capacitor will end up being more complicated than the simplified version seen in Figure: 7.

3.5 Phase

The phase of a combination of resistive and reactive components can be written as in Equation: (7).

$$\phi = tan^{-1}[\frac{X_c}{R_c}] \tag{7}$$

For an ideal capacitor, having no resistance and only capacitance, the phase angle can be simplified to:

$$\phi = -i = -90^0 \tag{8}$$

The practical implication of this can be seen in the phase response of a low pass filter (Figure: 6). The capacitor introduces a phase lag relative to the input signal's frequency. If you would compare the input and output signals in time, the output's peak would lag behind the input's by the phase amount predicted in the phase response.

3.6 ESL

The Equivalent Series Inductance (ESL) of a capacitor is a lumped estimate of all of the inductive components of a capacitor. It is typically modeled as an inductor in series with the bulk capacitance (See Figure 8).

Adding ESL to the capacitive model creates a new impedance equation (Equation: (9)). Note that for L<<C, this equation simplifies to Equation: (5) for low frequencies. In otherwords, the ideal impedance equation can be reasonably used for "low" frequencies.

$$\vec{Z_c} = j\frac{\omega^2 LC - 1}{\omega C} \tag{9}$$

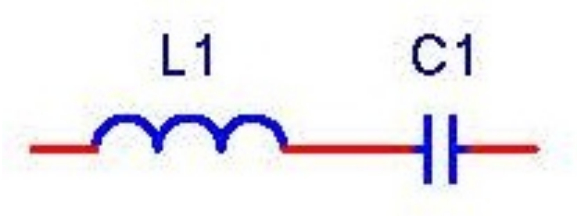


Figure 8: ESL Capacitor Model

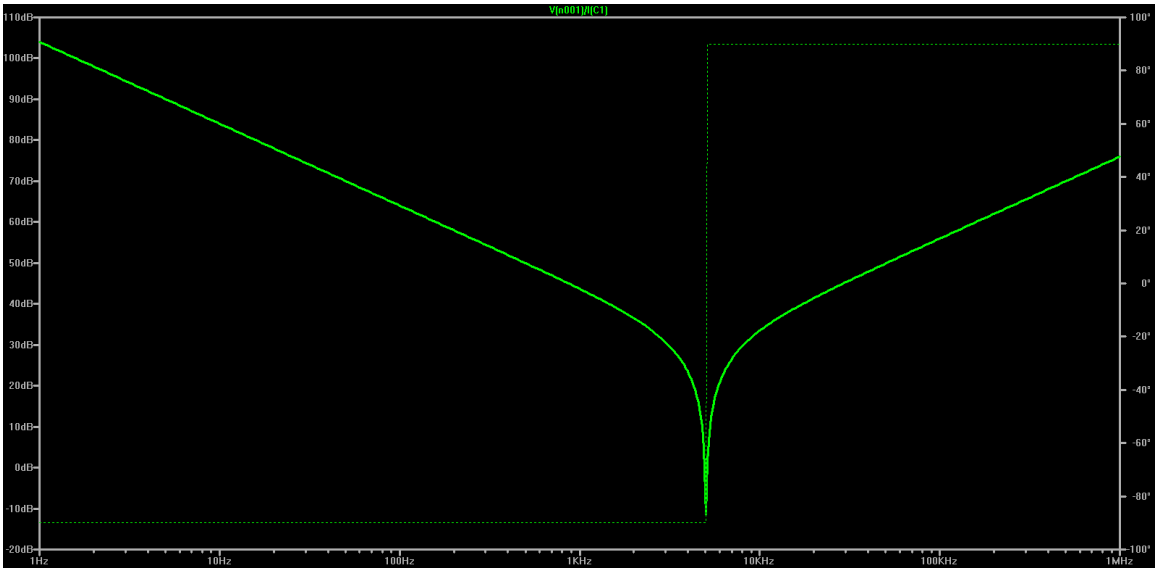


Figure 9: Capacitor Impedance with ESL

Figure: 9 shows a graphical representation of a capacitor's magnitude and phase once ESL is considered. This plot shows that after a resonance point, the impedance of the inductor (which increases with frequency) will begin to dominate. This makes the capacitor uneffective as a bypass element at frequencies higher than its resonance point. Typically, this frequency point and the capacitor's value have an inverse relationship. This is why you will see power supplies and sensitive chips being bypassed by a range of different valued capacitors.

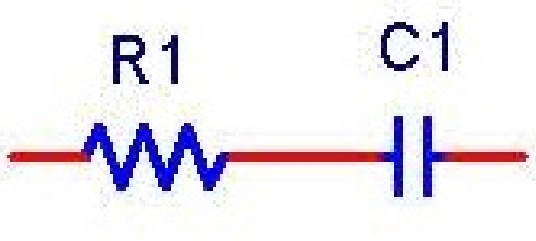


Figure 10: ESR Capacitor Model

3.7 ESR

The Equivalent Series Resistance (ESR) is the practical result of the fact that the materials used to create a capacitor have resistance. In simple cases, this can be approximated by a resistance in series with a capacitor (See figure: 10).

ESR becomes is important when thinking about DCDC switch mode power supplies. In this situation, a bypass capacitor is used to reduce the ripple voltage on the output of the converter. The AC current will pass through the ESR and dissipate heat as per Equation: (10)

$$P_{ESR} = I_{C,RMS}^2 * ESR[16] \tag{10}$$

Another important thing to note about ESR is that even though it is modeled as a resistance, it is not constant across all frequencies. It is a simplification of the resistive and capacitive elements in a capacitor that are dominated by resistance (Equation (11).

$$\vec{Z_c} = ESR + j * (\omega L - \frac{1}{\omega C})[16] \tag{11}$$

3.8 Resonance Frequency

Once C, ESL, and ESR are included into the capacitor model, a parameter know as the self-resonant frequency becomes evident. Equation: (11) shows that when

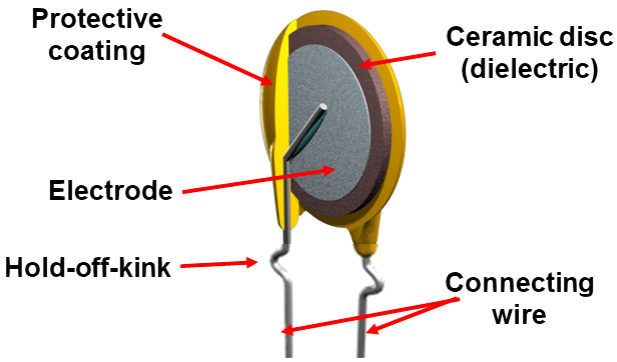


Figure 11: Dissipation Factor Plot

$Z_{ESL} == Z_C$, the capacitor is at its resonance point. At this frequency, the capacitor's impedance is determined solely by the ESR at that frequency. This frequency can be calculated by Equation: (12).

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

3.9 Dissipation Factor

Dissipation factor, otherwise known as the loss-tangent, is a measure of the energy stored to the energy dissipated per cycle. It is a measurement of the efficiency of the capacitor. The DF can be quantified through Equation: (13).

$$D = \frac{ESR}{Xc} \tag{13}$$

The loss tangent can be seen in Figure: 11. The greater the angle, the more efficient the capacitor will be.

3.10 Quality Factor

$$Q = \frac{1}{D} \tag{14}$$

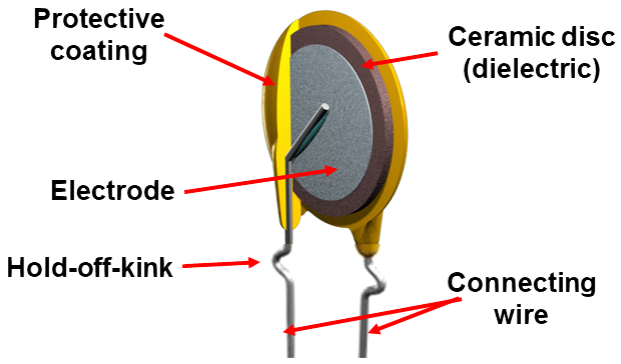


Figure 12: Dielectric Absorption

The Quality Factor, Q, of a capacitor is found by taking the reciprocal of the dissipation factor, Equation: (14). It is defined as the ratio of the energy stored to the energy dissipated per cycle.

3.11 Insulation Resistance

Every capacitor will have some DC leakage resistance associated with it. This measurement is attenuated by the insulation resistance of the capacitor. A high insulation resistance in a capacitor will increase its ability to store charge. This characteristic is especially important in sample and hold circuits.

3.12 Dielectric Absorption

Dielectric Absorption, DA, in a capacitor is a characteristic which describes the unit's ability to "regenerate" a charge after being shorted to ground for a brief time.

As seen in Figure: 12, a capacitor can be modeled with multiple RC element, of a much greater time constant, in parallel with the bulk capacitance. When the main capacitor is shorted to ground, and then released, the other capacitors may not have released their energy. After several minutes, they can recharge the main capacitance

to a significant portion of its original charge. This is why large valued electrolytic capacitors get shipped with a resistor across their terminals.

3.13 Old

This section will list and explain a large number of capacitor parameters. It will not deal with any analysis or measurement.

1. Impedance
2. Phase
3. Capacitance
4. Reactance
5. Equivalent Series Resistance (ESR)
6. Equivalent Series Inductance (ESI)
7. Leakage current
8. Dissipation factor
9. Quality factor
10. Dielectric absorption
11. Loss Tangent

4 Capacitor Modeling

Many designers have a need to simulate the response of the individual components in their systems to impulse and steady state inputs. When dealing with passive

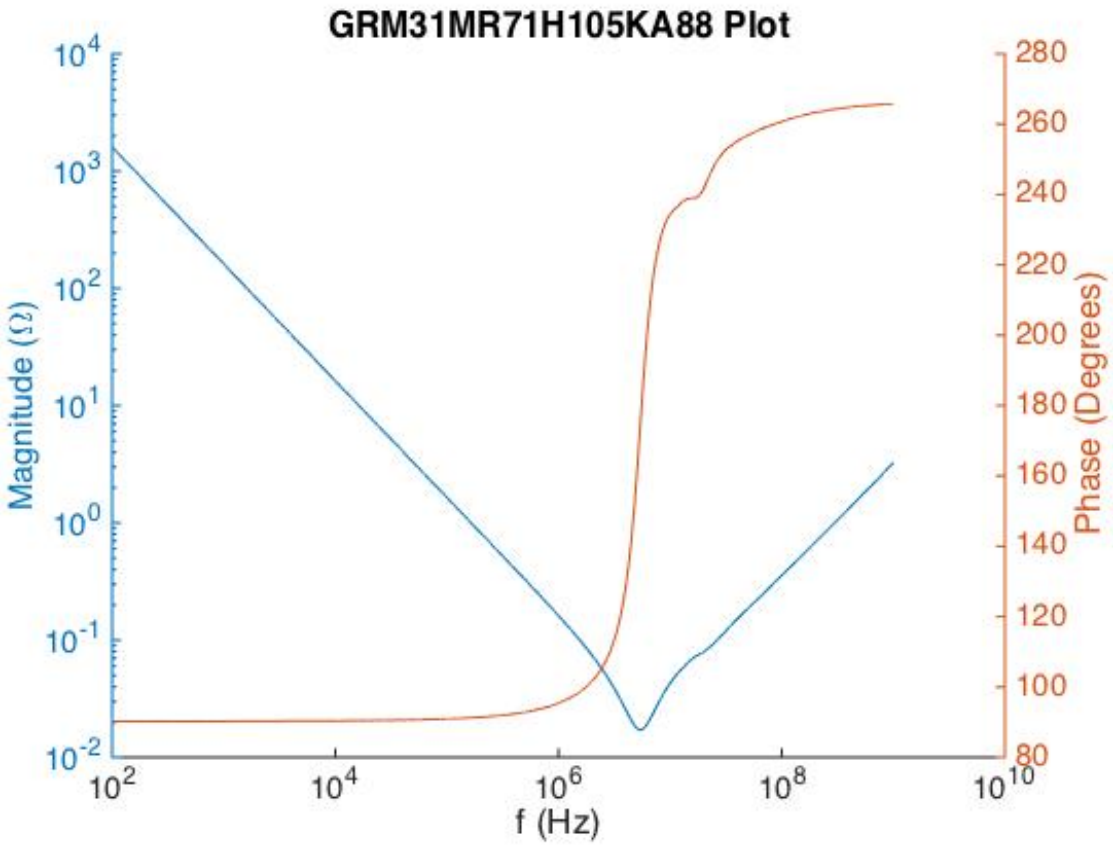


Figure 13: GRM31MR71H105KA88 Capacitor Data

electronic components, the device is typically modeled as a combination of various resitors, capacitors, and inductors. The model chosen is often due to either the required accuracy or a specific characteristic of the component that needs to be modeled. When characterizing a new component, the complex frequency response is recorded and then fit to a model. In this section, a progression of regression techniques will be evaluated for their ability to fit the measured frequency response of a capacitor to a polynomial equation. Then the accuracy of various capacitor models will be explored in regards to the fit. All models will attempt to fit the data from Figure: 13.

4.1 Regression Analysis

4.1.1 Basic LSE

At its core, regression analysis is an optimization problem whose purpose is to fit the equation of a line to a data set. A commonly use regression analysis technique is called the Least Equares Estimate (LSE). It attempts to find a model which minimizes the squared error between an emperical set of data and itself.

The first step in applying a LSE is to choose the form of the equation that best represents the data. The equation of a line, Equation: (15), is chosen when only a simple linear fit is needed. Then the squared error equation is generated, as in Equations: (16) & (17).

$$y = b_0 + b_1 x \tag{15}$$

$$E^2 = \sum_{i=1}^{n} (y_i - y)^2 \tag{16}$$

$$E^2 = \sum_{i=1}^{n} (y_i - (b_0 + b_1 x_i)^2 \tag{17}$$

In order to minimize the squared error over the data set, we need to take the partial derivate of Equation: (17) with respect to each of the unknown parameters, the coefficients, seperately. While b_0 and b_1 will be constants in the final equation, they are treated as variables here until they are known. Conversely, all x_i values are treated as constants. This results in Equations: (18) & (19).

$$\frac{\partial E^2}{\partial b_0} = 0 = \sum_{i=1}^{n} (-2y_i + 2b_0 + 2b_1 x_i) \tag{18}$$

$$\frac{\partial E^2}{\partial b_1} = 0 = \sum_{i=1}^{n} (-2y_i x_i + 2b_0 x_i + 2b_1 x_i^2) \tag{19}$$

Up to this point most LSE analyses follow the same basic path. But the rest of the steps depend upon the complexity of the model and solution techniques. The following steps in the basic LSE use transformations and substitutions to solve for the unknown variables. In our case, we can use Equations: (20) & (21) to remove the summation terms from the equation.

$$\bar{y} = (\sum_{i=1}^{n} y_i)/n \tag{20}$$

$$\sum_{i=1}^{n} y_i = \bar{y}n \tag{21}$$

This results in Equations: (22) & (23) with solutions shown in Equations: (24) & (25). The empirical data is then used to find the values of b_0 and b_1. At this point, the line can be used to estimate new points on the plot or to compare against other data sets.

$$0 = \bar{y} - (b_0 + 2b_1\bar{x}) \tag{22}$$

$$0 = \bar{xy} - (b_0\bar{x} + 2b_1\bar{x^2}) \tag{23}$$

$$b_0 = \bar{y} - b_1\bar{x} \tag{24}$$

$$b_1 = \frac{\bar{xy} - \bar{x}\bar{y}}{\bar{x^2} - \bar{x}^2} \tag{25}$$

4.1.2 Levy's Technique - Complex Curve Fitting

While the basic LSE technique is sufficient for many circumstances, it is not directly applicable in situations where we need to fit a complex line, such as a transfer function. Levy [15] shows an extension of the simple LSE example that is valid for a genaric

polynomial transfer function. This method is important because it not only allows for a complex-valued transfer functions, but it also prevents the nececcity of needing to rederive the system of equations for each new model.

$$G(s) = \frac{A_0 + A_1 s + A_2 s^2 + ... + A_n s^n}{B_0 + B_1 s + B_2 s^2 + ... + B_n s^n} \text{ [15][Eq. 3]} \tag{26}$$

Using Equation: (26) as the genaric model for the equation at hand, Levy shows that you can use Equations: (27), (28), (29), & (30) to simplify the series of partial derivates into a single matrix mtiplication equation shown in (31), (32), (33), & (34).

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h \text{ [15][Eq. 15]} \tag{27}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k \text{ [15][Eq. 16]} \tag{28}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k \text{ [15][Eq. 17]} \tag{29}$$

$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) \text{ [15][Eq. 18]} \tag{30}$$

$$MN = C \text{ [15][Eq. 20]} \tag{31}$$

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & \lambda_4 & \cdots & T_1 & S_2 & -T_3 & -S_4 & T_5 & \cdots \\ 0 & \lambda_2 & 0 & -\lambda_4 & 0 & \cdots & -S_2 & T_3 & S_4 & -T_5 & -S_6 & \cdots \\ \lambda_2 & 0 & -\lambda_4 & 0 & \lambda_6 & \cdots & T_3 & S_4 & -T_5 & -S_6 & T_7 & \cdots \\ 0 & \lambda_4 & 0 & -\lambda_6 & 0 & \cdots & -S_4 & T_5 & S_6 & -T_7 & -S_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots & \vdots & \vdots & \\ T_1 & -S_2 & -T_3 & S_4 & T_5 & \cdots & U_2 & 0 & -U_4 & 0 & U_6 & \cdots \\ S_2 & T_3 & -S_4 & -T_5 & S_6 & \cdots & 0 & U_4 & 0 & -U_6 & 0 & \cdots \\ T_3 & -S_4 & -T_5 & S_6 & T_7 & \cdots & U_4 & 0 & -U_6 & 0 & U_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \end{bmatrix} \quad [15][Eq.\ 21a] \tag{32}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \\ \vdots \\ B_1 \\ B_2 \\ B_3 \\ \vdots \end{bmatrix} \quad [15][Eq.\ 21b] \tag{33}$$

$$C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ T_3 \\ \vdots \\ 0 \\ U_2 \\ 0 \\ \vdots \end{bmatrix} \quad [15][Eq.\ 21c] \tag{34}$$

Levy's technique works well for applications where there is a small dynamic frequency range and a small number of coefficients, but there a several problems with it. The first problem is that for models with a wide bandwidth, the solution to Equation: (31), involves an ill-conditioned matrix. This means that the ratio of the "largest to smallest singular value in the singular value decomosition of a matrix is ... $>= log^{-1}$(input precision). In other words, it estimates a worse case loss of

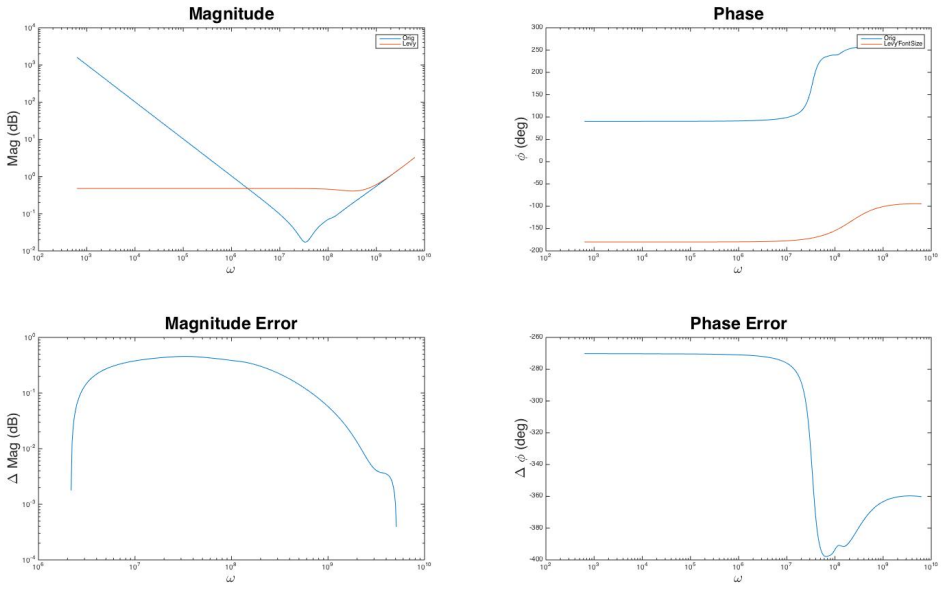


Figure 14: Levy's Technique

precision." The second problem is that this technique favors the magnitude plot at the high frequency range.

4.1.3 Weighted LSE

One improvement that can be made upon Levy's method is to iterate with a weighting function untill the error term is minimized[25]. By multiplying Levy's error function by the weighting term in Equation: (35), we get Equation: (36), which can be minimized to obtain a new system of equations.

$$W_{kL} = \frac{1}{|Q(jw_k)_{L-1}|^2} \text{ [25]} \tag{35}$$

$$E = \sum_{k=1}^{n} |\epsilon_k'|^2 W_{kL} \text{ [25][Eq. 7]} \tag{36}$$

Equations (31), (32), & (33) are the same, with Equations (27), (28), (29), & (30) being replaced with Equations: (37), (38), (39), & (40). The L subscript stands for

the current iteration, while $L-1$ stands for the previous iteration.

$$\lambda_h = \sum_{k=0}^{m} \omega_k^h W_{kL} \ [25][Eq.\ 9] \tag{37}$$

$$S_h = \sum_{k=0}^{m} \omega_k^h R_k W_{kL} \ [25][Eq.\ 10] \tag{38}$$

$$T_h = \sum_{k=0}^{m} \omega_k^h I_k W_{kL} \ [25][Eq.\ 11] \tag{39}$$

$$U_h = \sum_{k=0}^{m} \omega_k^h (R_k^2 + I_k^2) W_{kL} \ [25][Eq.\ 12] \tag{40}$$

This particular iteration method is not gauranteed to converge. Looking at Figure: 15. The squared error of the magnitude and phase do not converge after a particular number of iterations. Furthermore, they do not reach their minimums at the same iteration. In order to select the desired iteration, the magnitude and phase squared plots are normalized as such $n = min(Emag/max(eMag) + Epha/max(ePha))$. The index of the minium of Figure: 15 is selected as the best fit.

Figure: 17 shows that this method can result in a much improved result over the Levy's original method, as sseen in Figure: 14.

4.2 Modeling

This section will investigate several of the most common capacitor models. It will show how to fit them to a data set with Levy's method described in Section: 4.1, and will describe their effectiveness and limitations in doing so.

4.2.1 RLC

The RLC model, shown in Figue: 18, is one of the simplest models used to describe a capacitor. It shows the basic low and high frequency characteristics, along with the

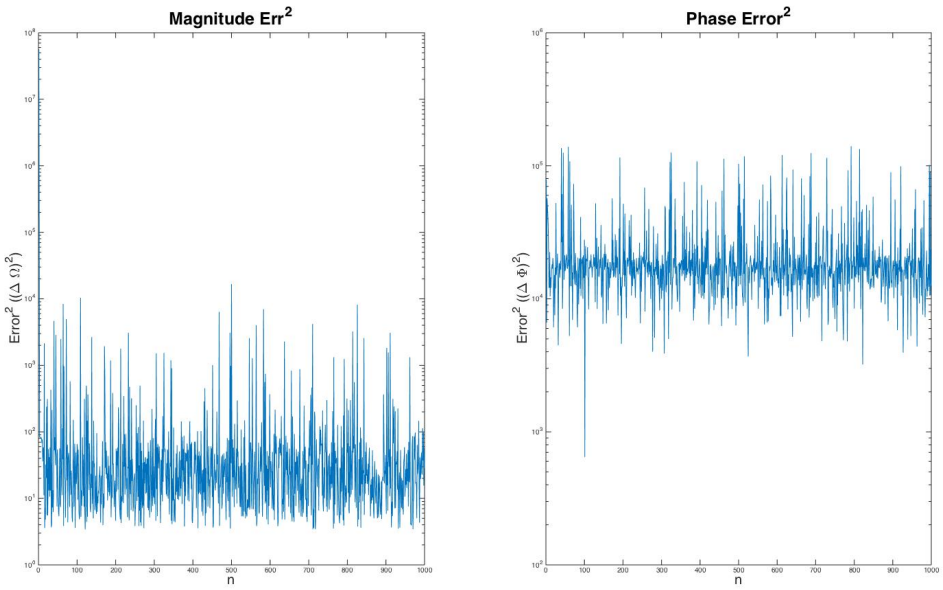


Figure 15: LSE + Iteration – Magnitude and Phase Error

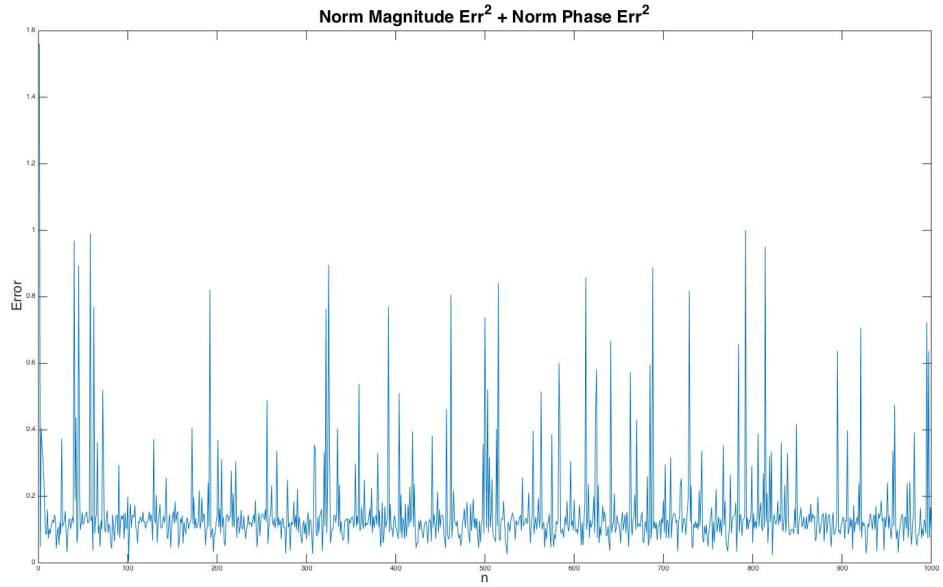


Figure 16: LSE + Iteration – Combined Error

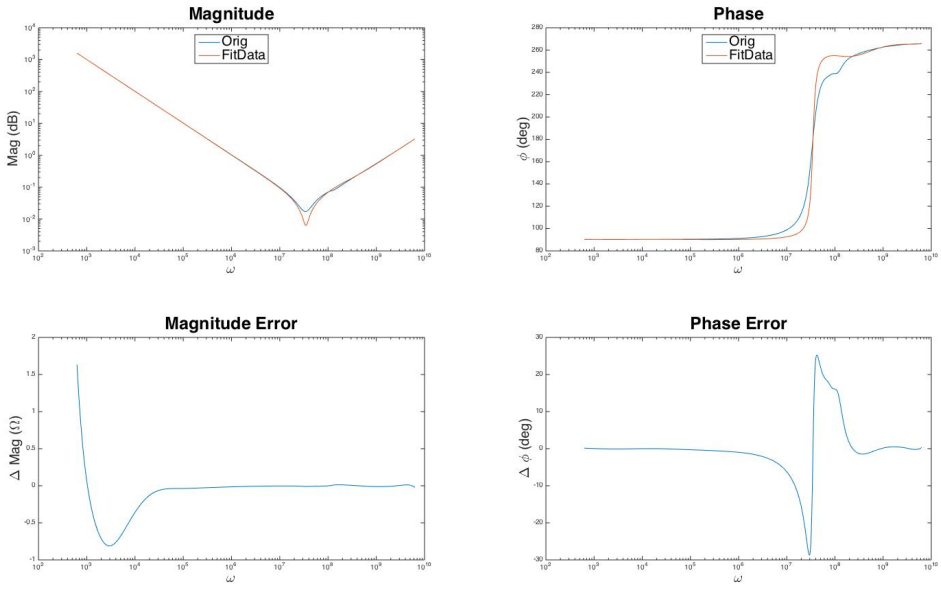


Figure 17: LSE + Iteration

Figure 18: RLC Model

capacitor's resonant point. Its impedance is described in Equations: (41) & (42), but our method does not allow for any poles at the origin. In Equation: (43) we multiply by s and fit the new equation to the data. At the end, we will divide by s to get our final result. At this point out eqution is in the proper form and can be abstracted into Equation (44).

$$Z(s) = R + sL + \frac{1}{sC} \tag{41}$$

$$Z(s) = \frac{1 + s(RC) + s^2(LC)}{sC} \tag{42}$$

$$Z_2(s) = Z(s) * s = \frac{\frac{1}{C} + s(R) + s^2(L)}{1} \tag{43}$$

$$Z_2(s) = \frac{A_0 + A_1 s + A_2 s^2}{B_0 + B_1 s + B_2 s^2} \tag{44}$$

For this model Equations: (32), (33), & (34) simplify down to Equations: (45), (46), & (47).

$$M = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & T_1 & S_2 \\ 0 & \lambda_2 & 0 & -S_2 & T_3 \\ \lambda_2 & 0 & -\lambda_4 & T_3 & S_4 \\ T_1 & -S_2 & -T_3 & U_2 & 0 \\ S_2 & T_3 & -S_4 & 0 & U_4 \end{bmatrix} \tag{45}$$

$$N = \begin{bmatrix} A_0 \\ A_1 \\ A_2 \\ B_1 \\ B_2 \end{bmatrix} \tag{46}$$

$$C = \begin{bmatrix} S_0 \\ T_1 \\ S_2 \\ 0 \\ U_2 \end{bmatrix} \tag{47}$$

Fitting this model to the data shown in Figure:

5 Measurement Circuitry

This section describes the schematic design used to meet the goals set out in the Abstract (Section: 0.2). The schematic can be found in the Appendix section: 7.

Input Scale	0 to +10V for 0 to 5kV
Input Impedance	1 MΩ
Accuracy	±0.2% of full scale
Update Rate	15 Hz
Output Slew Rate	<0.3s for 0 to full scale (full load)

Table 1: SRS PS350 External Voltage Control Characteristics

[28] [27]

5.1 DC Bias

A DC bias is needed to conduct AC measurements as well as to allow for measuring discharge curves of the DUT. In order to determine the effect of the DC bias on the DUT, it is necessary to conrol that quantity. This section describes the circuitry (Schematic Page: 3) used to provide a means to programatically control the DC bias from 0 to 500V. The supply used is a Stanford Research Supply (SRS) PS350. It accepts a DC control signal, which is supplied by the circuit through a DAC. If different supply characteristics are needed, it can be swapped out with any supply. A genaric RS232 bi-directional port (Schematic Page: 10) is provide to control the supply in this situation.

The SRS Supply's specifications can be seen in Table: 1. The output of the PS350 can either be set manually or with a 0-10V control voltage. This circuitry will take advantage of this analog input at a gain of 500.

The analog control uses an AD7391, 14-bit DAC with an internally generated reference. It is controlled via a SPI bus connected to a microcontroller. The update rate of this device is not important to this application because it will be set infrequently and only when the system is not actively collecting data. The output signal of the DAC is fed into an op amp which acts as a voltage limiter for safety. This clamps the control signal at 1.5V and the PS350's output at 750V.These numbers are

theoretical and will degrade from ideal due to the SRS's response to the control signal, the noise levels in the system, and various other factors, such as temperature.

The DAC has a 2.5V internal reference. With 14 bits, that gives the control signal an ideal resolution of $150\mu V$ and the PS350 an output resolution of $76mV$.

5.2 Current Measurement

Each of the tests utilize the low-side current measurement circuit. The AC measurement tests provide a known voltage across the DUT and then the current is used to construct the impedance. The discharge tests use the current measurement circuit to capture the current through the DUT over time as its energy drains.

Refdes	Value	Range	
R5	5	Hi	1A - 1mA
R6	5k	Med	1mA - 1uA
R7	5M	Low	1uA - 1nA

Table 2: Current Measurement Ranges

The current measurement circuit utilizes a transimpedance amplifier designed from the reference circuit in [4]. It utilizes 3 switched, feedback stages to measure 9 decades of current (See Table: 2). The circuit creates a virtual ground at the negative terminal of the DUT and then uses one of the feedback paths to create a voltage for a digitizer. Using a low-side current measurement circuit is beneficial in this circumstance because it allows low voltage circuitry to condition and measure a signal without needing to see the high DC voltage on the postive terminal of the DUT. The output voltage is calculated by Equation: (48).

$$Vo = I * R_f \tag{48}$$

*Add transitor in increase the Op Amp's current drive capability. *Change capacitors in feedback loop. *Add Salen-key filter to output *Exlain difference in two buffering stages

The output will be buffered and then filtered and digitized dependent of the specific test of interest.

5.3 Charge

This section of the circuitry is meant as a preperation stage for the other tests. It operates by setting the current measurement to High, closing the Charging Relay (LS4), and then ramping the DC Bias voltage with the high current measurement stage open. LS4 can be opened or left closed, dependent on the needs of the test.

5.4 Discharge Circuitry

The discharge circuitry provides a means to determine the bulk capacitance value of the DUT from the RC time constant. Once the DUT is charged to the desired voltage, the charging relay will open and then the high-current discharge relay will close. The current through the DUT will be measured as it decays.

There are 3 switched discharge stages that allow for the decay rate to be regulated. Each stage allows for a range of voltages and capacitances needed to stay within safety and operational constraints. As seen in Figure: 19, there are two constrainsts on both the voltage and capacitance. The lowest valued resistor constrains the maximum voltage when using that stage due to its power rating. The other two stages are constrained by the overall safety limit of 500VDC. The minimum capacitance for each stage is determined by setting a requirement of at least 100 ADC samples per time constant with a sampling rate of $250KSPS$. The maximum capacitance for each stage is determined by setting a maximum time constant.

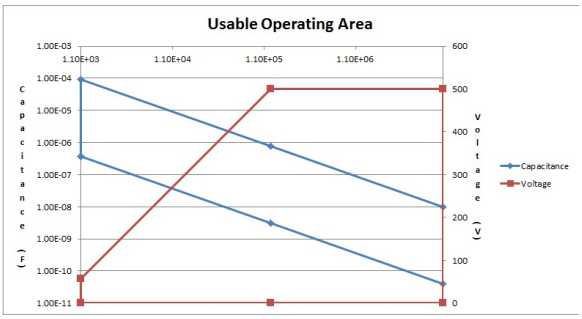


Figure 19: Operating Area

5.5 Magnitude

The magitude section takes the sinusoidal current measurement and creates a DC output by with a dual difference amplifier package. This technique as seen in [18] provides a method to measure the rms value of the AC current through the DUT. The first difference ampliflier is configured as a voltage follower. Since this circuit operates only from a single power rail, it passes the positive going portions of the waveform and clamps to ground for th negative going portions of the waveform. The second difference amplifier operates in different modes, based upon the output of the first differential amplifier. During the negative going portions of the waveform, its positive terminal is held at ground, and it operates as a unity gain, inverting amplifier. This rectifies the input signal to the output. During the positive going portions of the waveform, positive input terminal is held at the value of the input terminal. This forces the second difference amplifier to act as a voltage follower. In this manner, the circuit performs a full-wave rectification on the signal, which is then filtered and fed to the ADC for digitization.

5.6 Phase

This section explains the circuitry used to measure the phase difference between the input voltage and the output current. This measurement, combined with the

magnitude measurement, will allow for a complete impedance measurement at each frequency step of a test. The comparator circuit is configured as a sine to square wave converter. The two square wave signals will be fed directly into a timer input of the MCU. The MCU will measure the time between the two signals to determine their phase difference.

5.7 Communications

This section will describe the circuitry used to communicate to off-board processors.

5.7.1 USB

The USB section is used to communicate with a PC for data logging and data post processing. This circuitry centers around a FTDI FT232H serial to USB chip. It allows seemless USB communication to a PC's com port with the MCU only needing to use a UART port. This significantly lowers the complexity of the communication bus, as the MCU is not repsonible for running the USB stack.

5.7.2 RS-232

The board also has two, bidirectional RS-232 ports. They are able to be used for general purposes, but will most often be used for communicating with a sine-wave generator and an alternate DC Bias supply.

6 Conclusion

This section will summerize the methodologies used to solve the stated problem.

7 Future Work

This section will describe the future work needed to be accomplished in order to complete and further the stated goals of this thesis. It will mostly focus on the practical circuitry implementation and other aspects needed to make it a viable tool.

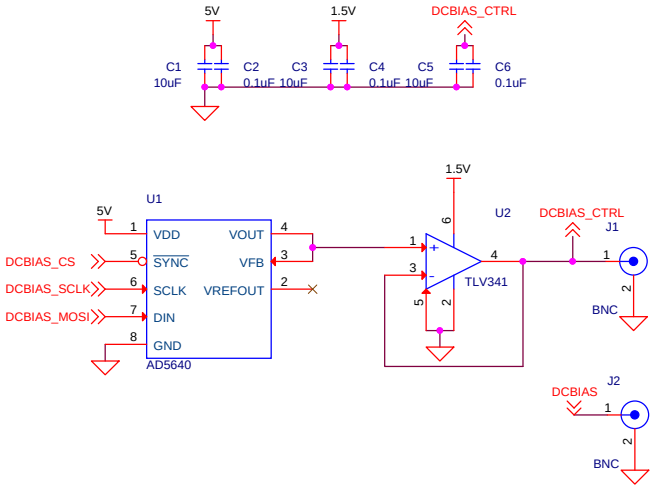
Appendix

TABLE OF CONTENTS

Title	TABLE OF CONTENTS
Size B	Document Number DELIBERO_THESIS
Date: Tuesday, February 17, 2015	Sheet

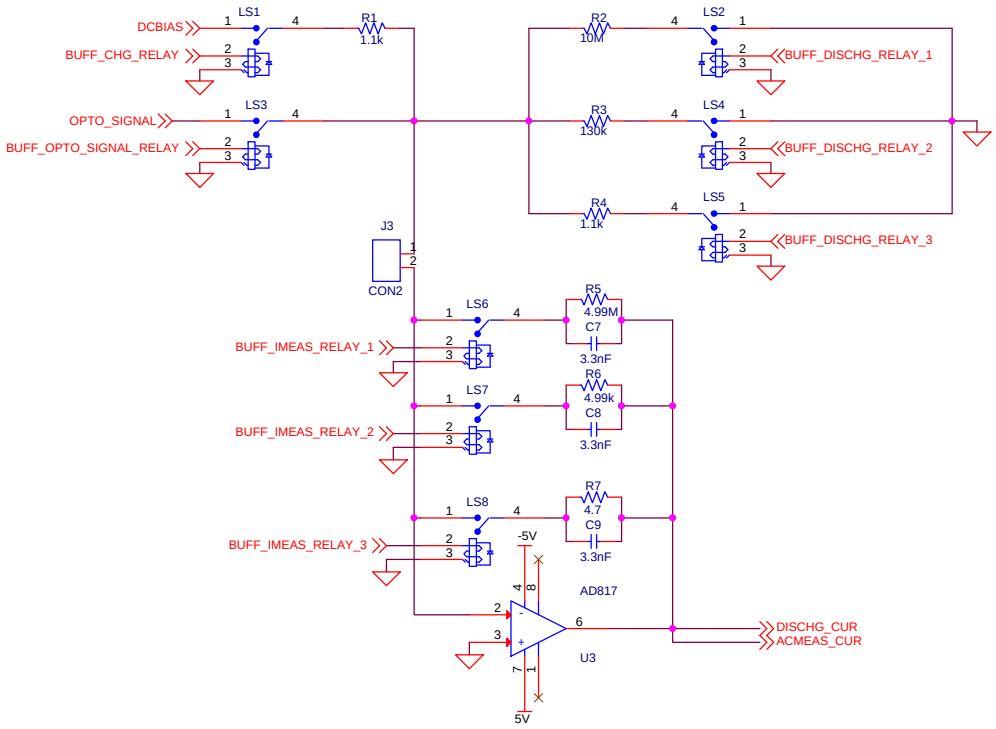
POWER SUPPLIES

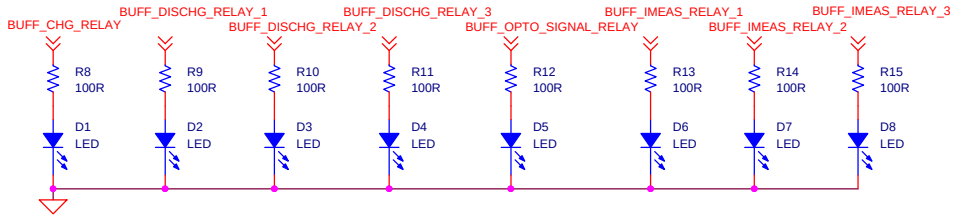
Title: POWER SUPPLIES		
Size: B	Document Number: DELIBERO_THESIS	
Date: Tuesday, February 17, 2015	Sheet	



DC BIAS CONTROL

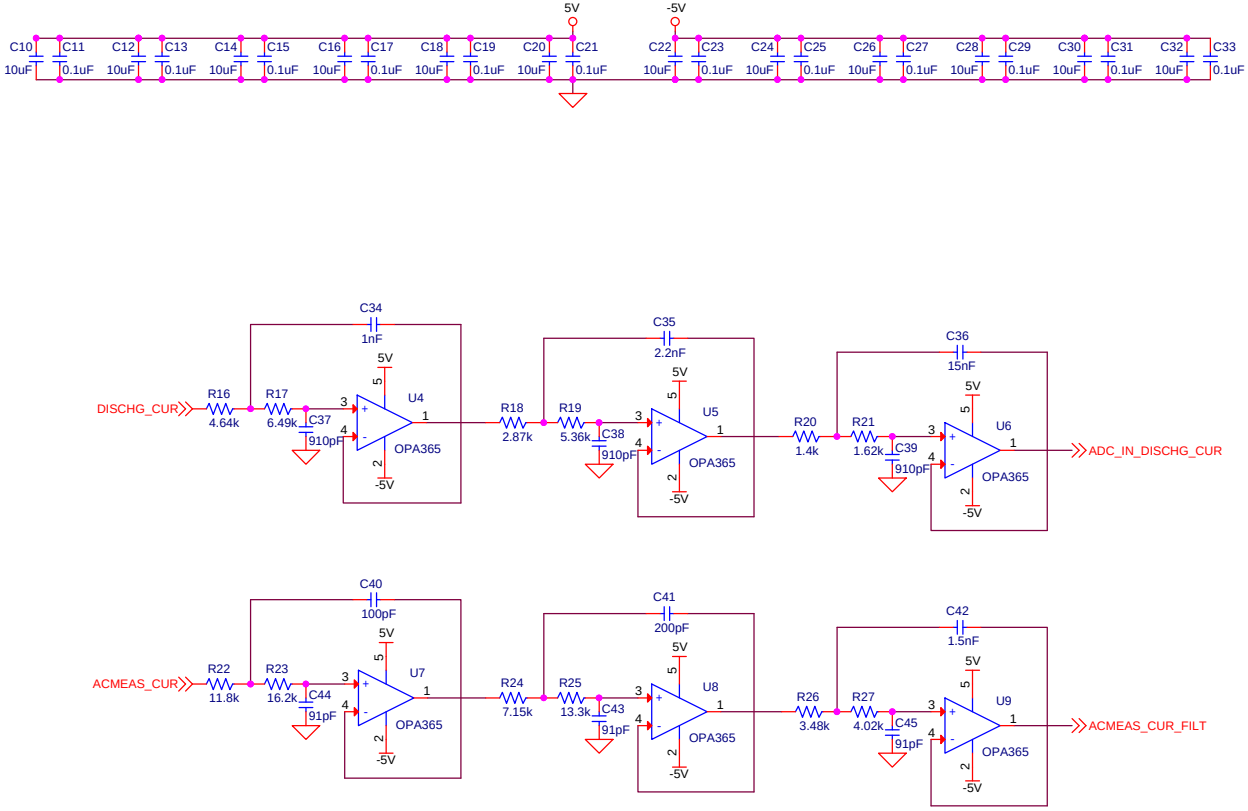
Title	DC BIAS CONTROL	
Size B	Document Number DELIBERO_THESIS	
Date: Tuesday, February 17, 2015		Sheet





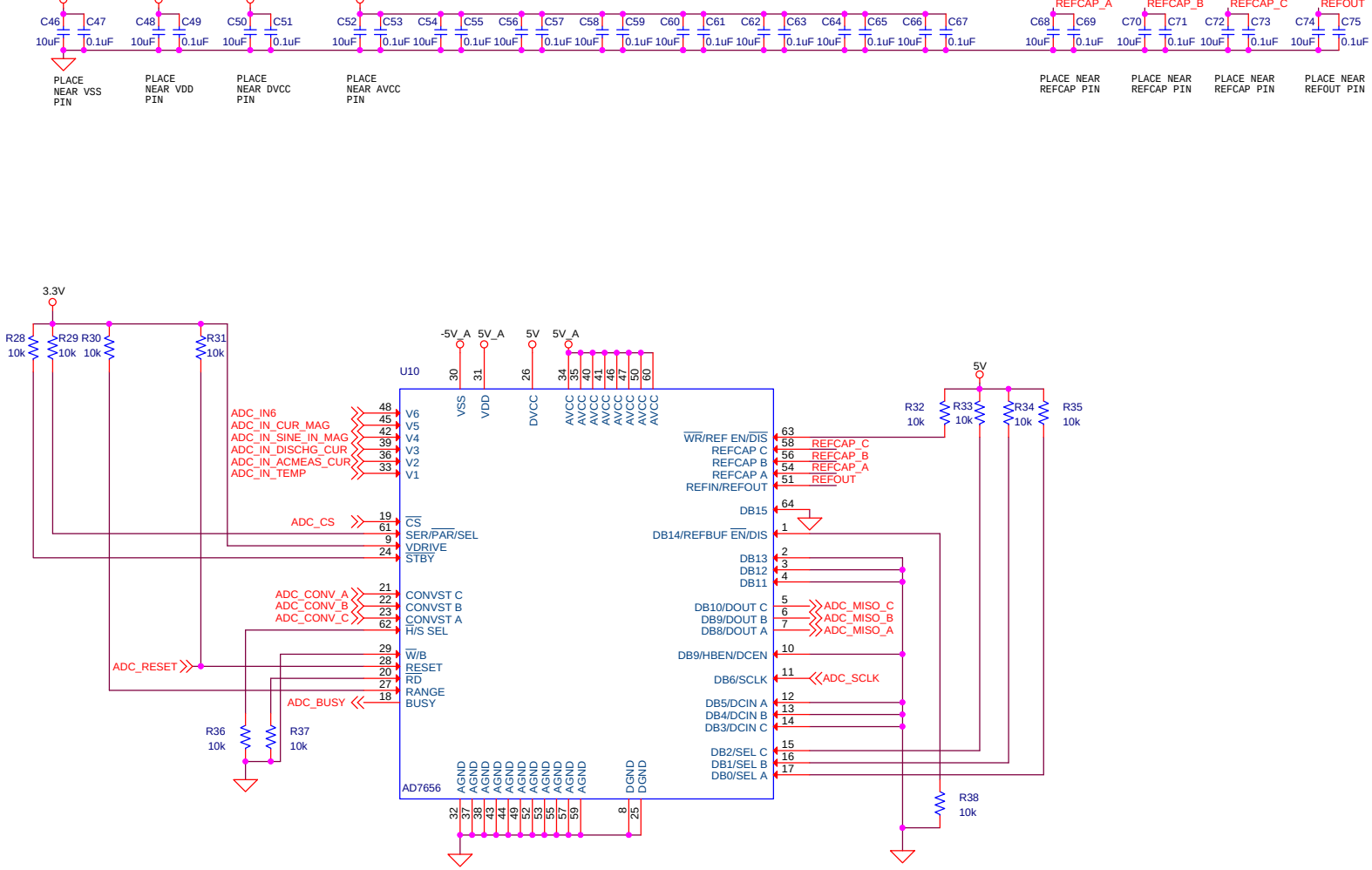
DISCHARGE CIRCUITRY

Title	DISCHARGE CIRCUITRY
Size: B	Document Number: DELIBERO_THESIS
Date: Tuesday, February 17, 2015	Sheet



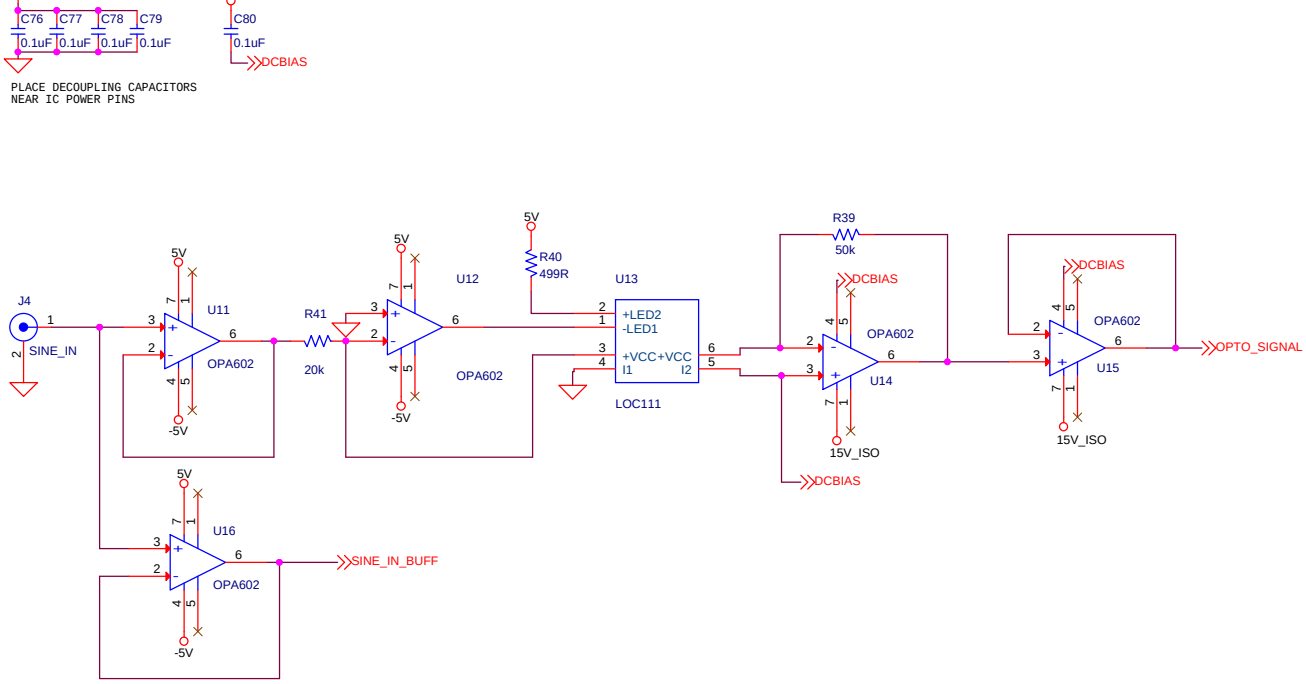
FILTERING

Title: FILTERING		
Size: B	Document Number: DELIBERO_THESIS	
Date: Tuesday, February 17, 2015	Sheet	



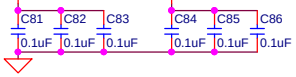
ADC

Title: ADC		
Size: B	Document Number: DELIBERO_THESIS	
Date: Tuesday, February 17, 2015	Sheet	

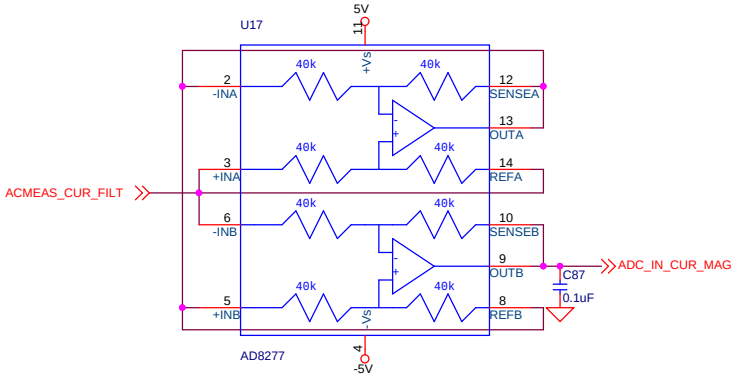


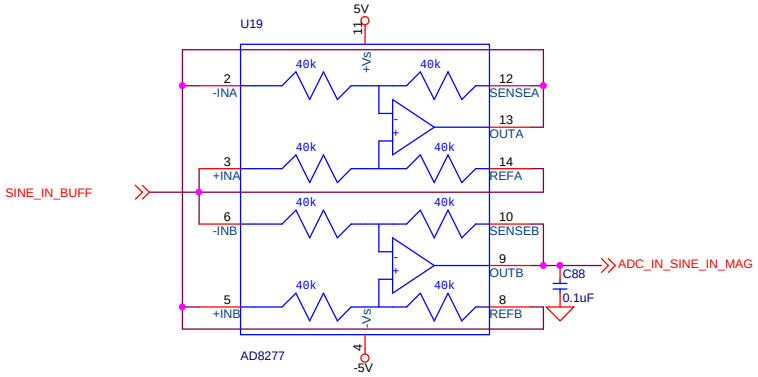
OPTOCOUPLER

Title	OPTOCOUPLER	
Size B	Document Number DELIBERO_THESIS	
Date: Tuesday, February 17, 2015		Sheet

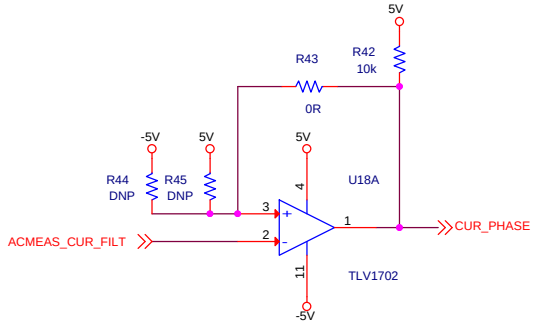


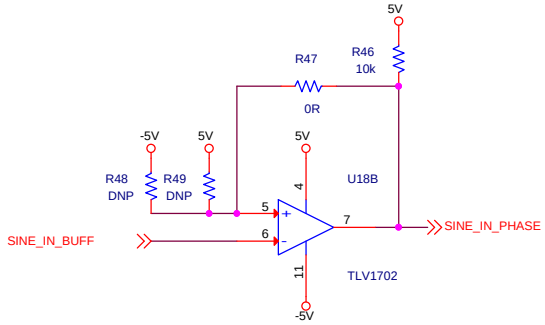
PLACE DECOUPLING CAPACITORS
NEAR IC POWER PINS





MAGNITUDE

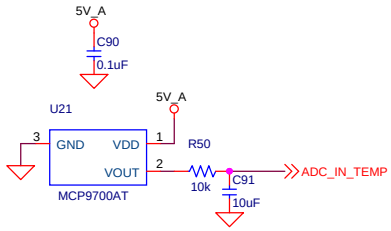




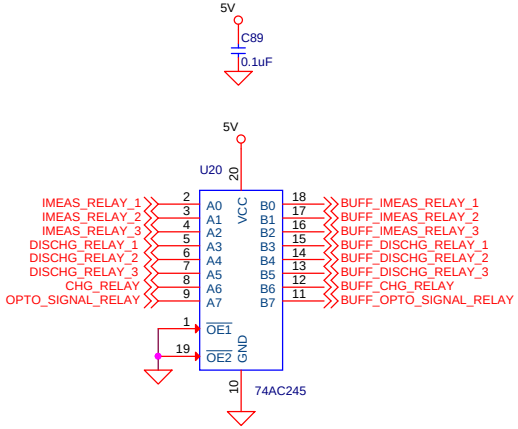
PHASE

IMPEDANCE / PHASE

Title	IMPEDANCE / PHASE	
Size B	Document Number DELIBERO_THESIS	
Date: Tuesday, February 17, 2015		Sheet



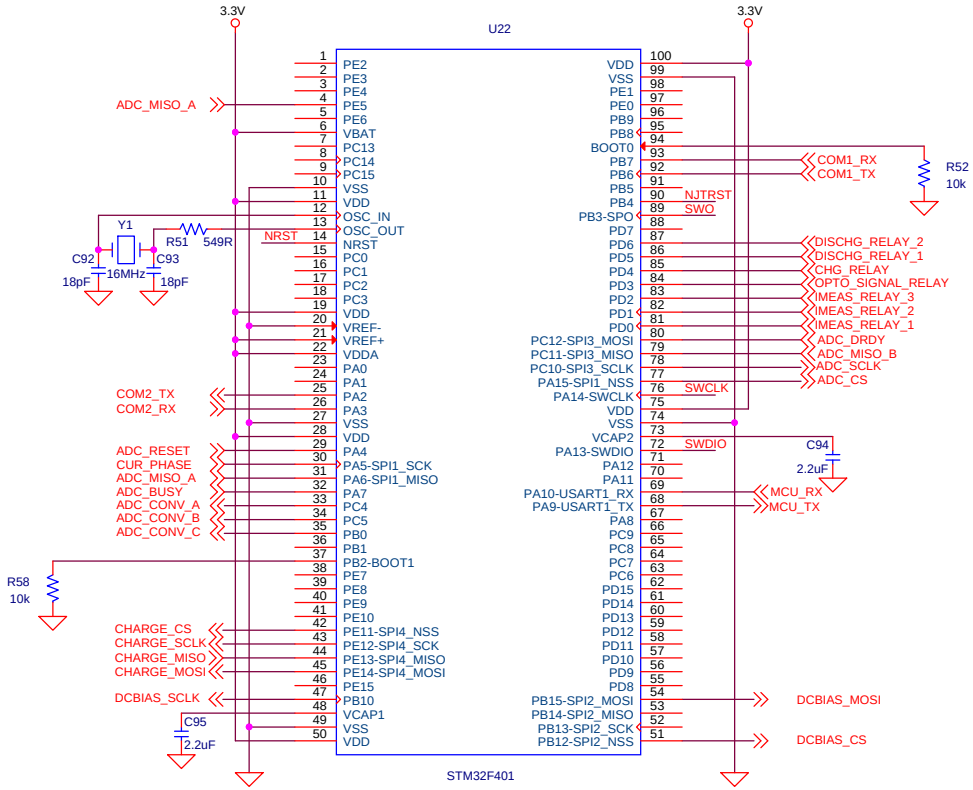
TEMPERATURE

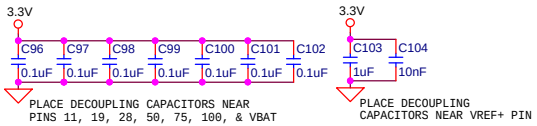


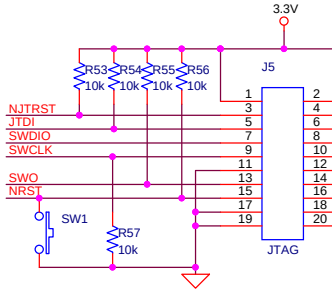
BUFFER

MISCELLANEOUS

Title	MISCELLANEOUS
Size: B	Document Number: DELIBERO_THESIS
Date: Tuesday, February 17, 2015	Sheet

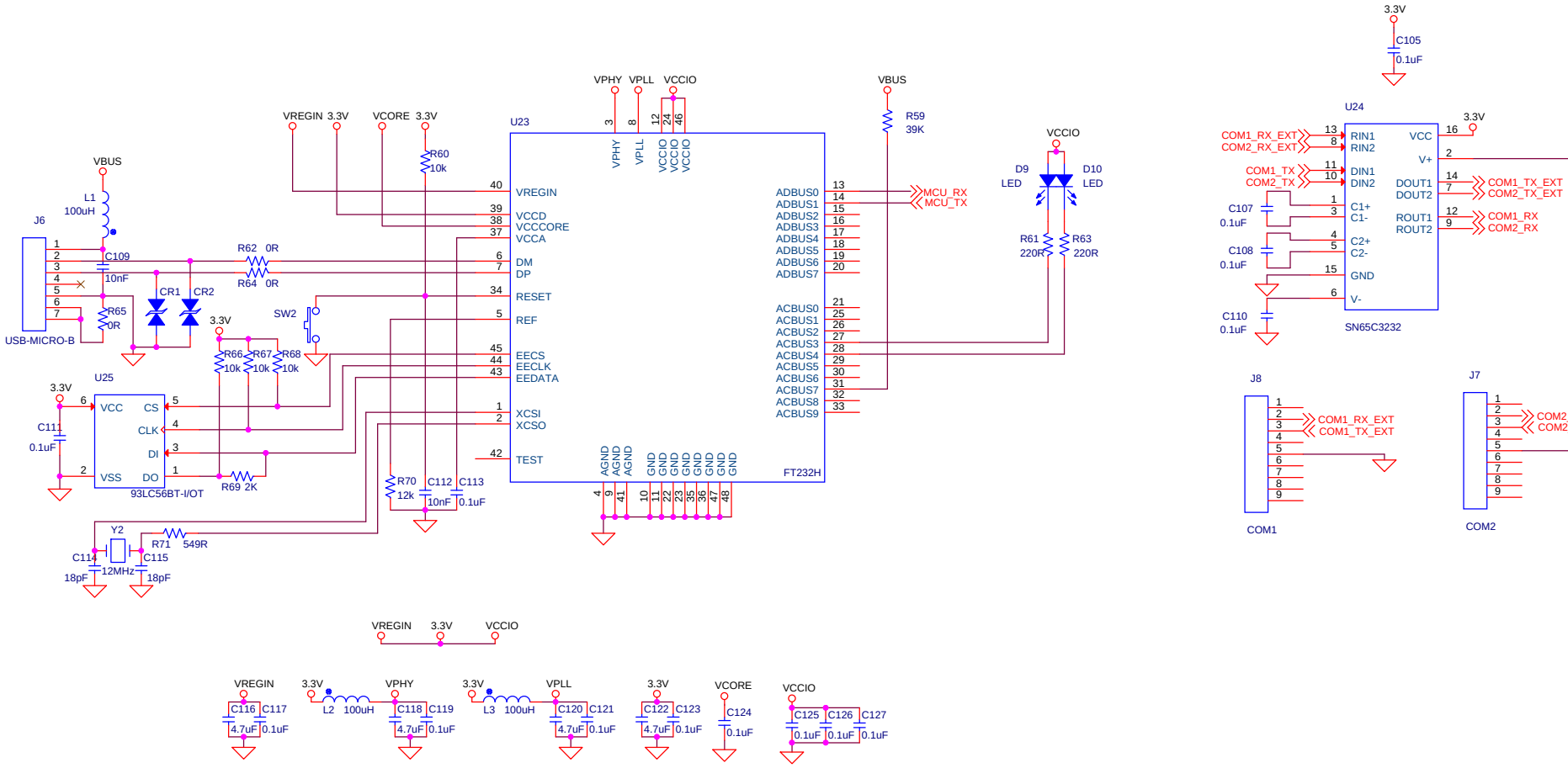






MCU I/O

Title: MCU I/O		
Size: B	Document Number: DELIBERO_THESIS	
Date: Tuesday, February 17, 2015	Sheet	



COMMUNICATIONS

Title	USB COMMUNICATIONS
Size: B	Document Number: DELIBERO_THESIS
Date: Tuesday, February 17, 2015	Sheet

References

[1] Relva C. Buchanan, editor. *Ceramic Materials for Electronics*. Marcel Dekker, 3 edition, June 2004.

[2] What are mica capacitors?, 2014.

[3] G W A Dummer. *Electronics Inventions and Discoveries*. Institute of Physics Publishing, 1997.

[4] Steven Ehret. *Instrumentation For Anodization and In-Situ Testing of Titanium Alloys for Capacitor Anodes*. Masters thesis, Case Western Reserve University, January 2012.

[5] Richard Fore. Understanding temperature coefficients of ceramics, January 2005.

[6] S. Fujishima. The history of ceramic filters. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, 47(1):1–7, Jan 2000.

[7] James M. Gleason. Steatite for high frequency insuation. In *Journal of the British Institution of Radio Engineers*. Institute of Radio Engineers, 1945.

[8] J. Ho, T.R. Jow, and S. Boggs. Historical introduction to capacitor technology. *Electrical Insulation Magazine, IEEE*, 26(1):20–25, January 2010.

[9] Brian Holman. *The Electrical Characterization of Tantalum Capacitors as MIS Devices*. ProQuest LLC, 2008.

[10] Capacitors.

[11] B. Jaffe, W.R Cook Jr., and H. Jaffe. *Piezoelectric Ceramics*. Adacemic Press Ince (London) Ltd, 1971.

[12] J.M.Herbert. *Ceramic Dielectrics in Capacitors*. Gordon and Breach Scientific Publishers, 1985.

[13] Jill Jonnes. *Empires of Light*. Random House, 2003.

[14] Learning about electronics.

[15] E. C. Levy. Complex-curve fitting. *Automatic Control, IRE Transactions on*, AC-4(1):37–44, 1959.

[16] An efficiency primer for switch-mode, dcdc converter power supplies, December 2008.

[17] Francis Merat Michael DeLibero, Steven Ehret. Instrumentation for the anodization and characterization of titanium electrodes for electrolytic capacitors. In *Energytech, 2012 IEEE*. IEEE, May 2012.

[18] Reem Malik Moshe Gerstenhaber. More value from your absolute value circuit. *Back Burner*, 44(04), 2010.

[19] Ming-Jen Pan and Clive A. Randall. A brief introduction to ceramic capacitors. *Electrical Insulation Magazine, IEEE*, 26(3):44–50, May 2010.

[20] Winfield Hill Paul Horowitz. *The Art of Electronics*. Cambridge University Press, 2 edition, 1989.

[21] Power factor and power factor correction.

[22] Ian Poole. Silver mica capacitor.

[23] S. Pooranchandra, B. Sasikala, and Afzal Khan. *Introduction to Electrical , Electronics and Communication Engineering*. FireWall Media, 2005.

[24] Krik K. Reed. Characterization of tantalum polymer capacitors, 2005.

[25] C.K. Sanathanan and J. Koerner. Transfer function synthesis as a ratio of two complex polynomials. *Automatic Control, IEEE Transactions on*, 8(1):56–58, Jan 1963.

[26] Sprague 50 year timeline.

[27] High voltage power supplies.

[28] Series ps300 high voltage power supplies.

[29] Electronic components - dipped mica capacitors.

[30] Ceramic capacitor, November 2014.

[31] Electrolytic capacitor.

[32] Silver mica capacitor, January 2014.