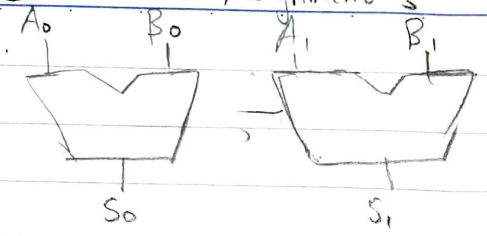
NO. Michael Lee
DATE

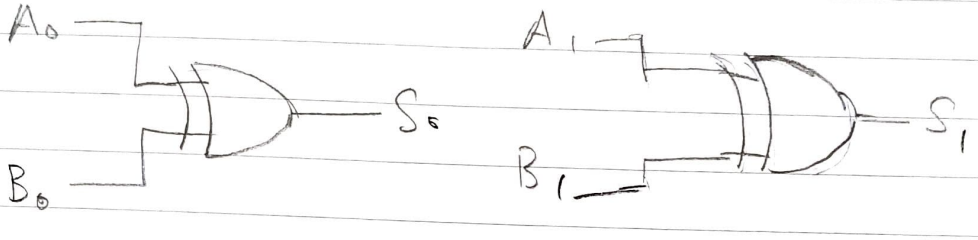
CSE 220 Assignment 3

1.



A_0	B_0	S_0
0	0	0
0	1	1
1	0	1
1	1	0

A_1	B_1	S_1
0	0	0
0	1	1
1	0	1
1	1	0

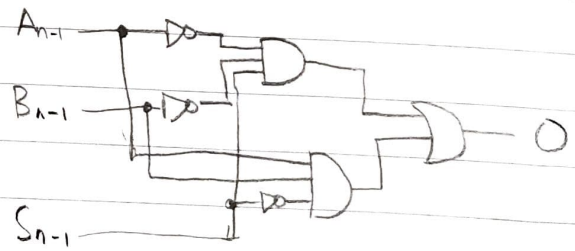


- Since the adders are half adders, they do not have a carry in which means less inputs, less circuitry / resistors, leading to less complexity. Thus it will have a faster performance than two full adders, but less functionality as it doesn't compute carry ins.

2. If the 2's complement is used, the most significant bit, S_{n-1} will tell if overflow occurred. If A_{n-1} and B_{n-1} are both same sign (0s or 1s) and S_{n-1} has opposite sign then overflow occurred.

A_{n-1}	B_{n-1}	S_{n-1}	O
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(0 = no over flow, 1 = overflow)



$$O = \overline{A_{n-1}}\,\overline{B_{n-1}}\,S_{n-1} + A_{n-1}\,B_{n-1}\,\overline{S_{n-1}}$$

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3. a) $-30.5 \rightarrow 30 = 011110 \Rightarrow -(0\,1111\,0100\,00)$

$0.5 = 100000$

$\rightarrow 1111\,0100\,0000 \rightarrow$ **FA0**

b) $16.25 \rightarrow 16 = 010000 \Rightarrow 0\,1000\,0010\,0000$

$0.25 = 010000$

$\rightarrow 0100\,0001\,0000 \rightarrow$ **810**

c) $-8.078125 \rightarrow 8 = 001000 \quad -(0\,0100\,0000\,101)$

$0.078125 \rightarrow 000101$

0.15625

$0.3125 \quad 1\,0100\,0000\,101$

0.625

$1.25 \quad =$ **A05**

0.5

1.0