CSE220 Assignment 2

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1. $-16 + 9$: $010000 + 001001$ → Overflow $01\,1001$

   $-27 + 31$: $011011 + 011111$ → Overflow $1\,1010$

   $-4 + 19$: $000100 \rightarrow 111011 \rightarrow 111100$; $111100 + 010011$ → no overflow $\$\ 0\,01111$

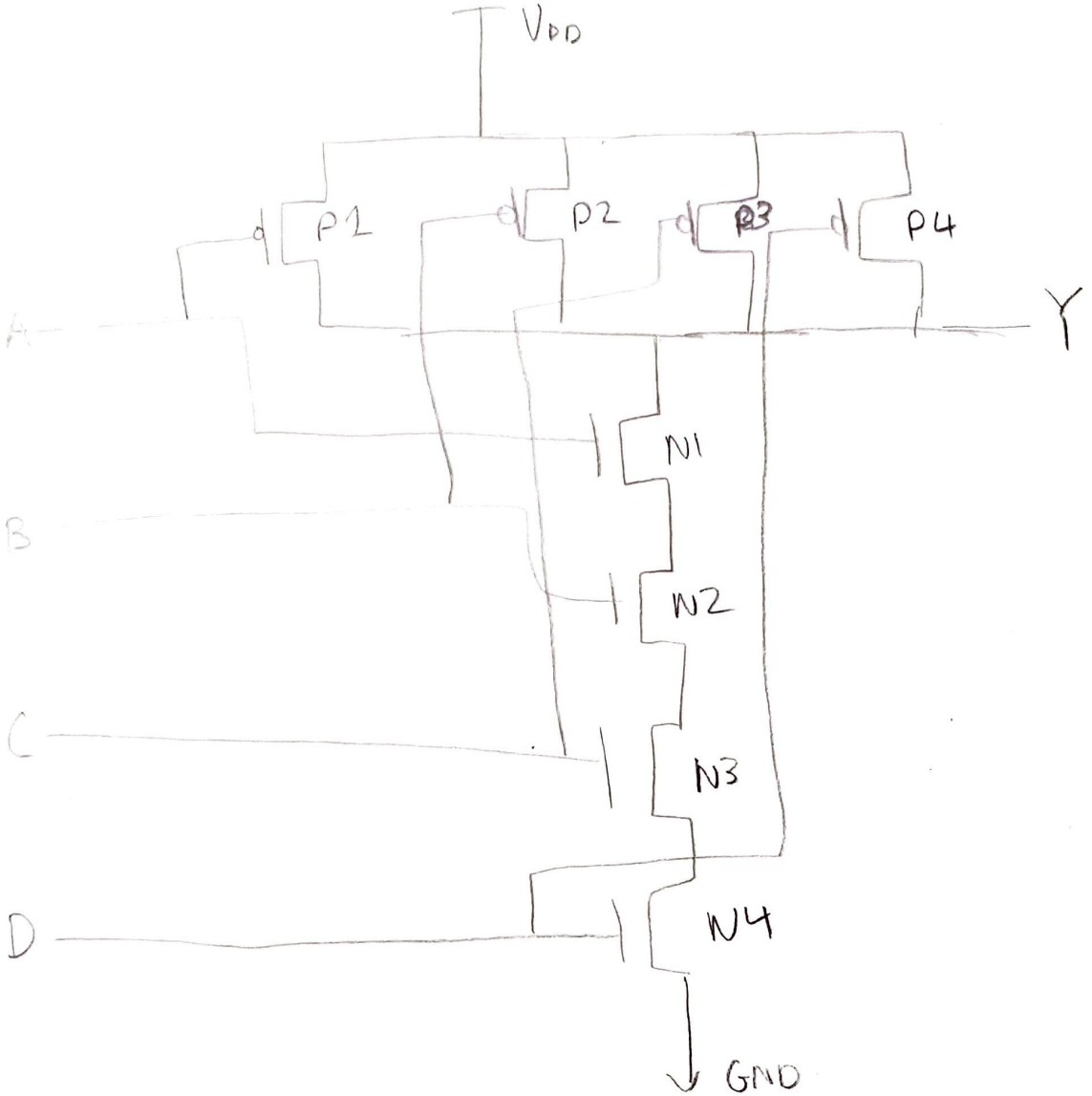
   $-32 + 3$: $100000 \rightarrow 011111 \rightarrow 100000$; $100000 + 000011$ → no overflow 100011

   $-16 + -1$: $010000 \rightarrow 101111 \rightarrow 110000$; $001001 \rightarrow 110110 \rightarrow 110111$ → no overflow $1\,100111$

   $-27 + -31$: $011011 \rightarrow 100100 \rightarrow 100101$; $011111 \rightarrow 100000 \rightarrow 100001$ → overflow $\$\ 000110$

2a. 4 input NAND

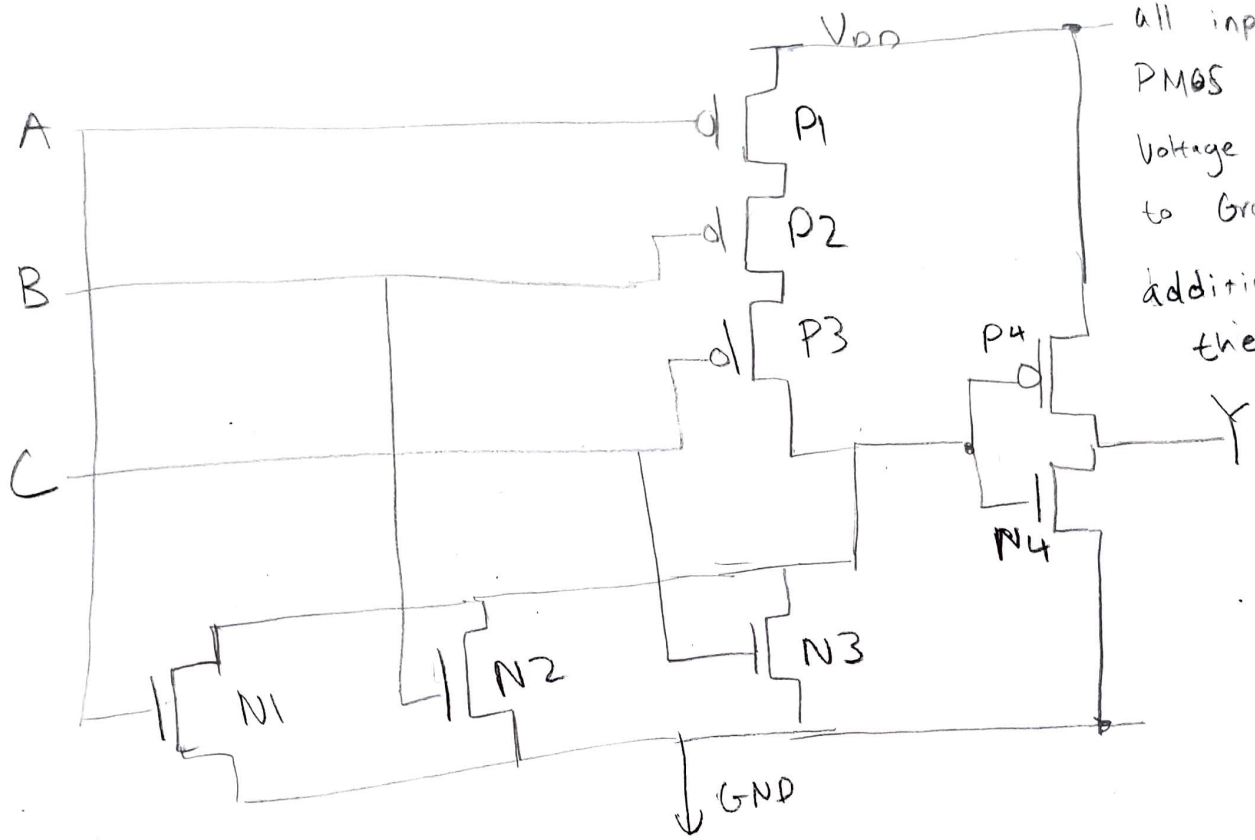
A	B	C	D	P1	P2	P3	P4	N1	N2	N3	N4	Y
0	0	0	0	ON	ON	ON	ON	OFF	OFF	OFF	OFF	1
0	0	0	1	ON	ON	ON	OFF	OFF	OFF	OFF	ON	1
0	0	1	0	ON	ON	OFF	ON	OFF	OFF	ON	OFF	1
0	0	1	1	ON	ON	OFF	OFF	OFF	OFF	ON	ON	1
0	1	0	0	ON	OFF	ON	ON	OFF	ON	OFF	OFF	1
0	1	0	1	ON	OFF	ON	OFF	OFF	ON	OFF	ON	1
0	1	1	0	ON	OFF	OFF	ON	OFF	ON	ON	OFF	1
0	1	1	1	ON	OFF	OFF	OFF	OFF	ON	ON	ON	1
1	0	0	0	OFF	ON	ON	ON	ON	OFF	OFF	OFF	1
1	0	0	1	OFF	ON	ON	OFF	ON	OFF	OFF	ON	1
1	0	1	0	OFF	ON	OFF	ON	ON	OFF	ON	OFF	1
1	0	1	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	1
1	1	0	0	OFF	OFF	ON	ON	ON	ON	OFF	OFF	1
1	1	0	1	OFF	OFF	ON	OFF	ON	ON	OFF	ON	1
1	1	1	0	OFF	OFF	OFF	ON	ON	ON	ON	OFF	1
1	1	1	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON	0



As it is an NAND circuit, only when NMOS transistors are all on can a connection be made with ground, hence why NMOS transistors are in series. If only 1 PMOS transistor is on (an input of one zero) there is a connection with voltage; hence why they are parallel.

2b. three input OR Gate

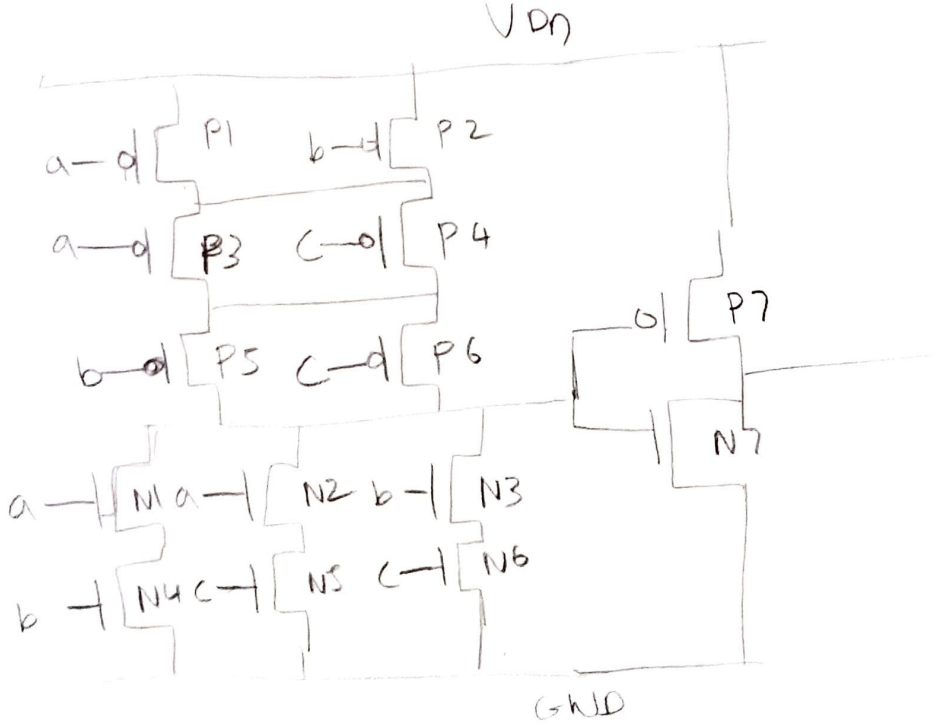
A	B	C	P1	P2	P3	N1	N2	N3	Y	P4	N4	
0	0	0	ON	ON	ON	OFF	OFF	OFF	0	OFF	ON	
0	0	1	ON	ON	OFF	OFF	OFF	ON	1	ON	OFF	
0	1	0	ON	OFF	ON	OFF	ON	OFF	1	ON	OFF	
0	1	1	ON	OFF	OFF	OFF	ON	ON	1	ON	OFF	
1	0	0	OFF	ON	ON	ON	OFF	OFF	1	ON	OFF	
1	0	1	OFF	ON	OFF	ON	OFF	ON	1	ON	OFF	
1	1	0	OFF	OFF	ON	ON	ON	OFF	1	ON	OFF	
1	1	1	OFF	OFF	OFF	ON	ON	ON	1	ON	OFF	



As it is a OR gate, the out put is zero only when all inputs are zeros. Due to PMOS being connected to voltage and NMOS being connected to Ground, there are two additional transistors to reverse the output

3.

A	B	C	P1	P2	P3	P4	P5	P6	P7	N1	N2	N3	N4	N5	N6	N7	q
0	0	0	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	0
0	0	1	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	0
0	1	0	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	0
0	1	1	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON	OFF	1
1	0	0	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	0
1	0	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
1	1	0	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	1
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	1



With two or more inputs of 1s, it produces an output of 1, Else it produces 0.