CSE-220: Systems Fundamentals I

Assignment 3. Due on 22 April 2021

Solutions are to be scanned or photographed and submitted by email by 5:00PM of the due date. Diagrams should be drawn neatly.

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1. [20pts] Suppose we have to design a 2-bit adder that but **without** using full adders. The inputs of the adder are A_1A_0 and B_1B_0; and the outputs are S_1S_0.
   - Give a truth table for the 2-bit adder.
   - Give a neat gate-level logic diagram for the adder.
   - Compare the adder, in terms of cost and performance, with a 2-bit adder made up of two full adders.

2. [10pts] Suppose we are to add two signed n-bit numbers, $A_{n-1}A_{n-1}\cdots A_0$ and $B_{n-1}B_{n-1}\cdots B_0$, with result $S_{n-1}S_{n-1}\cdots S_0$. For these operand and results:
   - How could we determine whether or not overflow has occured?
   - Give a logic expression and gate-level circuit for overflow detection. (The adders described in Chapter 5 of the textbook, and discussed in class, do not have overflow detection.)

3. [10pts] Exercise 5.26 of the textbook. (Show **all** the steps in obtaining the answer.)