Mats Leis

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Education

Western University, BESc in Electrical and AI Systems Engineering — Expected May 2029

GPA: 3.48/4.00
Awards: Dean's List, Rothwell Leadership Award, Computer Science Award, McPherson Shield
Technical Skills: CAD, PCB Design and Simulation, Java, ESP32, Soldering, 3D Printing, FPGA Programming

Experience

Customer Support/Sales & Assembly, Quoted Tech — May – August 2025

- Addressed 100+ B2C inquiries daily, providing comprehensive product knowledge and advising clients on optimal custom PC configurations.
- Built 6–8 custom PCs daily with a focus on high-quality assembly and cable management.
- Coordinated with the assembly team to ensure customer needs were met, including relaying progress updates and custom installations.

Projects

Western Sunstang | Driver Controls Subteam — January 2025

- Designed and led the transition from Nucleo-based prototyping to a fully custom STM32 driver control PCB, serving as the primary interface between driver inputs, vehicle powertrain, and safety-critical CAN networks.
- Engineered a robust CAN communication system with an STM32 microcontroller and transceiver, including impedance-aware routing, selectable 120 Ω termination, and physical-layer considerations to maintain signal integrity under vibration and extended trace lengths.
- Designed a 12 V $\rightarrow$ 3.3 V power architecture using switching regulation, bulk capacitance, and decoupling networks to ensure stable, low-noise operation for logic and peripheral domains.
- Implemented a four-layer PCB stackup with dedicated power and ground planes to minimize EMI, reduce return path impedance, and shield sensitive logic from noise generated by onboard switching regulators.
- Integrated USB–UART communication, SWD debugging, and programmable onboard diagnostic LEDs to support efficient firmware development, validation, and fault isolation.
- Applied Design for Manufacturability (DFM) principles under student-team constraints, prioritizing hand-solderable footprints and balancing PCB expansion against routing complexity and parasitic effects.

Moore FSM Sequence Detector on FPGA — November 2025

- Designed and implemented a Moore FSM-based sequence detector capable of identifying specific binary patterns in high-speed bit streams
- Optimized state assignments using multiple strategies (adjacency rules and Gray code) to minimize logic gate count and reduce overall circuit cost.
- Derived state diagrams, state tables, and logic equations, then implemented the design structurally using flip-flops and logic gates in Quartus.
- Integrated the system with a shift register and FPGA hardware to validate functional sequence detection through real-time testing and simulation.

Line Following Rescue Robot | Robocup Jr. (Team Canada) — September 2022 – May 2024

- Competed at the Robocup Jr. World Competition, where the robot successfully demonstrated its ability to autonomously navigate a complex modular course, follow a line and overcome obstacles.
- Applied expertise in CAD software (Fusion 360, SolidWorks) and rapid prototyping techniques (laser cutting, 3D printing) to iterate the robot's design from ideation to final build.
- Developed custom-moulded silicone tires that allowed the robot to climb ramps more than twice as steep as the original tires.