Michael L. Lewis

Home
2046 Badger Glen
Escondido, CA 92029
Phone: 760-735-9147
FAX: 419-793-1006
E-mail: lewis-michael@home.com
URL: members.home.com/susulewis/mikes_career.html

Work
15050 Avenue of Science, Suite 200
San Diego, CA 92128
Phone: 858-613-7935
FAX: 858-676-6896
E-mail: uml@cypress.com
URL: www.cypress.com/usb

Education

1987-1989, 1992-1994 — BS — California State University, Fresno. Electrical Engineering
G.P.A: 3.75 (on 4.0 scale)
Graduation Date: December, 1994

1995-1996 — MS — University of California, Santa Barbara. Computer Engineering
G.P.A: 3.53 (on 4.0 scale)
Graduation Date: December, 1996

Skills

Programming & Scripting Languages…. Verilog, VHDL, Awk, Sed, Perl, HTML, 8051 Assembly

Computer Aided Design…… Cadence (Verilog-XL and SignalScan Waveform Viewer,) ModelTech ModelSim, Synopsys (Design Compiler/Analyzer, Test Compiler/ATPG, Logic Modelling,) Xilinx Foundation

Specifications..……..…… IEEE Std. 1149.1 (Boundary Scan), PCI 2.1, USB 1.1, USB 2.0

Technical Experience

1999-Present…… Large-team, small-team, multi-site, and solo engineering products and tasks include:

1) *USB 1.1 Cost-Reduction ASIC:* Full-system functional verification and regression, scan vector generation, test engineering liason.
2) *USB 2.0 Bus Functional Models (Host and Monitor):* Behavioral design, verification, testbench enhancements (including packet/transaction-based tasks, and text I/O processing,) documentation, and corporate-wide integration (used on four projects to date.)
3) *USB 2.0 Integrated Microcontroller Peripheral:* RTL design (IP used on four projects to date,) full-system functional verification and regression, Synopsys library model generation, scan vector generation, and documentation. Three patents filed.
4) *USB 1.1 IP Transfer:* provided customer with IP-quality database, documentation, electronic transfer, on-site training, design and verification assistance.
5) *Bluetooth Integrated Microcontroller:* USB-side functional verification, testbench generation, and documentation.

Cypress Semiconductor, Interface Products Division. San Diego, CA

1997-1999..……. Large-team, small-team and solo engineering products and tasks include:

1) *100K-gate Multi-bus Interface ASIC:* RTL design, testbench generation, functional verification, and documentation.
2) *Low-latency Signal Processing Module:* HW/SW integration and test, work-around solutions, die-level hardware work-arounds with focused ion beam technology, avoided costly ASIC re-spins, schedule delays, and late customer deliveries.
3) *High-speed Parallel-to-Serial Bus Interface FPGAs (Master, Slave, and Monitor):* RTL design, testbench generation, functional verification, synthesis, place and route, timing analysis and simulation, documentation .

TRW, Avionics Systems Division. San Diego, CA.

1996……. Contracted in the design process of a PCI-FDDI interface ASIC for a network interface card. Tasks included VHDL design, simulation and verification, and documentation. *Rockwell Network Systems. Santa Barbara, CA*

1994……. Performed quality assurance, product testing, RMAs, manufacturing, field applications, and customer technical support for telemetry monitoring engineering firm. *Digital Prototype Systems. Fresno, CA*

Publications

"Adopting Software Methods for VHDL Design" — *Integrated Systems Design.* October, 1999.

"Testing a super-fast part on a super-cheap tester" — *Cypress International Technical Conference.* June, 2000