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EEL 4712

Lab 4 prelab report

Top level summary;

The top level uses the clock generator to drive both the counter and gray code fsm

In order to output the state bits to the 7 segment led configuration specified lower in the VHDL file for the top level entity. The clock divider is fed into the clock generator after the oscillations of the 50 Mhz signal has been dampened to 1000 Hz. These components together will create and drive the top level to display the FSM on the output LED’s.