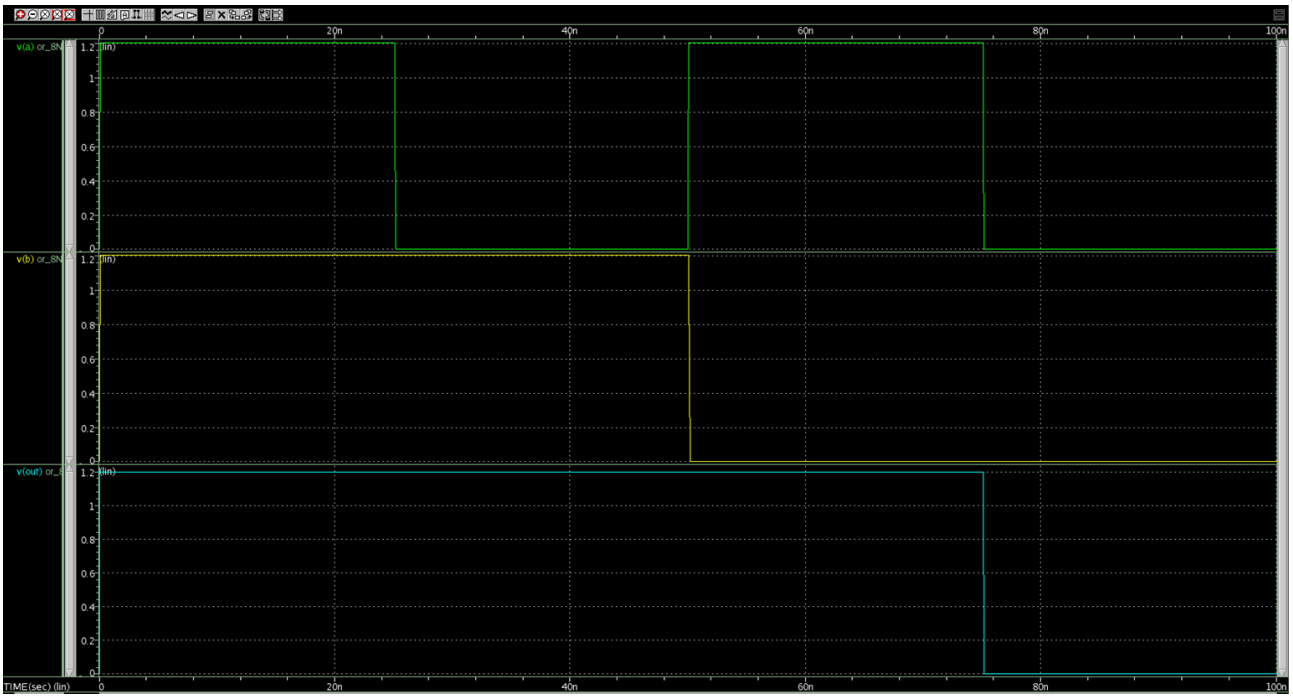
1) HSPICE

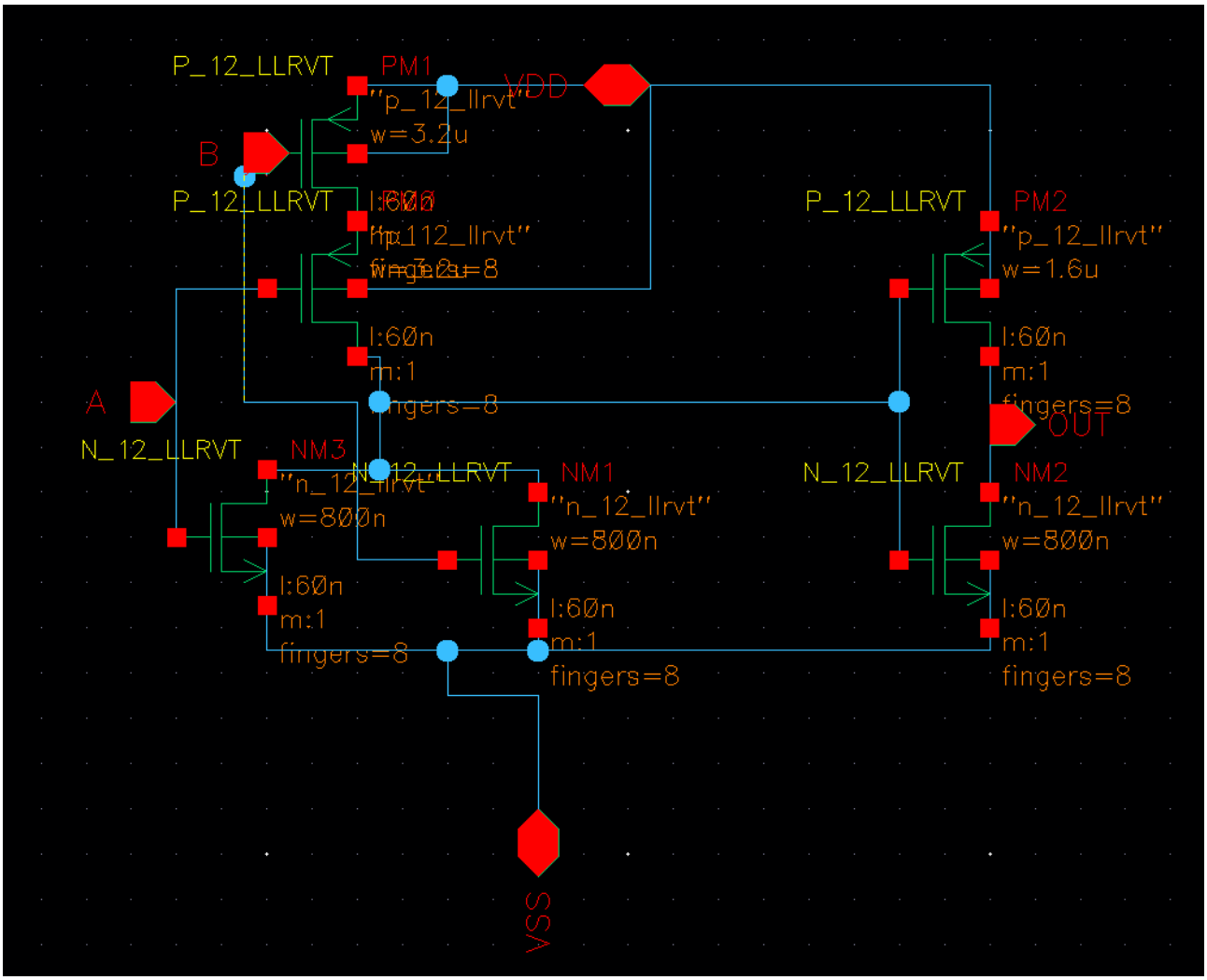
or_8N

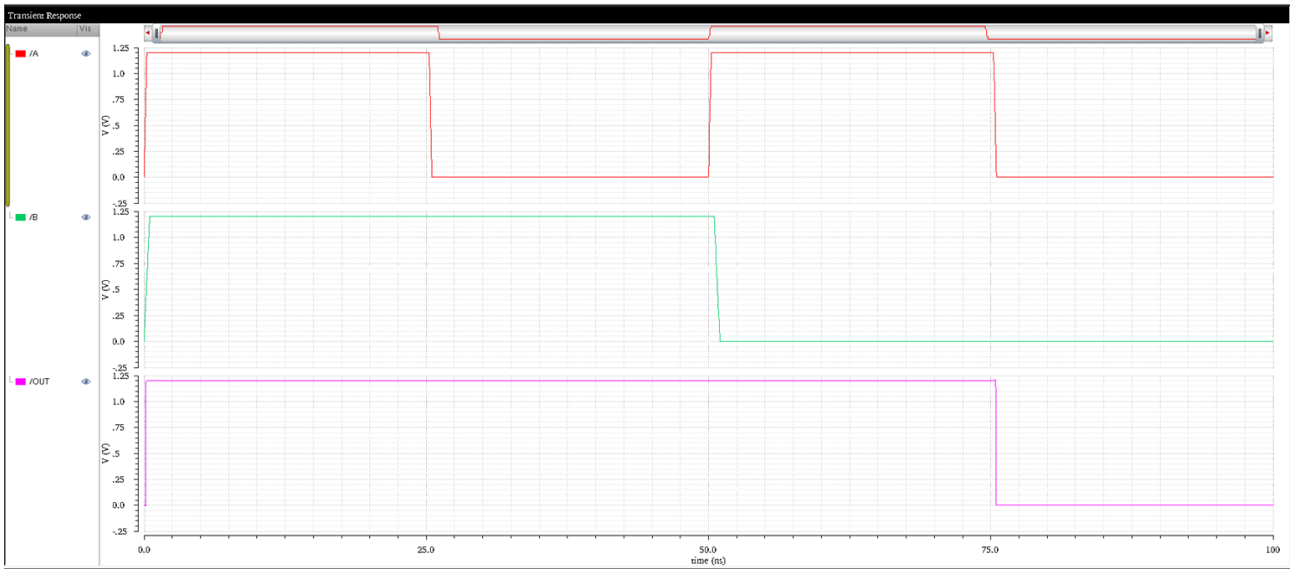
```
.lib
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_rvt12
.PARAM
.OPTION POST
.GLOBAL vss! vdd!

.model nm NMOS
.model pm PMOS

MP1 p b vdd! vdd! pm W=3200n L=60n NF=8
MP2 out1 a p vdd! pm W=3200n L=60n NF=8
MP3 out out1 vdd! vdd! pm W=1600n L=60n NF=8
MN1 out1 a gnd! gnd! nm W=800n L=60n NF=8
MN2 out1 b gnd! gnd! nm W=800n L=60n NF=8
MN3 out out1 gnd! gnd! nm W=800n L=60n NF=8
VVdd vdd! 0 1.2v
VGnd gnd! 0 0v
VA a gnd! pulse( 0 1.2 0 0.1n 0.1n 25n 50n)
VB b gnd! pulse( 0 1.2 0 0.1n 0.1n 50n 100n)
.tran 1n 100n

.END
```

SIMULATION OR GATE

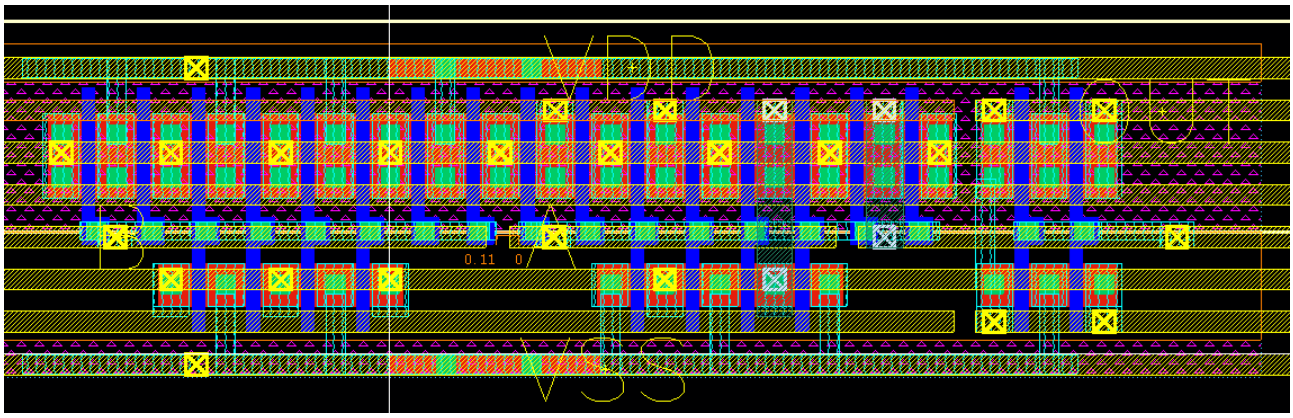


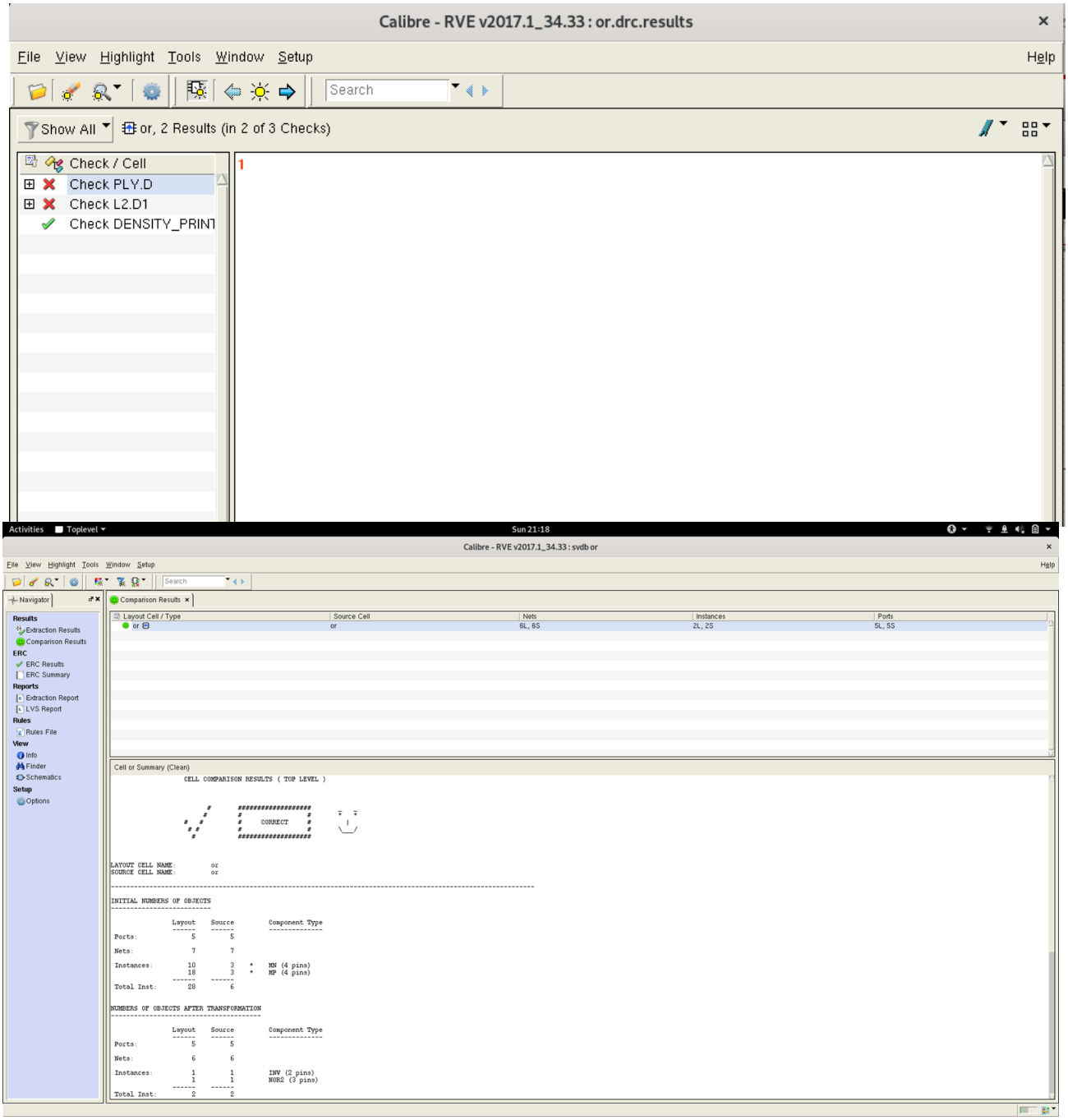
2)Schmatic : VDD VSS A B OUT as pins





3,4,5 LAYOUT DRC LVS PEX





attached full pex in drive
dimentions in last figue is (1.4(height)X(5.06(diffucion of pmos nor gate to diffusson of pmos inverter)))