

1) HSPICE

or_8N

.lib

"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC000000A_B11/Models/Hspice/l65ll_v1

81.lib" tt_ll_rvt12

.PARAM

.OPTION POST

.GLOBAL vss! vdd!

.model nm NMOS

.model pm PMOS

MP1 p b vdd! vdd! pm W=3200n L=60n NF=8

MP2 out1 a p vdd! pm W=3200n L=60n NF=8

MP3 out out1 vdd! vdd! pm W=1600n L=60n NF=8

MN1 out1 a gnd! gnd! nm W=800n L=60n NF=8

MN2 out1 b gnd! gnd! nm W=800n L=60n NF=8

MN3 out out1 gnd! gnd! nm W=800n L=60n NF=8

VVdd vdd! 0 1.2v

VGnd gnd! 0 0v

VA a gnd! pulse(0 1.2 0 0.1n 0.1n 25n 50n)

VB b gnd! pulse(0 1.2 0 0.1n 0.1n 50n 100n)

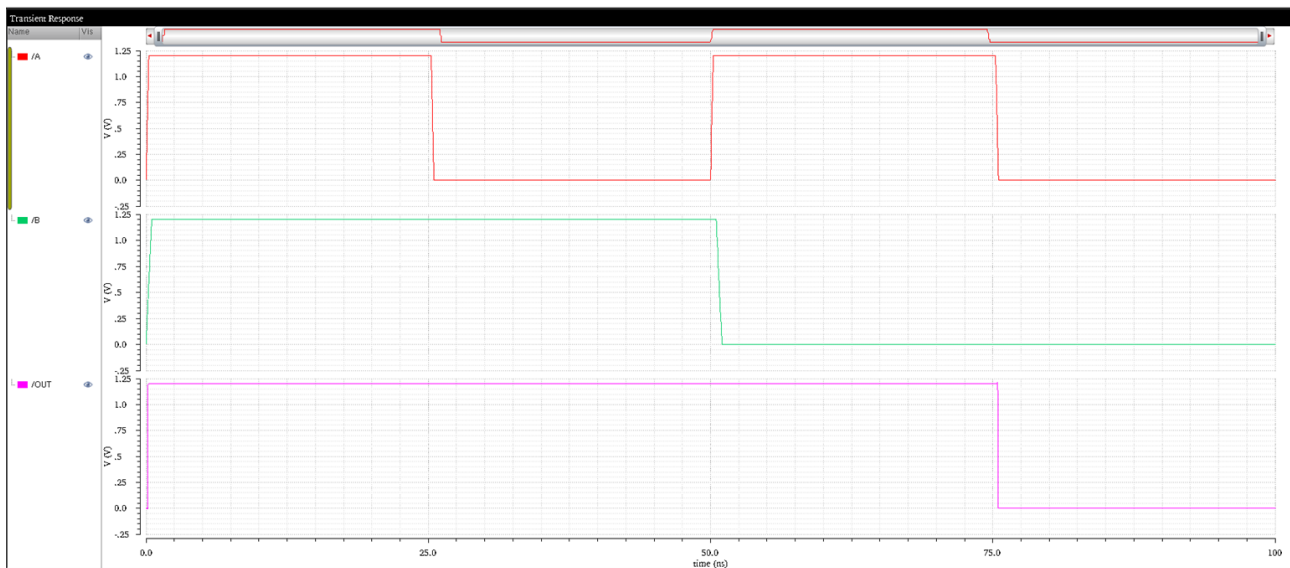
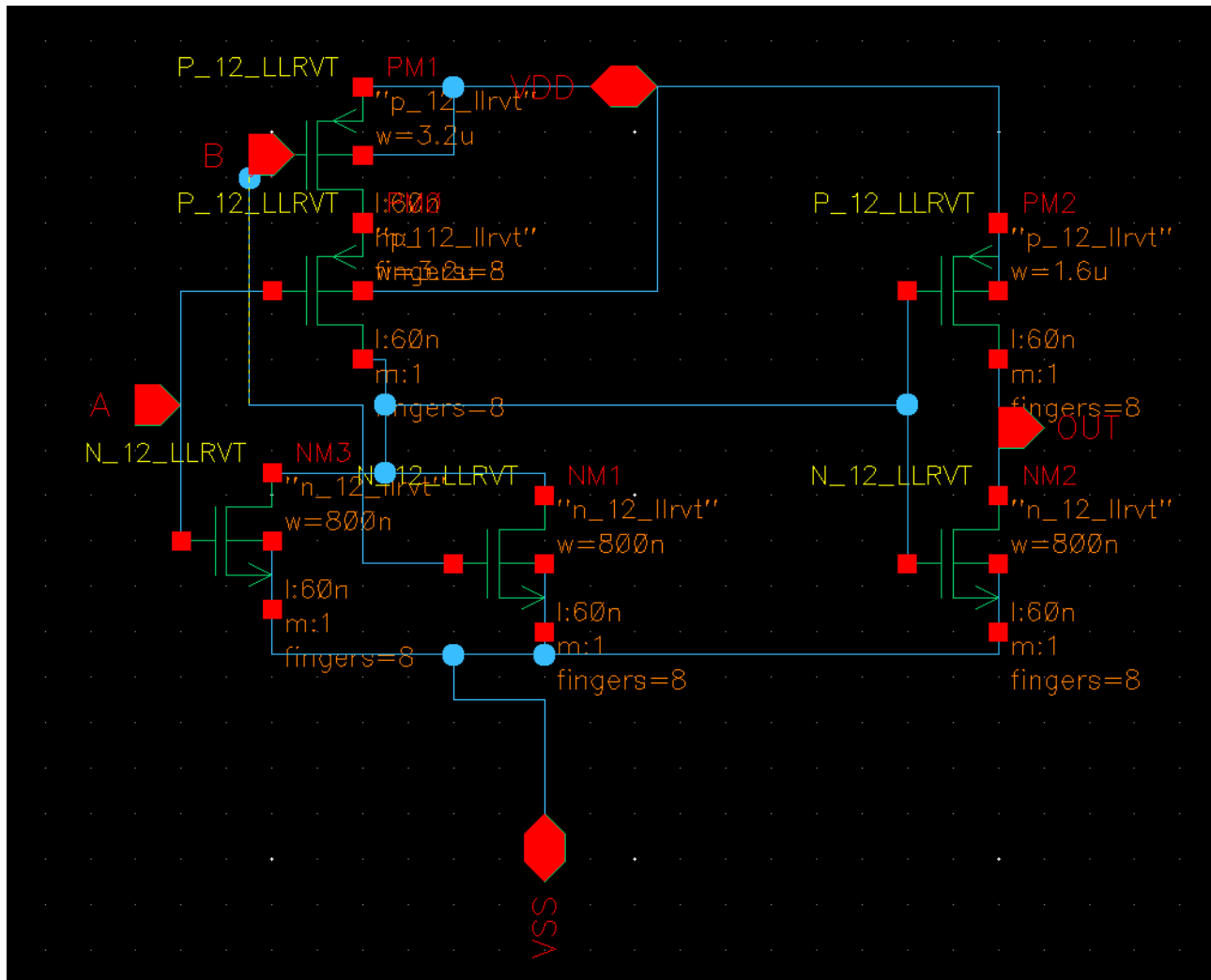
.tran 1n 100n

.END

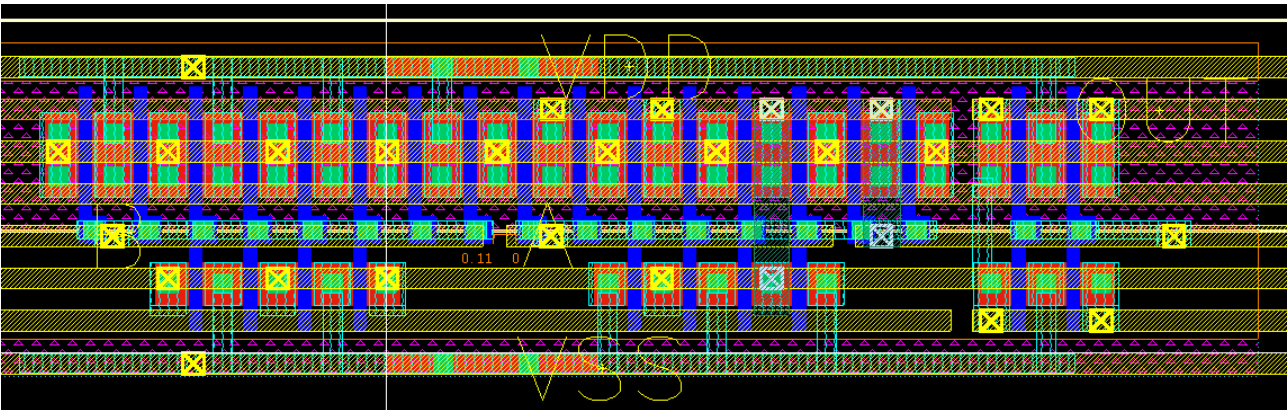
SIMULATION OR GATE



2)Schematic : VDD VSS A B OUT as pins



3,4,5 LAYOUT DRC LVS PEX



Calibre - RVE v2017.1_34.33 : or.drc.results

FileViewHighlightToolsWindowSetup

Help

Search

or, 2 Results (in 2 of 3 Checks)

Check / Cell

Check PLY.D

Check L2.D1

Check DENSITY_PRINT

1

ActivitiesToplevel

Sun 21:18

Calibre - RVE v2017.1_34.33 : svdb or

Help

Navigator

Results

Extraction Results

Comparison Results

ERC

ERC Results

ERC Summary

Reports

Extraction Report

LVS Report

Rules

Rules File

View

Info

Finder

Schematics

Setup

Options

Comparison Results

Layout Cell / Type

Source Cell

Nets

Instances

Ports

or

or

6L, 6S

2L, 2S

5L, 5S

Cell or Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

Layout Cell Name

Source Cell Name

or

or

INITIAL NUMBERS OF OBJECTS

| | Layout | Source | Component Type |
|-------------|--------|--------|----------------|
| Ports: | 5 | 5 | |
| Nets: | 7 | 7 | |
| Instances: | 10 | 3 | • NW (4 pins) |
| | 18 | 3 | • MP (4 pins) |
| Total Inst: | 28 | 6 | |

NUMBERS OF OBJECTS AFTER TRANSFORMATION

| | Layout | Source | Component Type |
|-------------|--------|--------|----------------|
| Ports: | 5 | 5 | |
| Nets: | 6 | 6 | |
| Instances: | 1 | 1 | • INW (2 pins) |
| | 1 | 1 | • NWS (2 pins) |
| Total Inst: | 2 | 2 | |

attached full pex in drive
dimentions in last figue is (1.4(height)X(5.06(diffucion of pmos nor gate to diffusson of pmos
inverter)))

[illegible]