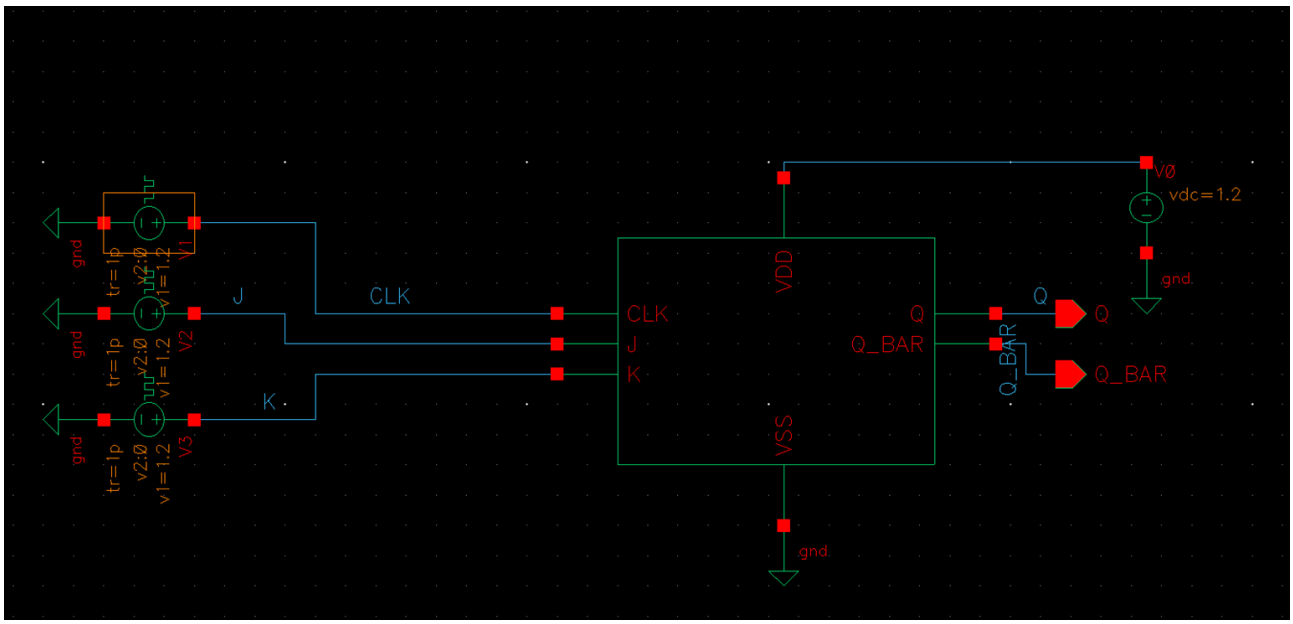
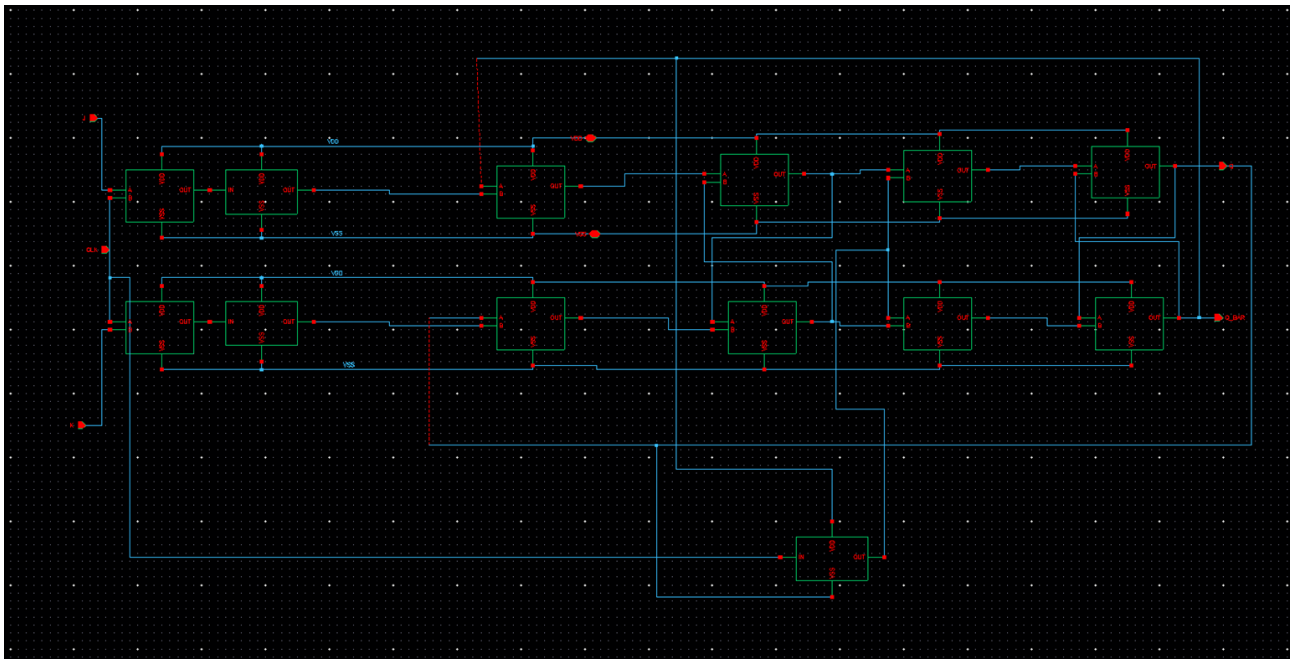
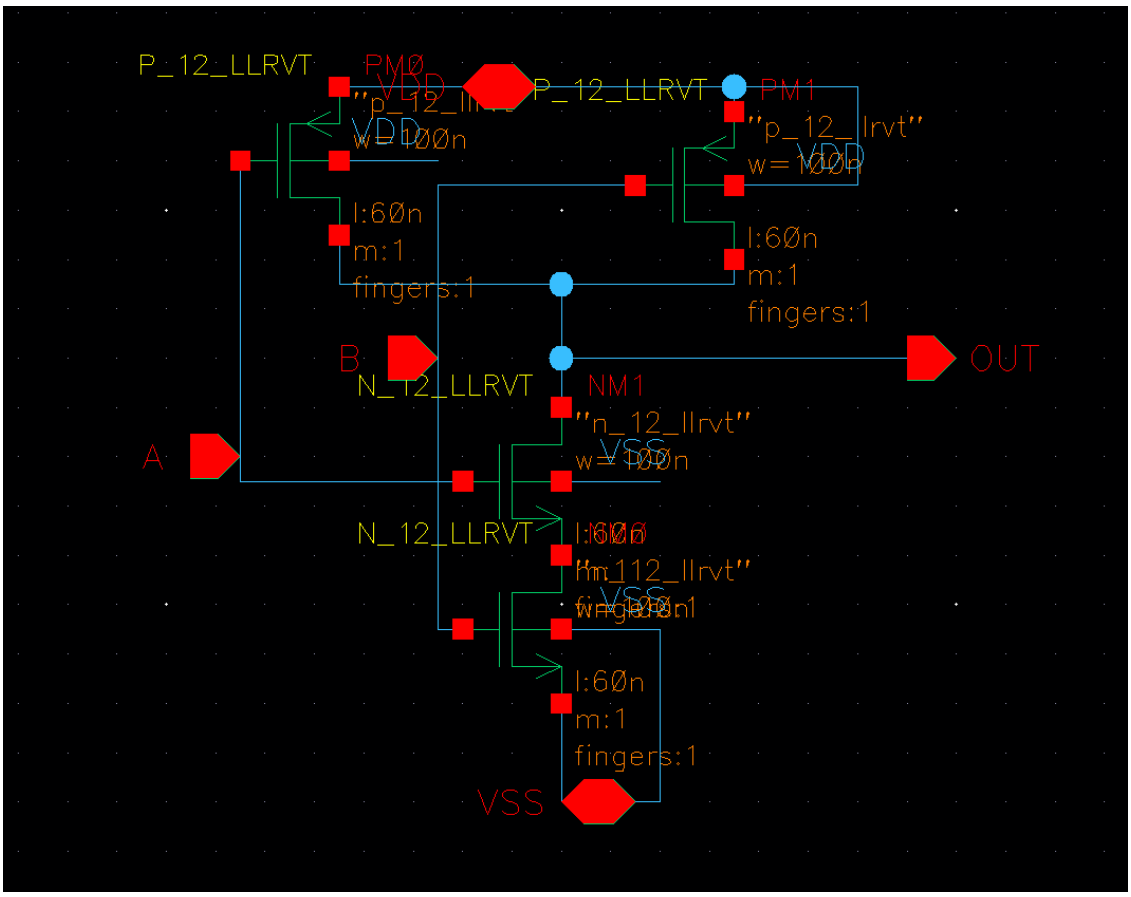


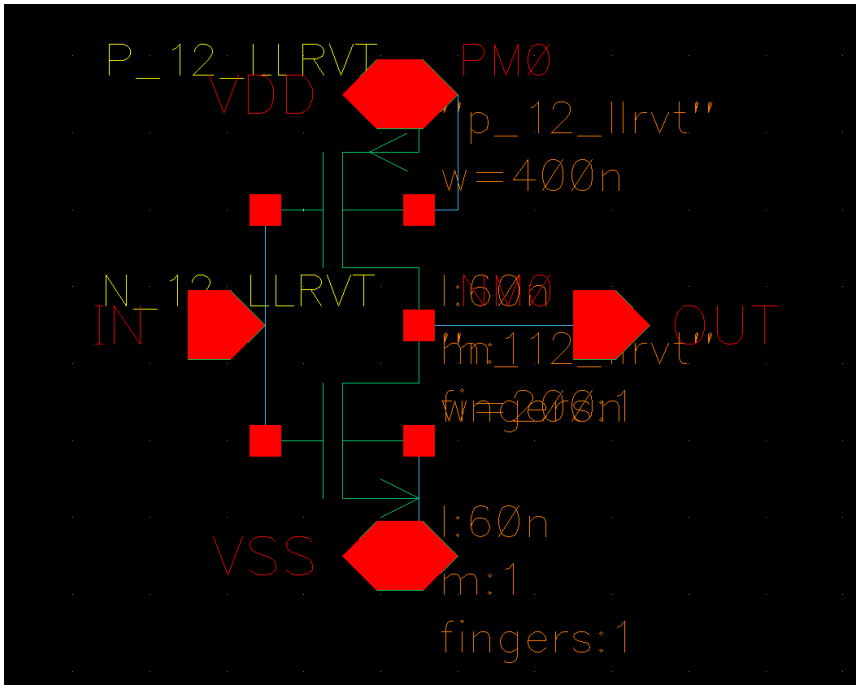
JK SCHEMATIC AND SYMBOL

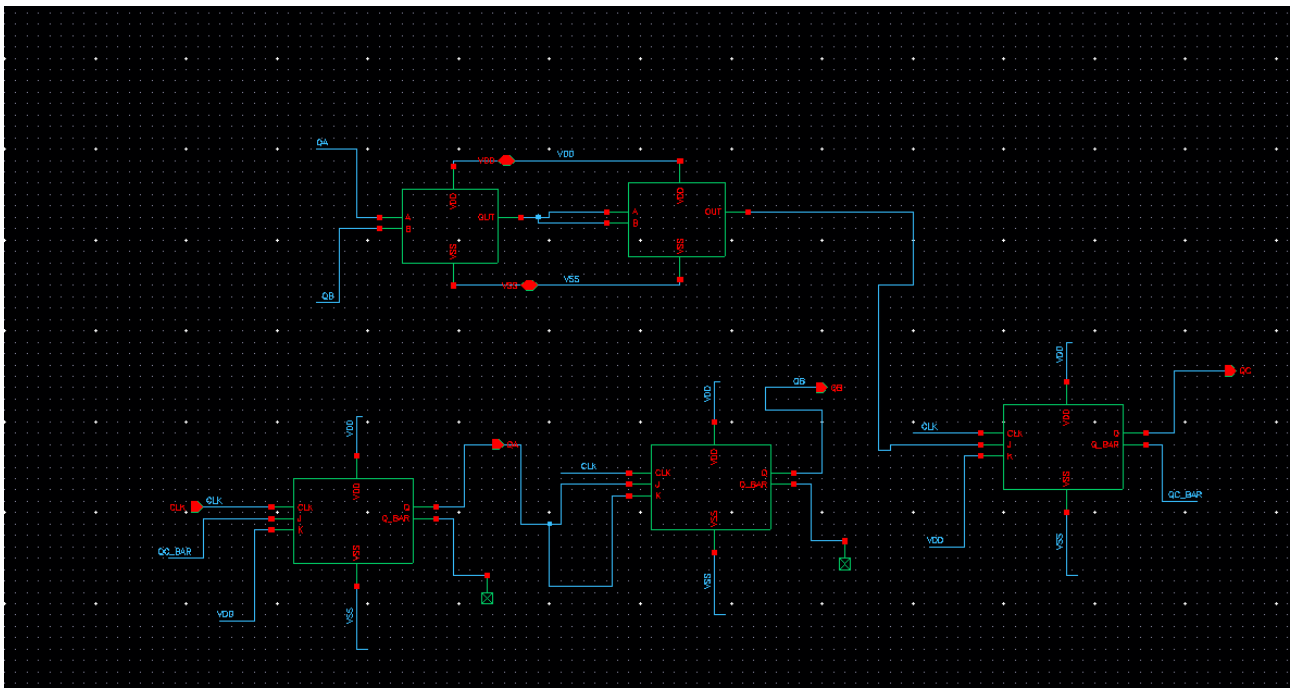




AND

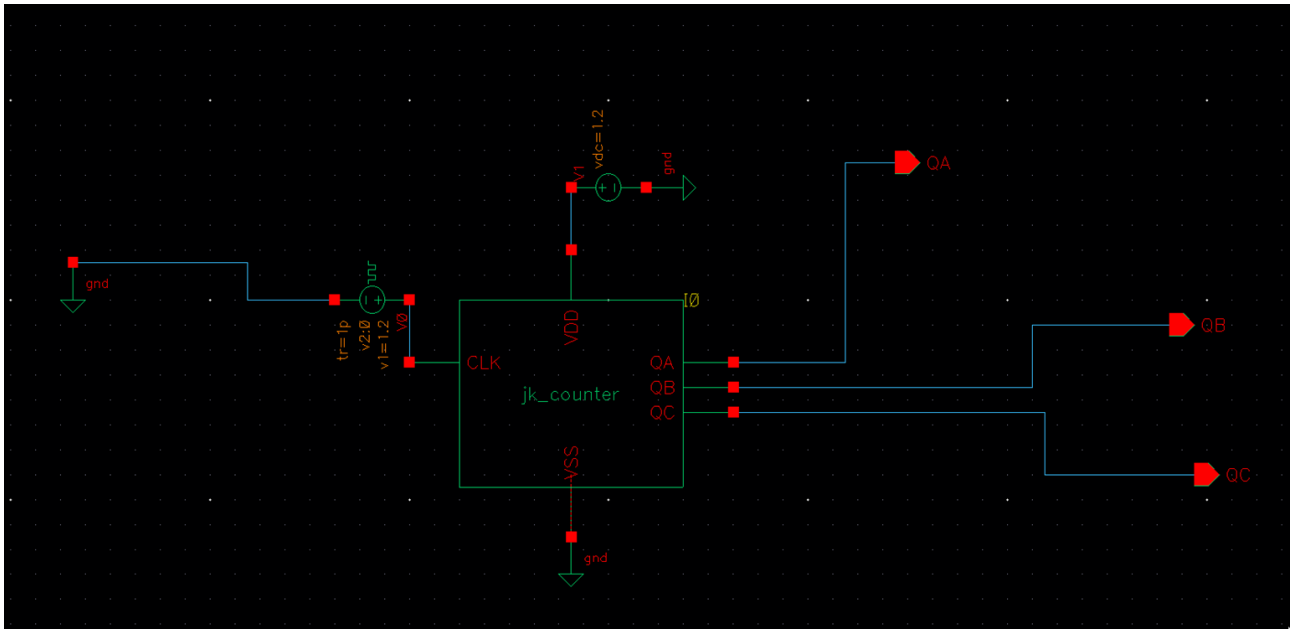
INVERTER





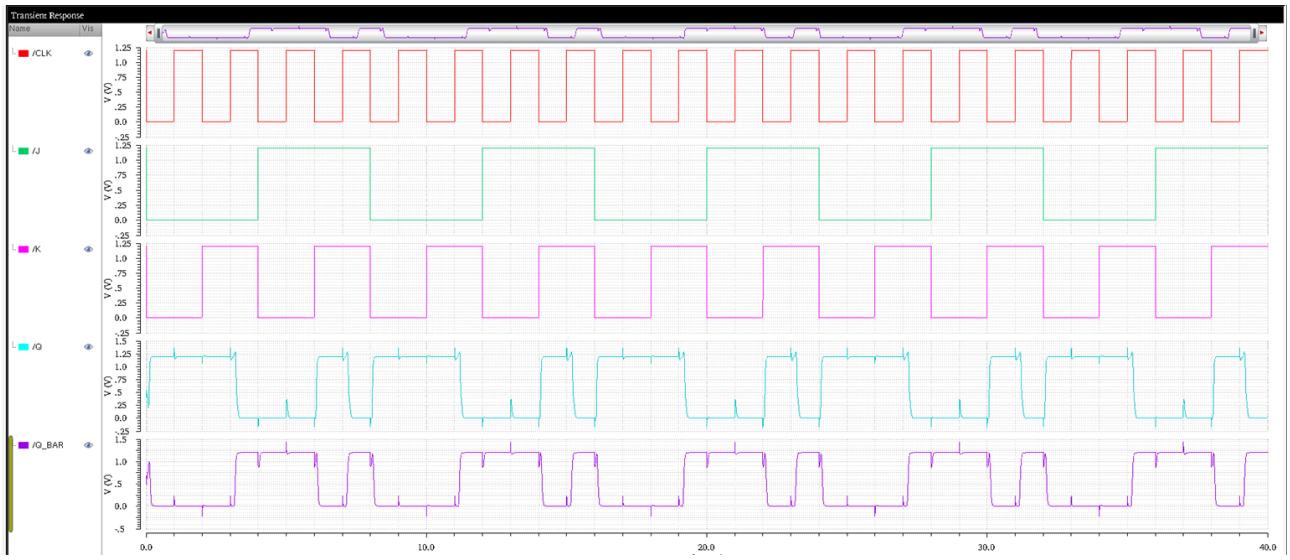
COUNTER SCHEMATIC

SYMBOLFOR COUNTER

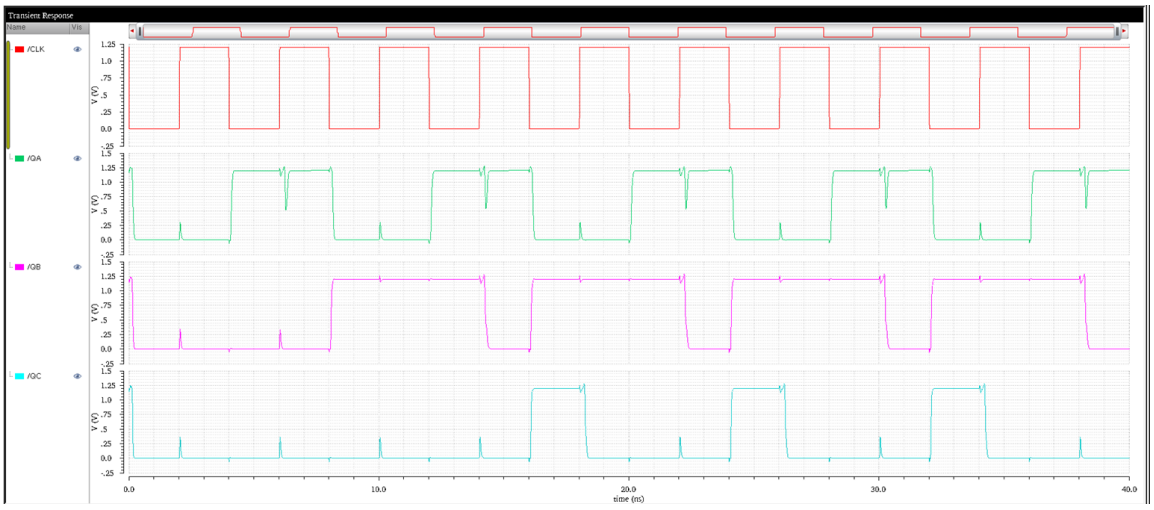


USING NAND GATES AND INVERTER

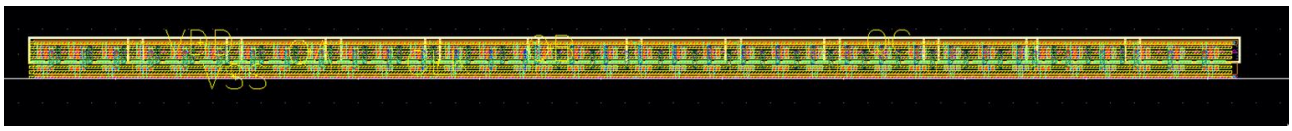
OUTPUT OF JK



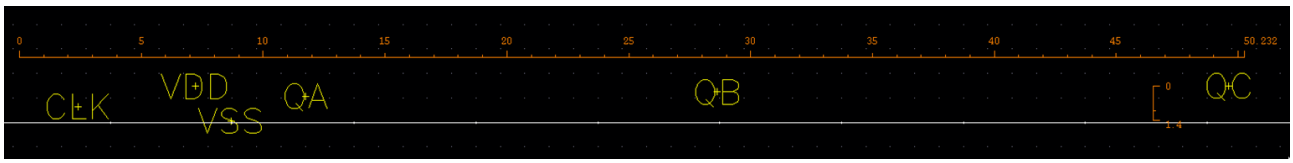
OUTPUT FOR COUNTER



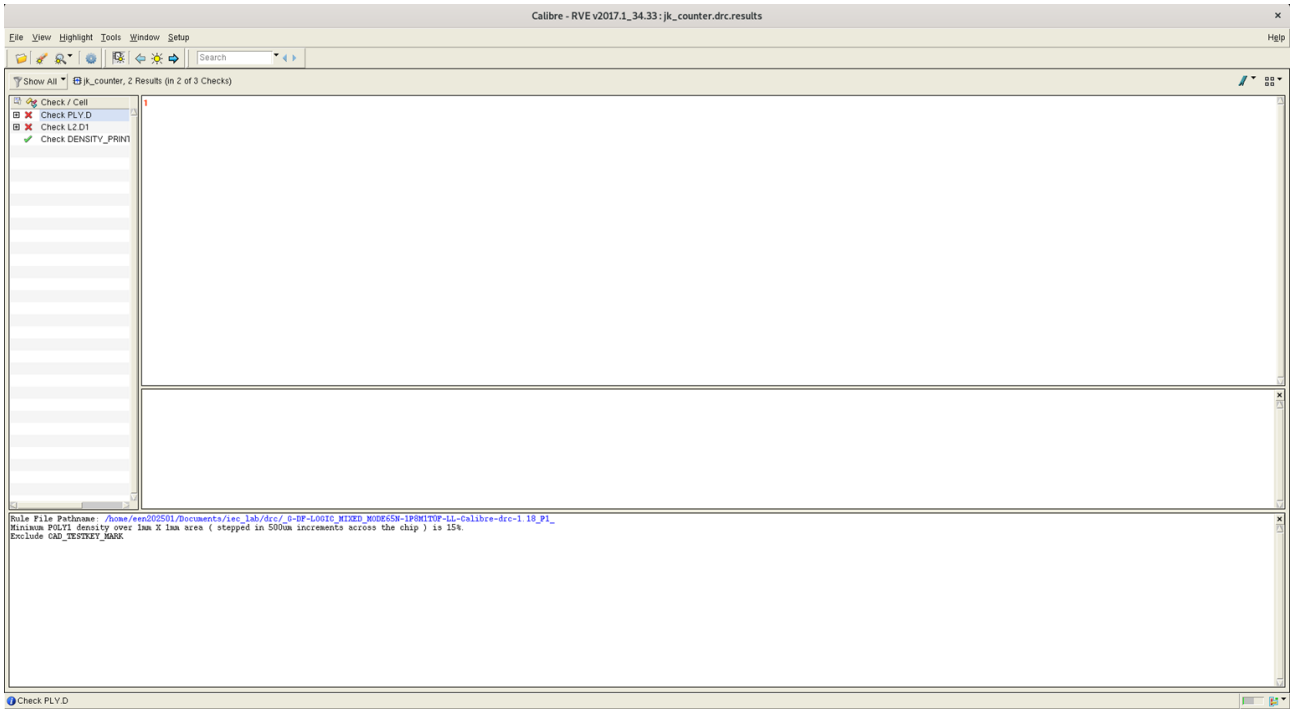
LAYOUT



SIZES



DRC



HSPICE

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL

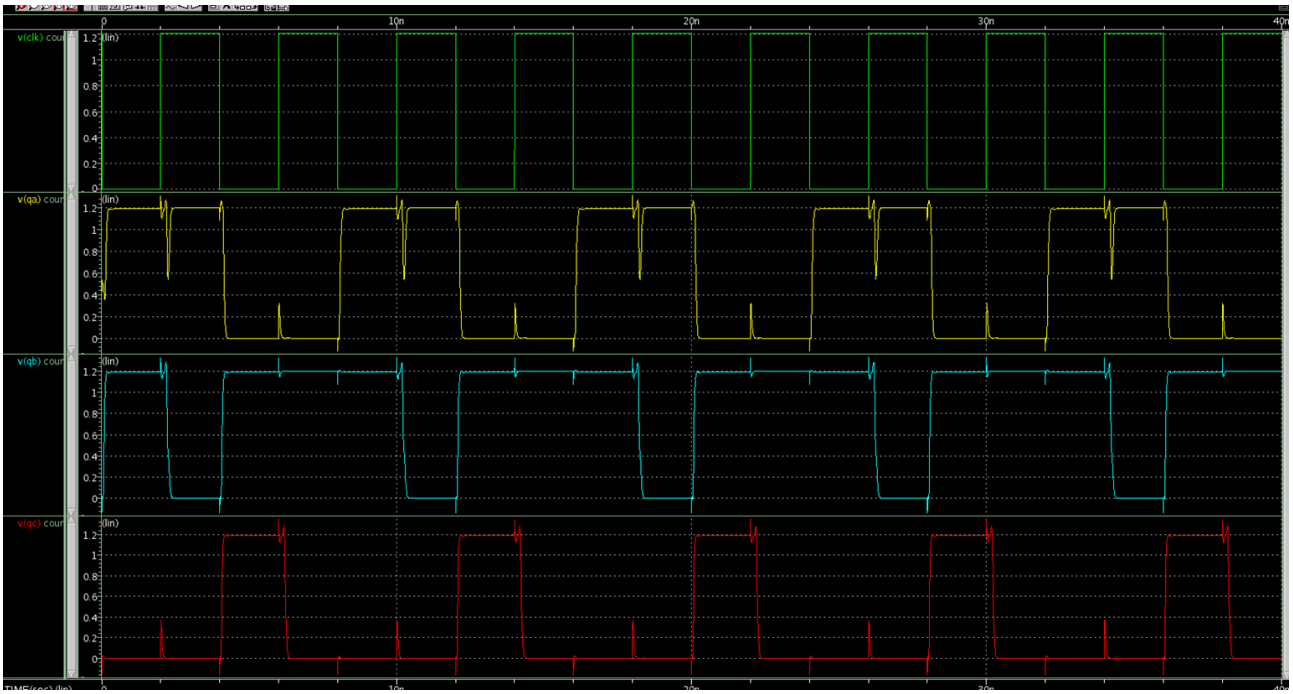
+ PSF=2
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_rvt12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_hvt12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_lvt12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_io18
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_io25od33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_io33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt12_bpw
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt18
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt18_bpw
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt25od33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt25od33_bpw
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_nvt33_bpw
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_bjt
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_diode
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_momcaps

.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_ncap12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_ncap18
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_ncap25
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_ncap33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_pcap12
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_pcap18
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_pcap25
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_pcap33
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/l65ll_v1
81.lib" tt_ll_res
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
RVT12_V101_RF.lib" tt
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
HVT12_V101_RF.lib" TT
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
LVT12_V101_RF.lib" TT
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
IO18_V101_RF.lib" TT
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
IO25_V101_RF.lib" tt
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
IO33_V111_RF.lib" TT
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
VARMIS12_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_
VARMIS18_V111_RF.lib" typ

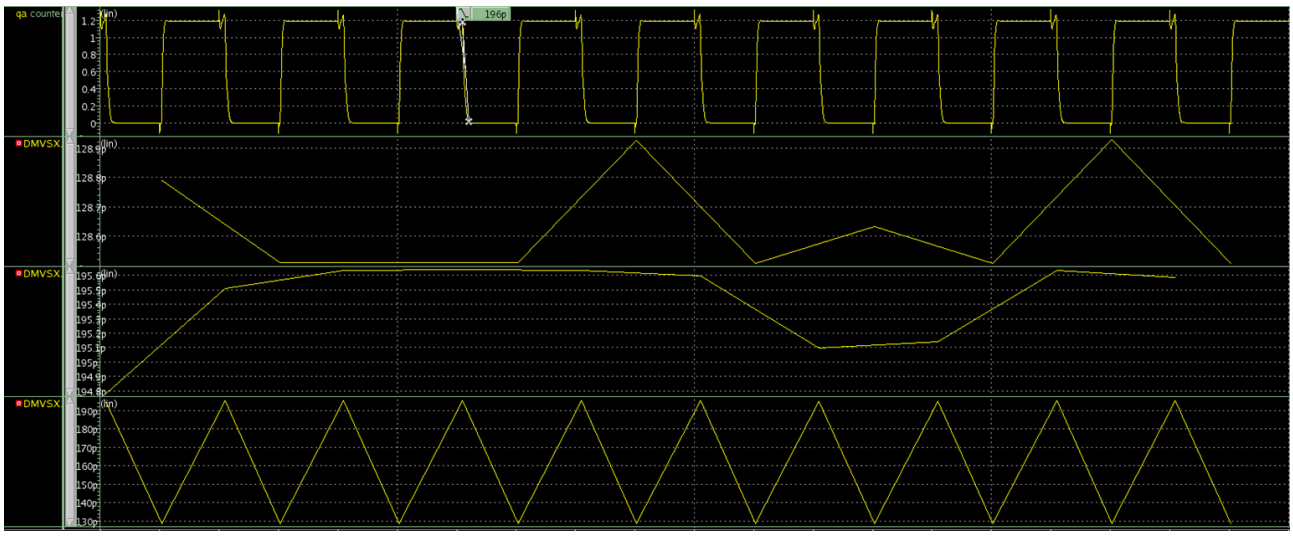
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_VARMIS25_V121_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_VARMIS33_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_VARDIOP_V101_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/momcaps_array_vp3_rfvcl_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/momcaps_array_vp4_rfvcl_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/momcaps_array_vp5_rfvcl_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65_MIMCAPS_20F_KF_V101_RF.lib" TT
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_RNNPO_V101_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_RNPPO_V101_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65LL_RNHR_V101_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/L65_pad_rf_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VIL/1P8M1T1U/l_sy30k_vil_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VIL/1P8M1T1U/l_syct30k_vil_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VIL/1P8M1T1U/l_slcr30k_vil_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VIL/1P8M1T1U/l_sqsk_vil_V111_RF.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VTL/1P8M1T1U/l_occtout_trans_rfvil_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VTL/1P8M1T1U/l_sq_trans_rfvil_V101.lib" typ

```
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VTL/1P
8M1T1U/l_sqctin_trans_rfvil_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VTL/1P
8M1T1U/l_sqctinout_trans_rfvil_V101.lib" typ
.LIB
"/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/Models/Hspice/VTL/1P
8M1T1U/l_sqctout_trans_rfvil_V101.lib" typ

* TEST IS NAND GATE

.subckt test a b out vdd vss
mnm1 out a net18 vss n_12_llrvt m=1 w=100e-9 l=60e-9 sa=175e-9 sb=175e-9 nf=1 mis_flag=1
sd=0 ad=24.1e-15 as=24.1e-15 pd=660e-9 ps=660e-9 sca=106.667 scb=36.4011e-3 scc=13.5264e-3
mf=1
mnm0 net18 b vss vss n_12_llrvt m=1 w=100e-9 l=60e-9 sa=175e-9 sb=175e-9 nf=1 mis_flag=1
sd=0 ad=24.1e-15 as=24.1e-15 pd=660e-9 ps=660e-9 sca=106.667 scb=36.4011e-3 scc=13.5264e-3
mf=1
mpm1 out b vdd vdd p_12_llrvt m=1 w=100e-9 l=60e-9 sa=175e-9 sb=175e-9 nf=1 mis_flag=1
sd=0 ad=24.1e-15 as=24.1e-15 pd=660e-9 ps=660e-9 sca=106.667 scb=36.4011e-3 scc=13.5264e-3
mf=1
mpm0 out a vdd vdd p_12_llrvt m=1 w=100e-9 l=60e-9 sa=175e-9 sb=175e-9 nf=1 mis_flag=1
sd=0 ad=24.1e-15 as=24.1e-15 pd=660e-9 ps=660e-9 sca=106.667 scb=36.4011e-3 scc=13.5264e-3
mf=1
.ends test

.subckt inverter in out vdd vss
mnm0 out in vss vss n_12_llrvt m=1 w=200e-9 l=60e-9 sa=160e-9 sb=160e-9 nf=1 mis_flag=1
sd=0 ad=32e-15 as=32e-15 pd=720e-9 ps=720e-9 sca=76.1905 scb=34.8763e-3 scc=10.5484e-3
mf=1
mpm0 out in vdd vdd p_12_llrvt m=1 w=400e-9 l=60e-9 sa=160e-9 sb=160e-9 nf=1 mis_flag=1
sd=0 ad=64e-15 as=64e-15 pd=1.12e-6 ps=1.12e-6 sca=48.4848 scb=29.3456e-3 scc=6.64077e-3
mf=1
.ends inverter

.subckt jk clk j k q q_bar vdd vss
xi9 clk k net43 vdd vss test
xi8 j clk net44 vdd vss test
xi7 q net40 q_bar vdd vss test
xi6 net39 q_bar q vdd vss test
xi5 net30 net27 net40 vdd vss test
xi4 net15 net30 net39 vdd vss test
xi3 net15 net25 net27 vdd vss test
xi2 net23 net27 net15 vdd vss test
xi1 q net027 net25 vdd vss test
xi0 q_bar net028 net23 vdd vss test
xi12 net43 net027 vdd vss inverter
xi11 net44 net028 vdd vss inverter
xi10 clk net30 q_bar q inverter
.ends jk
```

```
.subckt jk_counter clk qa qb qc vdd vss
xi8 clk net024 vdd qc qc_bar vdd vss jk
xi7 clk qa qa qb net30 vdd vss jk
xi0 clk qc_bar vdd qa net23 vdd vss jk
xi4 net14 net14 net024 vdd vss test
xi3 qa qb net14 vdd vss test
.ends jk_counter

xi0 clk qa qb qc net9 0 jk_counter
v0 clk 0 PULSE 0 1.2 0 1e-12 1e-12 2e-9 4e-9
v1 net9 0 DC=1.2
.END
```

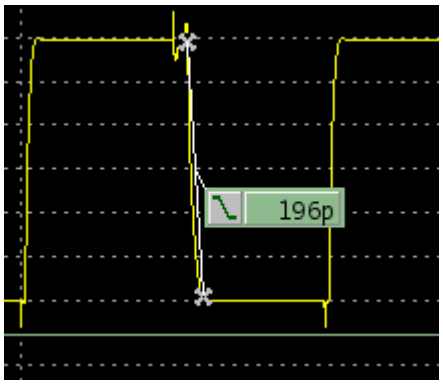


for rise and fall time



ri

rise tiime



fall time

for max current
End of pVA setup on Fri Jan 15 19:08:38 2021 GTM/In-use: 14.8750/5.0972 MB

info dc convergence successful at GMINDC ramping method

******

****** transient analysis tnom= 25.000 temp= 25.000 ******
******

****** transient analysis tnom= 25.000 temp= 25.000 ******
maxcur=   3.67m
iavg=   166n
power=   4.04m

        ***** job concluded
******

****** job statistics summary tnom= 25.000 temp= 25.000 ******

****** Machine Information ******
CPU:
model name   : Intel(R) Xeon(R) CPU E5-2650 v4 @ 2.20GHz
cpu MHz   : 2197.456

OS:
Linux version 4.9.0-4-amd64 (debian-kernel@lists.debian.org) (gcc version 6.3.0 20170516 (Debian 6.3.0-18)) #1 SMP Debian 4.9.65-3+deb9u1 (2017-12-23)