

GENUS

```

@genus:root: 23> report_qor
=====
Generated by:          Genus(TM) Synthesis Solution 19.12-s121_1
Generated on:         Mar 04 2021  10:25:31 pm
Module:               mips_16
Technology library:   uk65lscllmvbbr_100c25_tc
Operating conditions: uk65lscllmvbbr_100c25_tc (balanced_tree)
Wireload mode:        top
Area mode:            timing library
=====

Timing
-----
Clock Period
-----
clk  2000.0

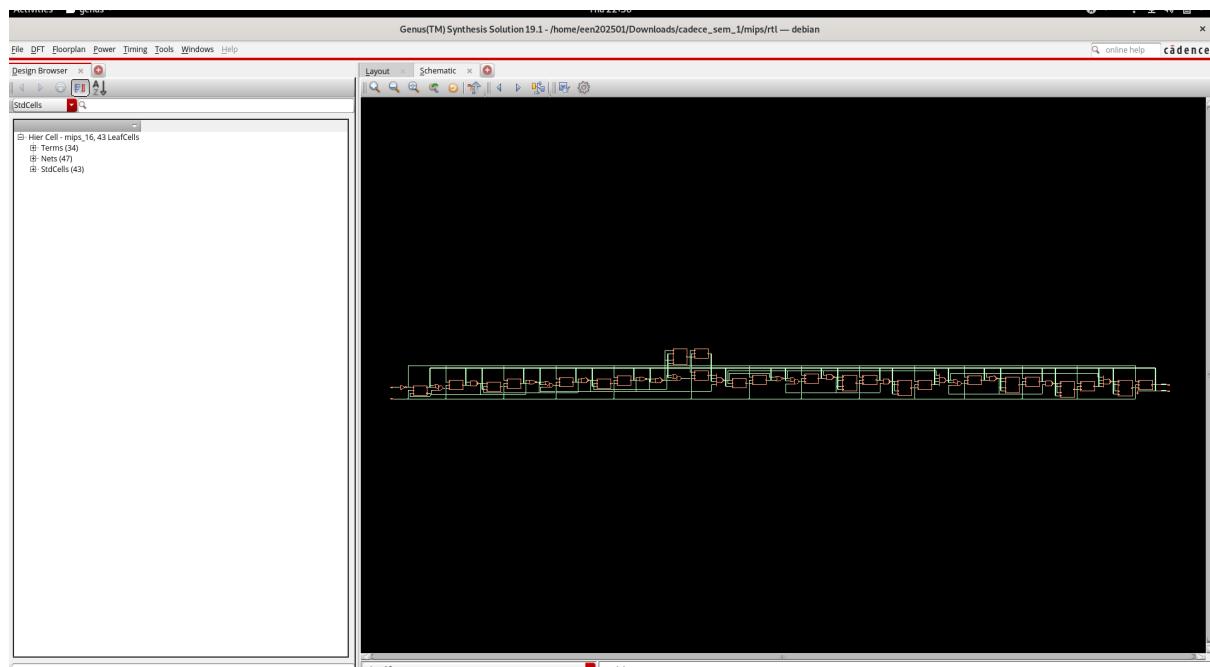
  Cost    Critical      Violating
 Group  Path Slack  TNS    Paths
-----
clk      800.2    0.0      0
default   No paths  0.0
-----
Total      0.0      0.0      0

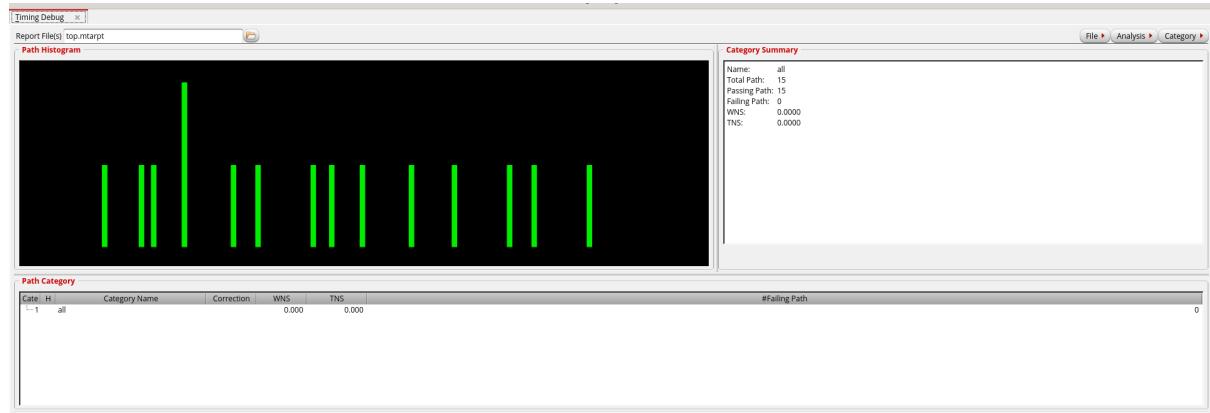
Instance Count
-----
Leaf Instance Count      43
Physical Instance count  0
Sequential Instance Count 15
Combinational Instance Count 28
Hierarchical Instance Count 0

Area
-----
Cell Area                185.400
Physical Cell Area       0.000
Total Cell Area (Cell+Physical) 185.400
Net Area                 0.000
Total Area (Cell+Physical+Net) 185.400

Max Fanout              17 (pc_out[0])
Min Fanout              0 (n_28)
Average Fanout          3.0
Terms to net ratio       3.6170
Terms to instance ratio  3.9535
Runtime                  101.481251 seconds
Elapsed Runtime          585 seconds
Genus peak memory usage 1196.18
Innovus peak memory usage no_value
Hostname                 debian
@genus:root: 24>

```





Generated by: Genus(TM) Synthesis Solution 19.12-s121_1 (Dec 3 2019 15:07:17)

Generated on: Mar 04 2021 22:40:10

Module: design:mips_16

Technology library: uk65lscllmvbbbr_100c25_tc

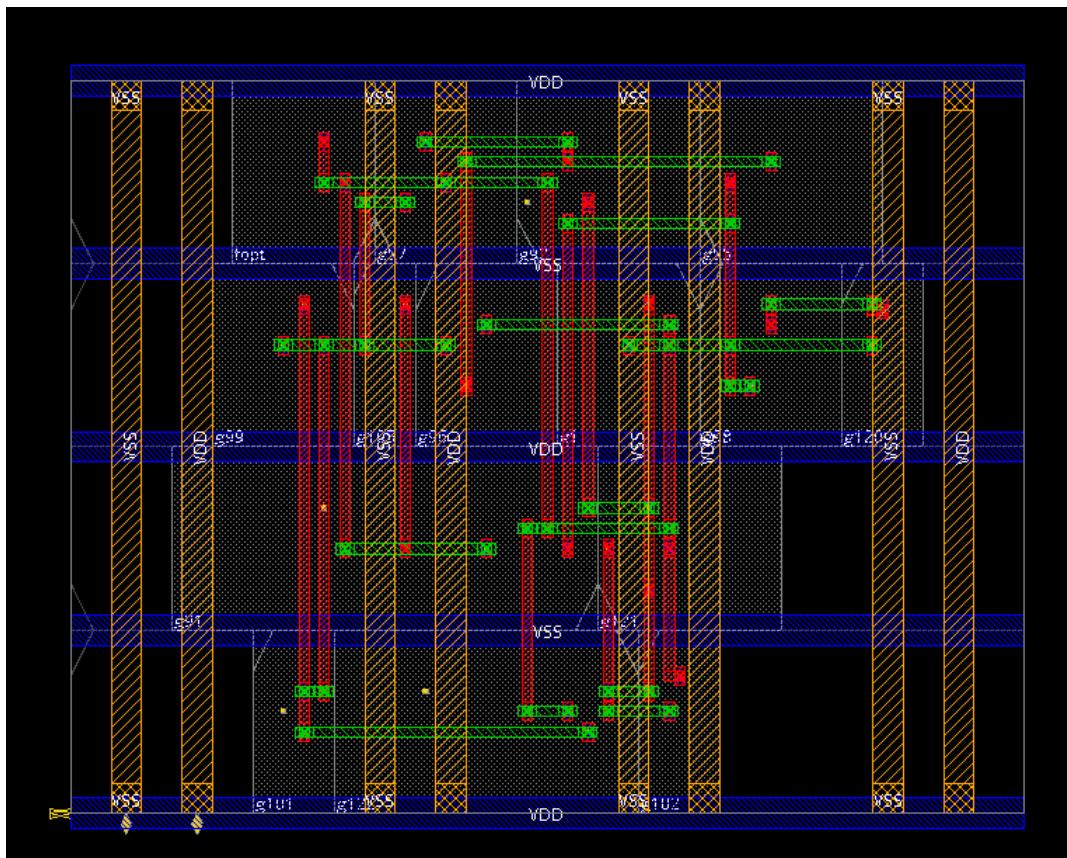
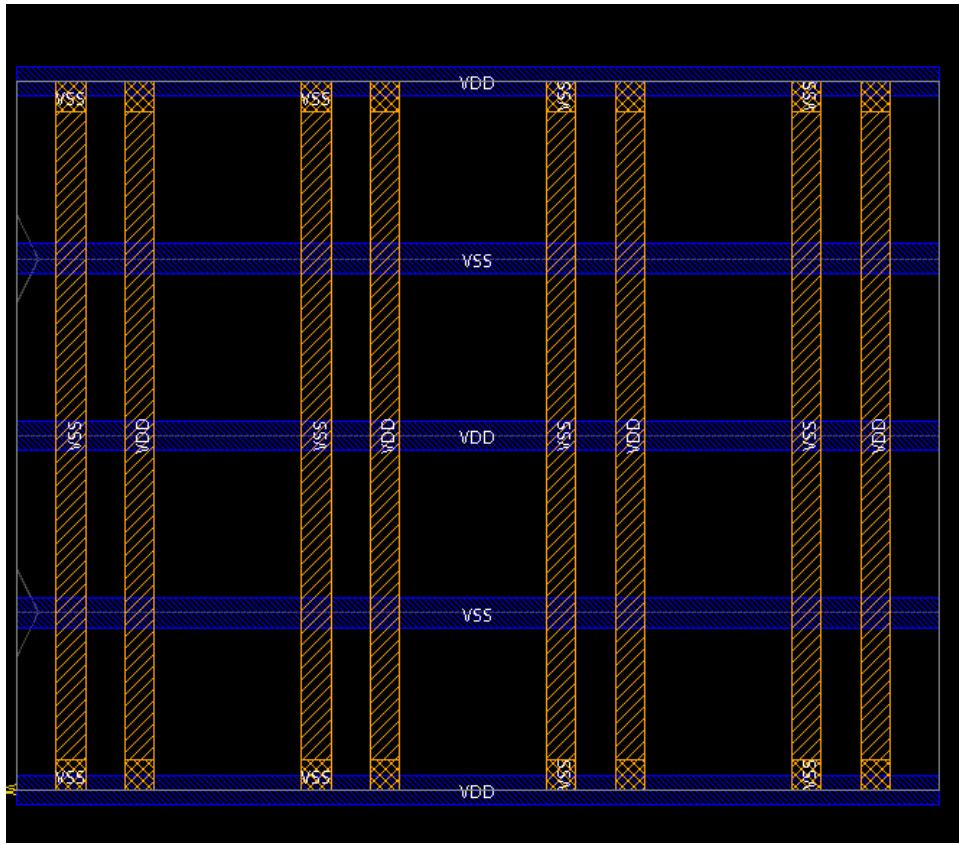
Operating conditions: uk65lscllmvbbbr_100c25_tc (balanced_tree)

Wireload mode: top

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
mips_16	43	7.411	51669.418	9172.923	60842.341

INNOVUS

- Alu control



1. Connectivtity

```
Design Name: ALUControl
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (9.4000, 7.2000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 16:52:22 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

2. Geometry

```

innovus 1> *** Starting Verify Geometry (MEM: 1262.2) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
    VERIFY GEOMETRY ..... Starting Verification
    VERIFY GEOMETRY ..... Initializing
    VERIFY GEOMETRY ..... Deleting Existing Violations
    VERIFY GEOMETRY ..... Creating Sub-Areas
        ..... bin size: 2880
    VERIFY GEOMETRY ..... SubArea : 1 of 1
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.

VG: elapsed time: 0.00
Begin Summary ...
    Cells : 0
    SameNet : 0
    Wiring : 0
    Antenna : 0
    Short : 0
    Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1  MEM: 0.0M)

```

3. Drc

```

#-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion "
                # enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure
re color min_step protrusion min_area out_of_die}_list, default= , user setting
#-check_implant false                      # bool, default=true, user setting
#-exclude_pg_net true                      # bool, default=false, user setting
#-ignore_trial_route true                  # bool, default=false, user setting
#-report ALUControl.drc.rpt               # string, default="", user setting
*** Starting Verify DRC (MEM: 1305.6) ***

    VERIFY DRC ..... Starting Verification
    VERIFY DRC ..... Initializing
    VERIFY DRC ..... Deleting Existing Violations
    VERIFY DRC ..... Creating Sub-Areas
    VERIFY DRC ..... Using new threading
    VERIFY DRC ..... Sub-Area: {0.000 0.000 9.400 7.200} 1 of 1
    VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***

```

4. Timing

```

-----  

          timeDesign Summary  

-----  

Setup views included:  

worst_case  

+-----+-----+-----+
|   Setup mode    | all   | default |
+-----+-----+-----+
|       WNS (ns):| 0.000 | 0.000 |
|       TNS (ns):| 0.000 | 0.000 |
| Violating Paths:| 0     | 0     |
| All Paths:| 0     | 0     |
+-----+-----+-----+  

+-----+-----+-----+
|           Real           |      Total      |
|      DRVs      +-----+-----+
|           | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0)        | 0.000  | 0 (0)  |
| max_tran | 0 (0)        | 0.000  | 0 (0)  |
| max_fanout | 0 (0)        | 0      | 0 (0)  |
| max_length | 0 (0)        | 0      | 0 (0)  |
+-----+-----+-----+  

Density: 63.830%
Routing Overflow: 0.00% H and 0.00% V
-----  

Reported timing to dir timingReports
Total CPU time: 3.95 sec
Total Real time: 13.0 sec
Total Memory Usage: 1830.191406 Mbytes
innovus 2> □

```

```

-----  

          timeDesign Summary  

-----  

Hold  views included:  

best_case  

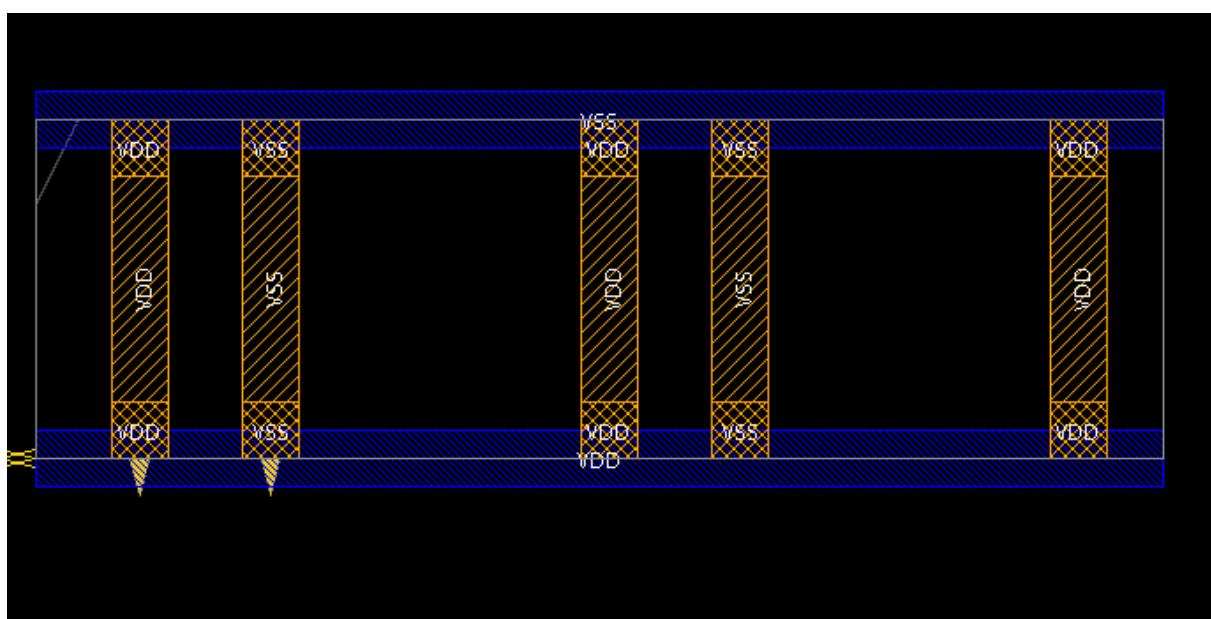
+-----+-----+-----+
|   Hold mode     | all   | default |
+-----+-----+-----+
|       WNS (ns):| 0.000 | 0.000 |
|       TNS (ns):| 0.000 | 0.000 |
| Violating Paths:| 0     | 0     |
| All Paths:| 0     | 0     |
+-----+-----+-----+  

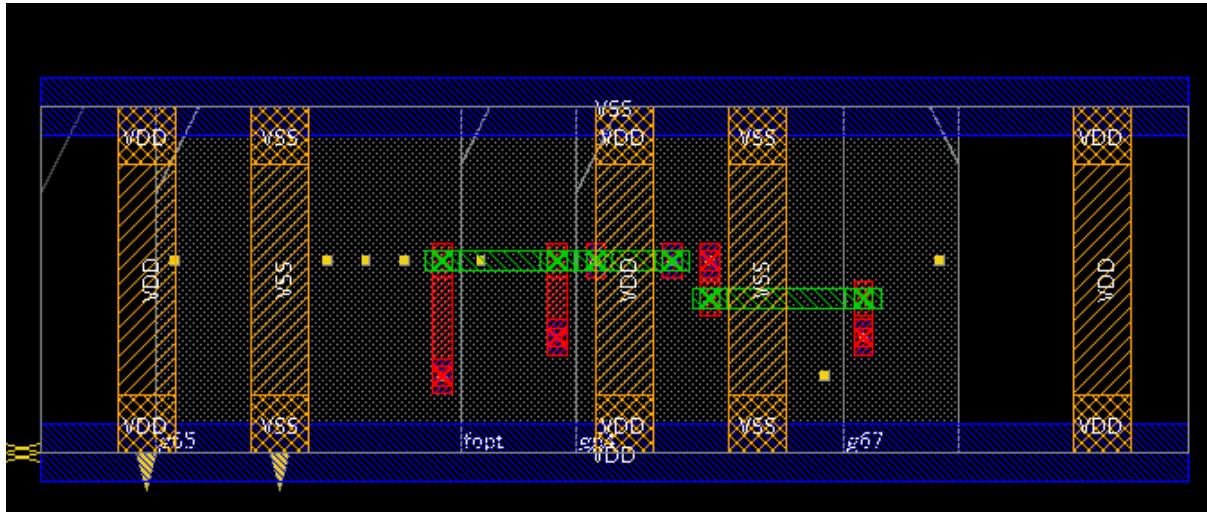
Density: 63.830%
Routing Overflow: 0.00% H and 0.00% V
-----  

Reported timing to dir timingReports
Total CPU time: 0.21 sec
Total Real time: 0.0 sec
Total Memory Usage: 1848.332031 Mbytes
innovus 2> □

```

- JR_control





1. Timming

```

optDesign Final Summary

Setup views included:
worst_case
Hold views included:
best_case

+-----+-----+-----+
| Setup mode | all | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
+-----+-----+-----+

+-----+-----+-----+
| Hold mode | all | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 70.000%
Routing Overflow: 0.00% H and 0.00% V

**optDesign ... cpu = 0:00:05, real = 0:00:07, mem = 2061.0M, totSessionCpu=0:05:03 ***
*** Finished optDesign ***
innovus 6>
innovus 6> innovus 6> □

```

2. DRC

```
innovus 2> verify_drc -limit 10000
#-limit 10000                                # int, default=10000, user setting
*** Starting Verify DRC (MEM: 1940.5) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 6.000 1.800} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 10 Viols.

Verification Complete : 10 Viols.

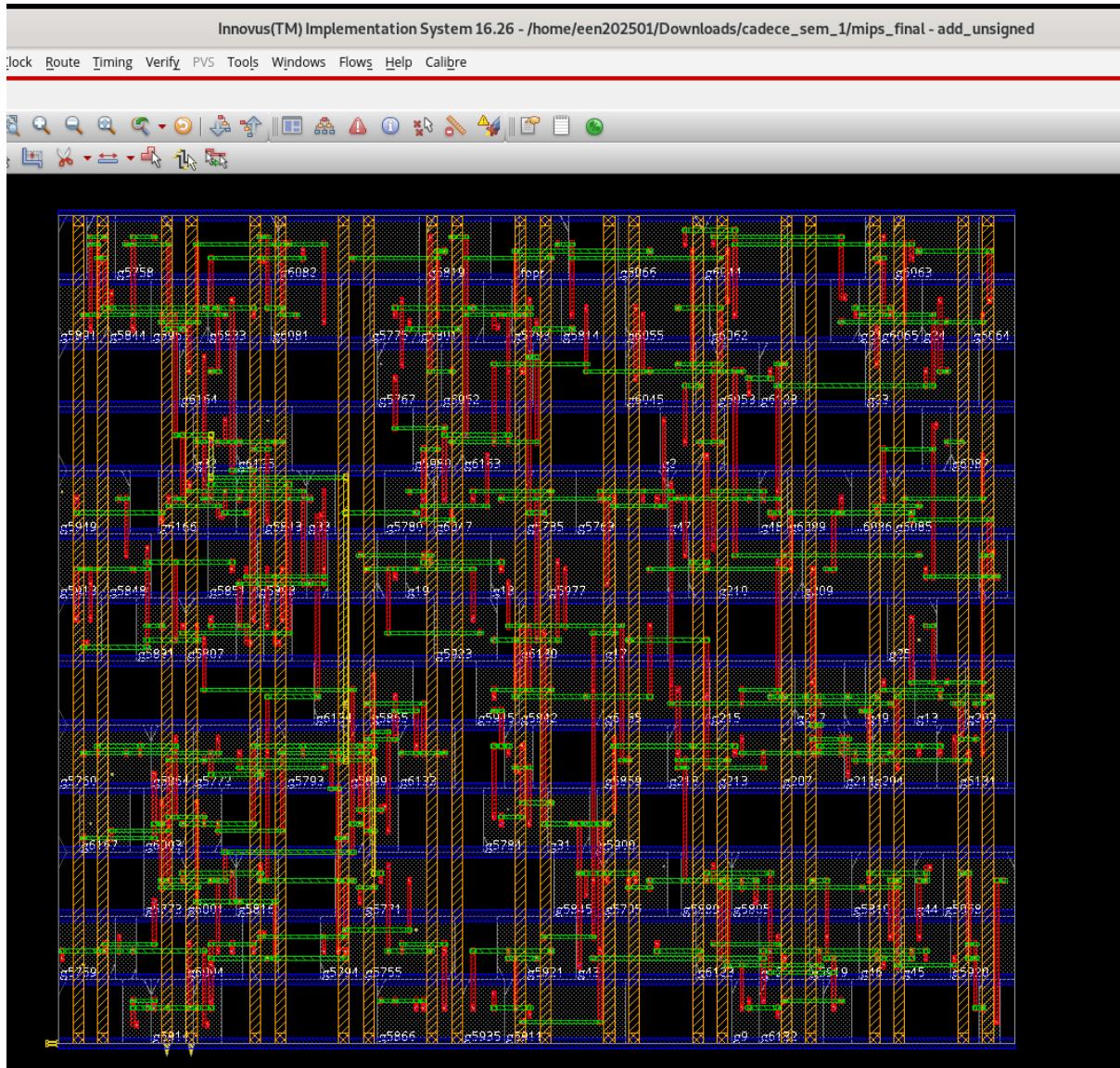
*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

3. placement

```
innovus 1> Begin checking placement ... (start mem=1999.4M, init mem=1999.4M)
*info: Placed = 43
*info: Unplaced = 0
Placement Density:69.22%(185/268)
Placement Density (including fixed std cells):69.22%(185/268)
Finished checkPlace (cpu: total=0:00:00.1, vio checks=0:00:00.0; mem=1999.4M)
innovus 1> █
```

```
innovus 1> Begin checking placement ... (start mem=1999.4M, init mem=1999.4M)
*info: Placed = 43
*info: Unplaced = 0
Placement Density:69.22%(185/268)
Placement Density (including fixed std cells):69.22%(185/268)
Finished checkPlace (cpu: total=0:00:00.1, vio checks=0:00:00.0; mem=1999.4M)
innovus 1> █
```

add_unsigned



1. placement

```
innovus l> Begin checking placement ... (start mem=1866.8M, init mem=1866.8M)
*info: Placed = 154
*info: Unplaced = 0
Placement Density:67.35%(426/632)
Placement Density (including fixed std cells):67.35%(426/632)
Finished checkPlace (cpu: total=0:00:00.1, vio checks=0:00:00.0; mem=1866.8M)
innovus l> 
```

2. Geometry

```

innovus 1> *** Starting Verify Geometry (MEM: 1974.9) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
..... maxBinCols: 129, maxBinRows: 129
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 0.0M)

innovus 1> 
```

3. CONNECTION

```

innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar 5 17:17:44 2021

Design Name: add_unsigned
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (27.0000, 23.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Fri Mar 5 17:17:44 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 1> 
```

4. DRC

```

#-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion "
#-enable_color_min_step protrusion min_area out_of_die_list, default= , user setting
#-check_implant false # bool, default=true, user setting
#-exclude_pg_net true # bool, default=false, user setting
#-ignore_trial_route true # bool, default=false, user setting
#-report add_unsigned.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 1878.1) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 27.000 23.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***

```

5. SETUP

```

-----
timeDesign Summary
-----

Setup views included:
worst_case

+-----+-----+-----+
| Setup mode | all | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
+-----+-----+-----+

+-----+-----+-----+-----+
| | Real | | Total | |
| DRVs +-----+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

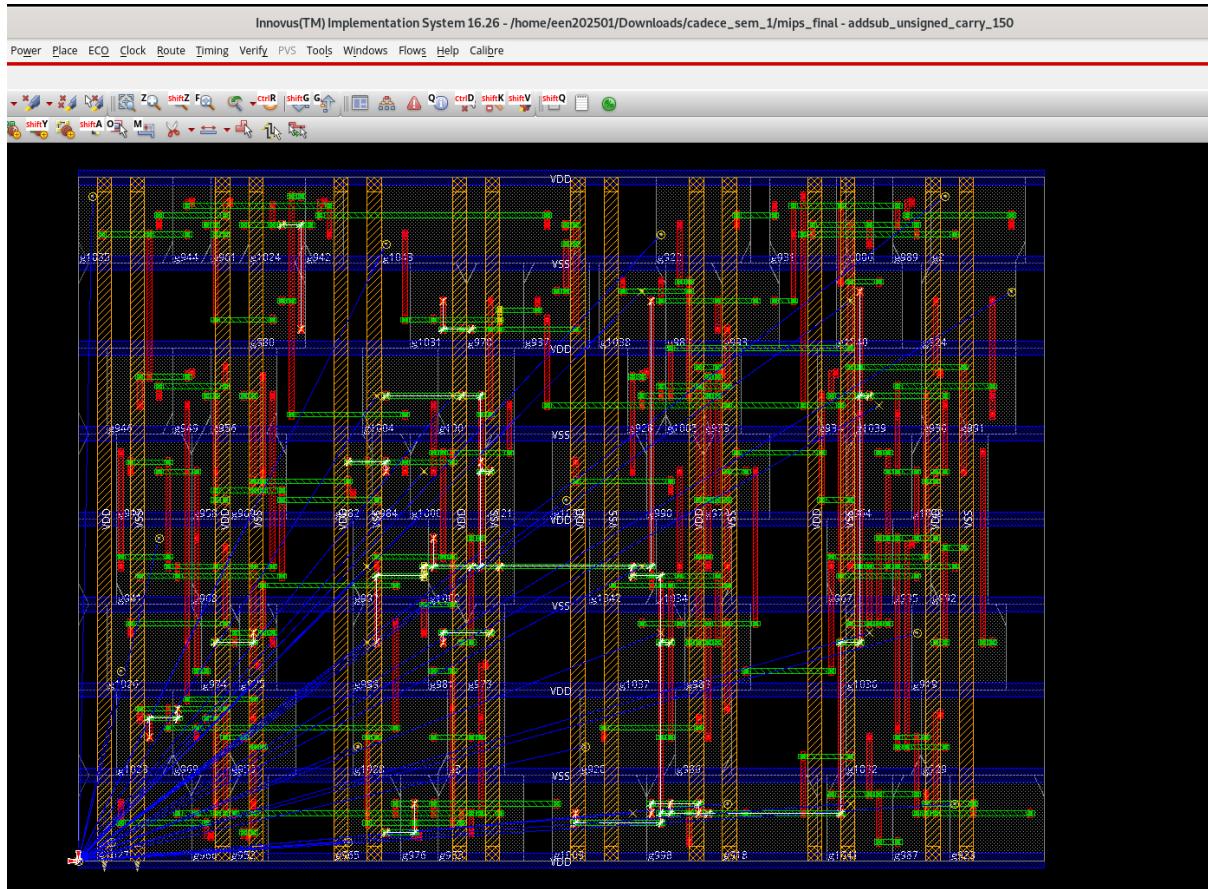
Density: 67.853%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 1.31 sec
Total Real time: 10.0 sec
Total Memory Usage: 1946.566406 Mbytes
innovus 4> 

```

6. HOLD

```
-----  
          timeDesign Summary  
-----  
  
Hold  views included:  
 best_case  
  
+-----+-----+-----+  
| Hold mode |    all    | default |  
+-----+-----+-----+  
|      WNS (ns):|  0.000  |  0.000  |  
|      TNS (ns):|  0.000  |  0.000  |  
| Violating Paths:|    0    |    0    |  
| All Paths:|    0    |    0    |  
+-----+-----+-----+  
  
Density: 67.853%  
Routing Overflow: 0.00% H and 0.00% V  
-----  
Reported timing to dir timingReports  
Total CPU time: 0.23 sec  
Total Real time: 0.0 sec  
Total Memory Usage: 1930.425781 Mbytes  
innovus 4> [ ]
```

ADD_SUB_UNSIGNED_CARRY



1. PLACEMENT

```
innovus 3> Begin checking placement ... (start mem=1302.3M, init mem=1302.3M)
*info: Placed = 84
*info: Unplaced = 0
Placement Density:69.36%(204/294)
Placement Density (including fixed std cells):69.36%(204/294)
Finished checkPlace (cpu: total=0:00:00.0, vio checks=0:00:00.0; mem=1302.3M)
innovus 3> 
```

2. GEOMETRY

```

innovus 3> *** Starting Verify Geometry (MEM: 1408.8) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
    VERIFY GEOMETRY ..... Starting Verification
    VERIFY GEOMETRY ..... Initializing
    VERIFY GEOMETRY ..... Deleting Existing Violations
    VERIFY GEOMETRY ..... Creating Sub-Areas
        ..... bin size: 2880
    VERIFY GEOMETRY ..... SubArea : 1 of 1
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
    Cells : 0
    SameNet : 0
    Wiring : 0
    Antenna : 0
    Short : 0
    Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 0.0M)

innovus 3> 

```

3.DRC

```

#-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion "
# enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure
re color min_step protrusion min_area out_of_die} list, default= , user setting
#-ignore_trial_route true # bool, default=false, user setting
#-report addsub_unsigned_carry_150.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 1313.0) ***

    VERIFY DRC ..... Starting Verification
    VERIFY DRC ..... Initializing
    VERIFY DRC ..... Deleting Existing Violations
    VERIFY DRC ..... Creating Sub-Areas
    VERIFY DRC ..... Using new threading
    VERIFY DRC ..... Sub-Area: {0.000 0.000 20.400 14.400} 1 of 1
    VERIFY DRC ..... Sub-Area : 1 complete 2 Viols.

Verification Complete : 2 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***

```

4. CONNECTIVITY

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 17:44:40 2021

Design Name: addsub_unsigned_carry_150
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (20.4000, 14.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 17:44:40 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 3> 
```

5. TIMMING

```

-----
optDesign Final Summary
-----

Setup views included:
worst_case
Hold views included:
best_case

+-----+-----+-----+
| Setup mode | all | default |
+-----+-----+-----+
| WNS (ns):| 0.000 | 0.000 |
| TNS (ns):| 0.000 | 0.000 |
| Violating Paths:| 0 | 0 |
| All Paths:| 0 | 0 |
+-----+-----+-----+

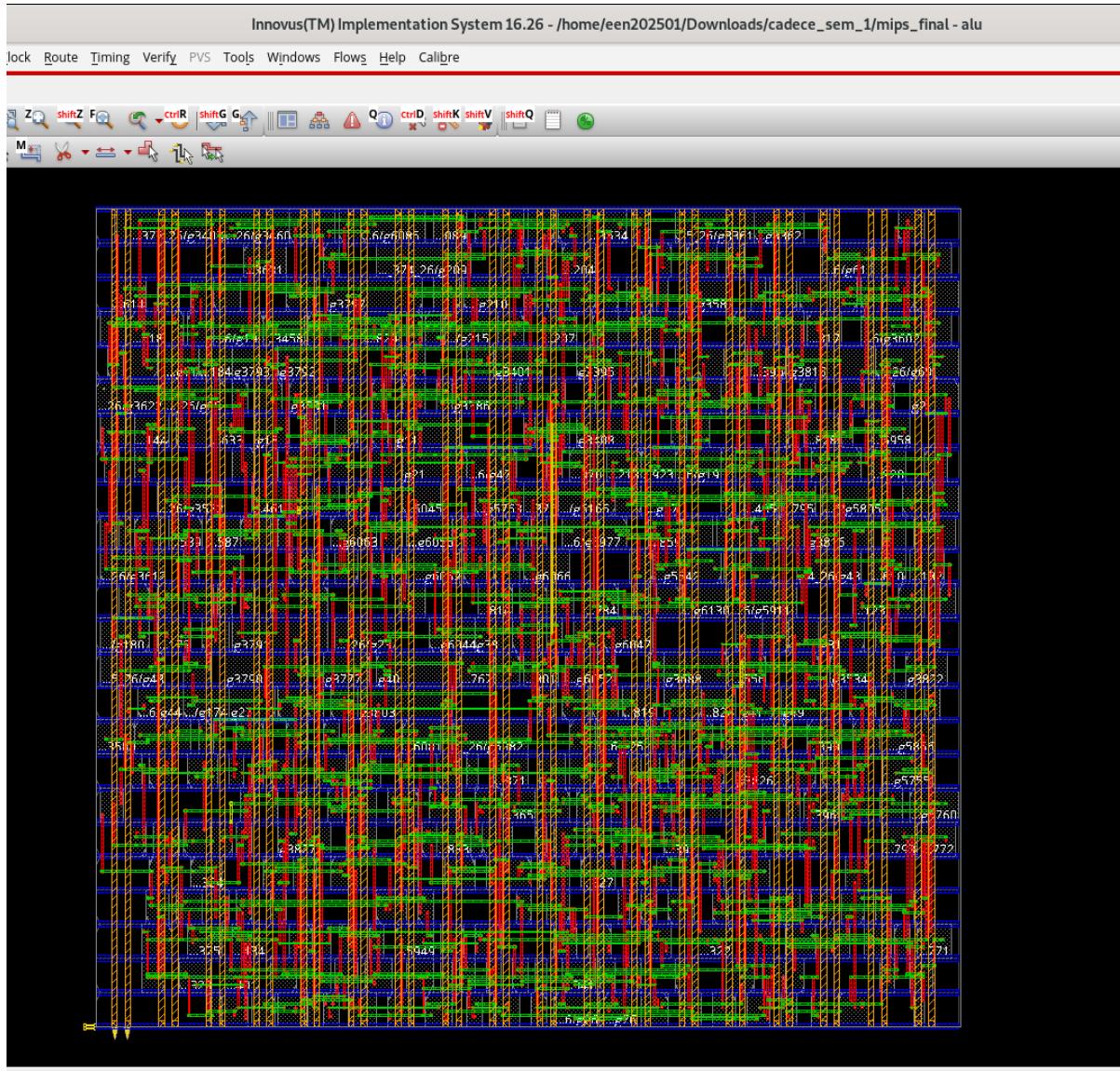
+-----+-----+-----+
| Hold mode | all | default |
+-----+-----+-----+
| WNS (ns):| 0.000 | 0.000 |
| TNS (ns):| 0.000 | 0.000 |
| Violating Paths:| 0 | 0 |
| All Paths:| 0 | 0 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 69.363%
Routing Overflow: 0.00% H and 0.00% V
-----
**optDesign ... cpu = 0:00:10, real = 0:00:23, mem = 2076.8M, totSessionCpu=0:03:08 ***
*** Finished optDesign ***
innovus 5>
innovus 5> innovus 5> []

```

ALU



1. CONNECTION

```

innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 17:55:51 2021

Design Name: alu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (45.6800, 43.2000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 17:55:51 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 1> □

```

2. DRC

```

#-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion "
#               # enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure
re color min_step protrusion min_area out_of_die}_list, default= , user setting
#-exclude_pg_net true                      # bool, default=false, user setting
#-ignore_trial_route true                  # bool, default=false, user setting
#-report alu.drc.rpt                      # string, default="", user setting
*** Starting Verify DRC (MEM: 1874.2) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 45.680 43.200} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
□

```

3. GEOMETRY

```
innovus 3> *** Starting Verify Geometry (MEM: 2079.8) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.

VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
    ..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.

VG: elapsed time: 0.00
Begin Summary ...
    Cells : 0
    SameNet : 0
    Wiring : 0
    Antenna : 0
    Short : 0
    Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.2 MEM: 43.5M)

innovus 3> 
```

4. TIMMING

```

optDesign Final Summary

Setup views included:
worst_case
Hold views included:
best_case

-----+-----+-----+
Setup mode | all | default |
-----+-----+-----+
      WNS (ns):| 0.000 | 0.000 |
      TNS (ns):| 0.000 | 0.000 |
Violating Paths:| 0 | 0 |
All Paths:| 0 | 0 |
-----+-----+-----+

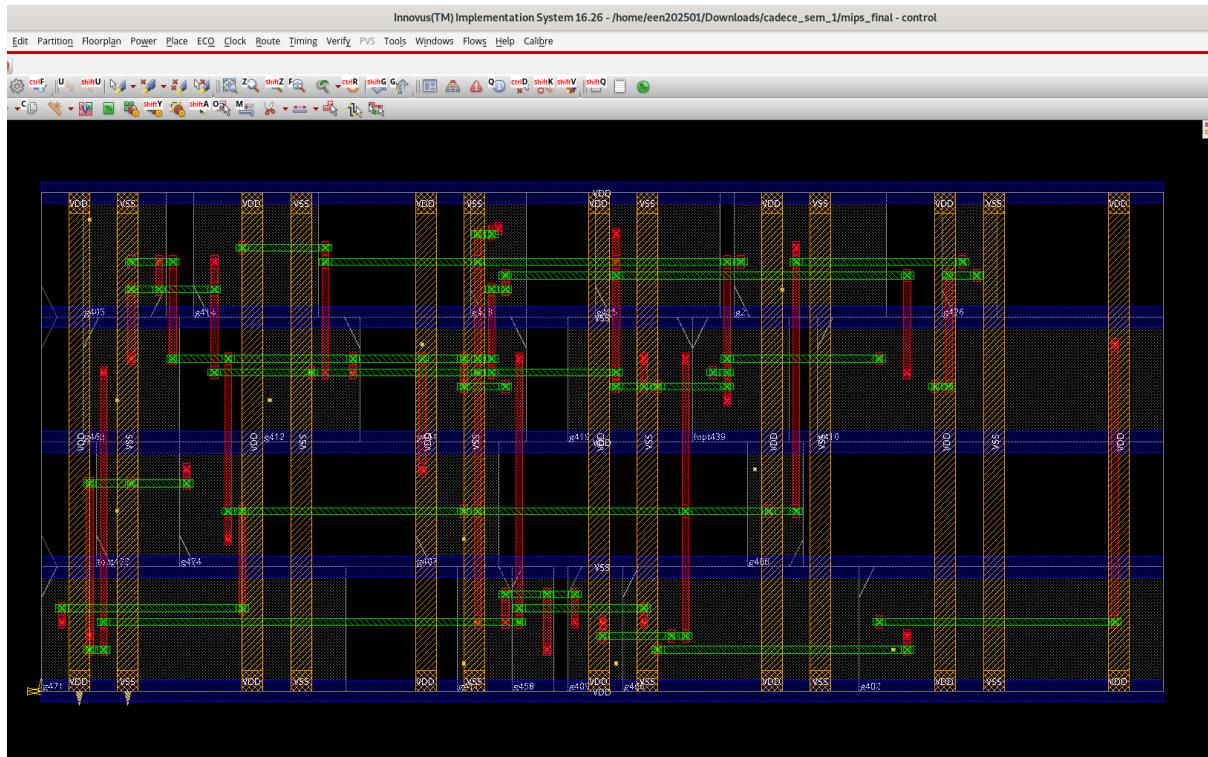

-----+-----+-----+
Hold mode | all | default |
-----+-----+-----+
      WNS (ns):| 0.000 | 0.000 |
      TNS (ns):| 0.000 | 0.000 |
Violating Paths:| 0 | 0 |
All Paths:| 0 | 0 |
-----+-----+-----+


-----+-----+-----+
DRVs | Real | Total |
-----+-----+-----+
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
-----+-----+-----+
max_cap | 0 (0) | 0.000 | 0 (0) |
max_tran | 0 (0) | 0.000 | 0 (0) |
max_fanout | 0 (0) | 0 | 0 (0) |
max_length | 0 (0) | 0 | 0 (0) |
-----+-----+-----+


Density: 65.387%
Routing Overflow: 0.00% H and 0.00% V
**optDesign ... cpu = 0:00:11, real = 0:00:29, mem = 2079.8M, totSessionCpu=0:02:49 ***
*** Finished optDesign ***
Innovus 3>
Innovus 3> Innovus 3> []

```

CONTROL



1. GEOMETRY

```
innovus 1> *** Starting Verify Geometry (MEM: 1845.2) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.

VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
    ..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells      : 0 Viols.
VERIFY GEOMETRY ..... SameNet    : 0 Viols.
VERIFY GEOMETRY ..... Wiring     : 0 Viols.
VERIFY GEOMETRY ..... Antenna   : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
    Cells      : 0
    SameNet    : 0
    Wiring     : 0
    Antenna   : 0
    Short     : 0
    Overlap   : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 102.0M)

innovus 1> 
```

2. DRC

```
innovus 1> #-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion
"
                                         # enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure
re color min_step protrusion min_area out_of_die}_list, default= , user setting
#-exclude_pg_net true                      # bool, default=false, user setting
#-ignore_trial_route true                  # bool, default=false, user setting
#-report control.drc.rpt                 # string, default="", user setting
*** Starting Verify DRC (MEM: 1947.1) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 16.200 7.200} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

3. CONNECTIVITY

```
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 19:47:24 2021

Design Name: control
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (16.2000, 7.2000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 19:47:24 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

4. TIMMING

```

-----  

optDesign Final Summary  

-----  

Setup views included:  

worst_case  

Hold views included:  

best_case  

-----  

+-----+-----+-----+
| Setup mode | all | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
+-----+-----+-----+  

+-----+-----+-----+
| Hold mode | all | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
+-----+-----+-----+  

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+  

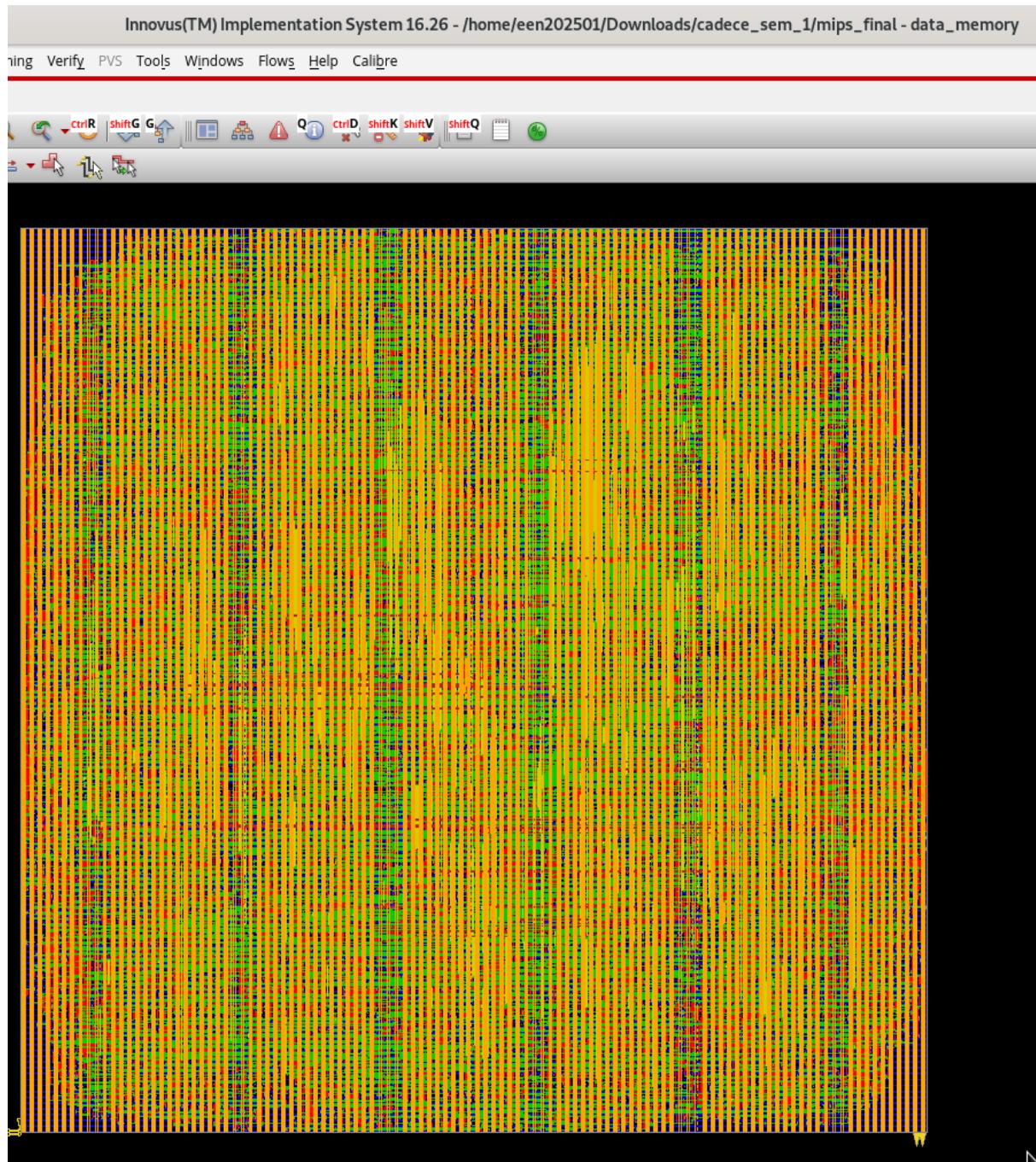
Density: 61.728%
Routing Overflow: 0.00% H and 0.00% V
-----  

**optDesign ... cpu = 0:00:07, real = 0:00:13, mem = 2080.3M, totSessionCpu=0:18:25 **  

*** Finished optDesign ***

```

Data_memory



1. GEOMETRY

```

Reported timing to dir timingReports
Total CPU time: 4.21 sec
Total Real time: 4.0 sec
Total Memory Usage: 2198.730469 Mbytes
innovus 7> *** Starting Verify Geometry (MEM: 2198.7) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
    VERIFY GEOMETRY ..... Starting Verification
    VERIFY GEOMETRY ..... Initializing
    VERIFY GEOMETRY ..... Deleting Existing Violations
    VERIFY GEOMETRY ..... Creating Sub-Areas
        ..... bin size: 2880
        ..... maxBinCols: 129, maxBinRows: 129
    VERIFY GEOMETRY ..... SubArea : 1 of 4
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
    VERIFY GEOMETRY ..... SubArea : 2 of 4
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 2 complete 0 Viols. 0 Wrngs.
    VERIFY GEOMETRY ..... SubArea : 3 of 4
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 1 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 3 complete 1 Viols. 0 Wrngs.
    VERIFY GEOMETRY ..... SubArea : 4 of 4
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 4 complete 0 Viols. 0 Wrngs.

VG: elapsed time: 3.00
Begin Summary ...
    Cells : 0
    SameNet : 1
    Wiring : 0
    Antenna : 0
    Short : 0
    Overlap : 0
End Summary

    Verification Complete : 1 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****

```

2. DRC

```

#-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion "
#-check_color_min_step_min_area_min_cut_min_step_protrusion_min_area_out_of_die_list_default_
#-check_implant false # bool, default=true, user setting
#-exclude_pg_net true # bool, default=false, user setting
#-ignore_trial_route true # bool, default=false, user setting
#-report_data_memory.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 2377.3) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 70.560 70.560} 1 of 16
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {70.560 0.000 141.120 70.560} 2 of 16
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {141.120 0.000 211.680 70.560} 3 of 16
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {211.680 0.000 279.610 70.560} 4 of 16
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 70.560 70.560 141.120} 5 of 16
VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {70.560 70.560 141.120 141.120} 6 of 16
VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {141.120 70.560 211.680 141.120} 7 of 16
VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {211.680 70.560 279.610 141.120} 8 of 16
VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 141.120 70.560 211.680} 9 of 16
VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {70.560 141.120 141.120 211.680} 10 of 16
VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {141.120 141.120 211.680 211.680} 11 of 16
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {211.680 141.120 279.610 211.680} 12 of 16
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 211.680 70.560 279.000} 13 of 16
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {70.560 211.680 141.120 279.000} 14 of 16
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {141.120 211.680 211.680 279.000} 15 of 16
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {211.680 211.680 279.610 279.000} 16 of 16
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.0M) ***

```

3. CONNECTIVITY

```
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 20:07:54 2021

Design Name: data_memory
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (279.6100, 279.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 20:07:55 **** Processed 5000 nets.
**** 20:07:55 **** Processed 10000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 20:07:55 2021
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.4  MEM: 0.000M)
```

4. Setup and hold

```

optDesign Final Summary

Setup views included:
worst_case
Hold views included:
best_case

+-----+-----+-----+-----+
|   Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
|       WNS (ns):| -0.205 | 1.284 | -0.205 |
|       TNS (ns):| -199.511 | 0.000 | -199.511 |
| Violating Paths:| 2573 | 0 | 2573 |
| All Paths:| 8679 | 3431 | 6720 |
+-----+-----+-----+-----+

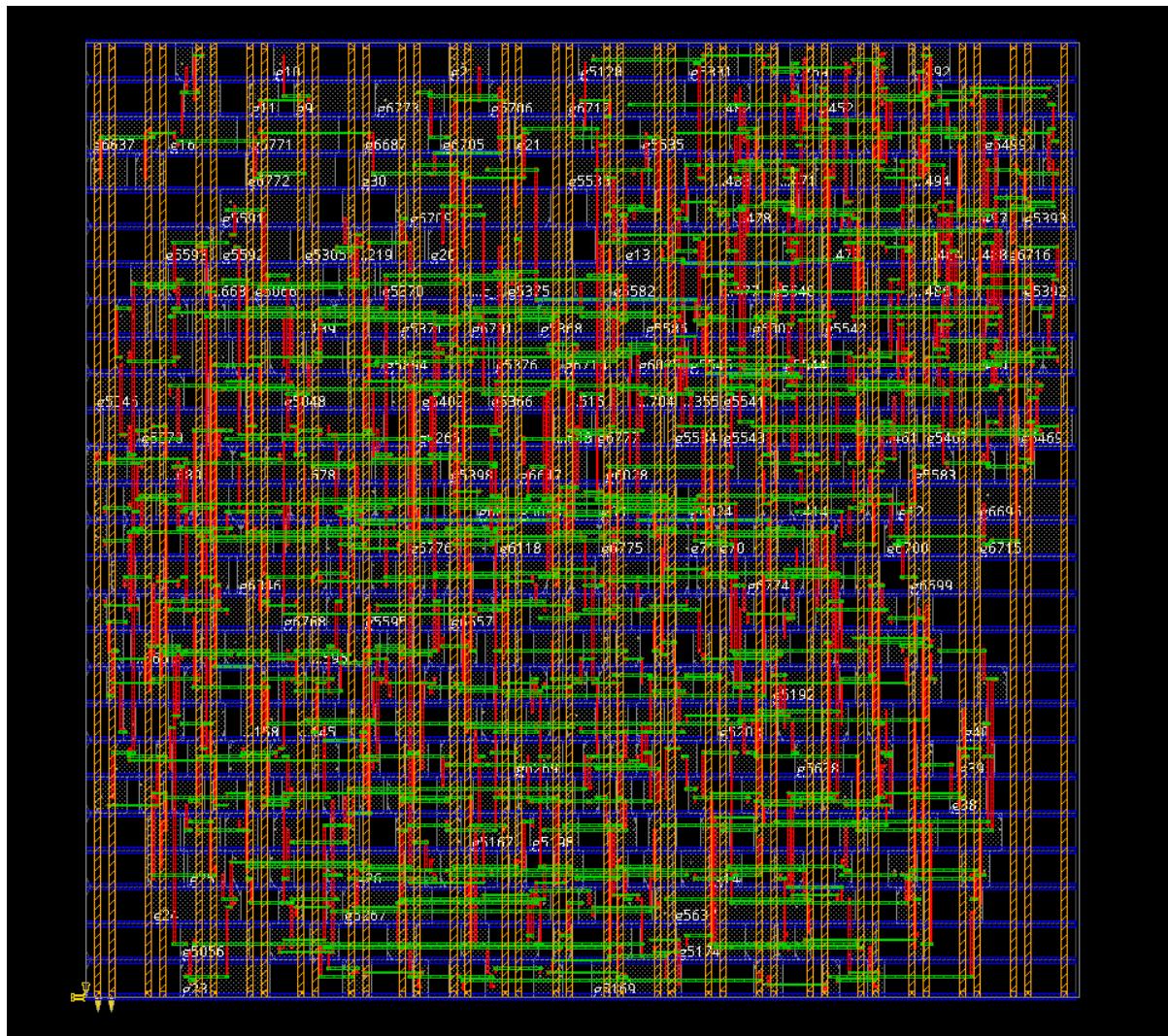
+-----+-----+-----+-----+
|   Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
|       WNS (ns):| 0.007 | 0.093 | 0.007 |
|       TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 8679 | 3431 | 6720 |
+-----+-----+-----+-----+

+-----+-----+-----+-----+
|           |          Real          |          Total          | |
| DRVs      |          |          |          |
|           | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap  | 4 (4)    | -0.185 | 4 (4)    |
| max_tran | 5 (585)  | -1.446 | 5 (585)  |
| max_fanout | 0 (0)    | 0       | 0 (0)    |
| max_length | 0 (0)    | 0       | 0 (0)    |
+-----+-----+-----+-----+

Density: 68.641%
Routing Overflow: 0.00% H and 0.00% V
**optDesign ... cpu = 0:00:19, real = 0:00:22, mem = 2476.2M, totSessionCpu=0:04:24 ***
**WARN: (IMPOPT-3195): Analysis mode has changed.
Type 'man IMPOPT-3195' for more detail.
*** Finished optDesign ***

```

Instr_mems



1. GEOMETRY

```

innovus l> **WARN: (IMPTCM-77): Option "-drouteStartIteration" for command getNanoRouteMode is obsolete and will be removed in a future release. The obsolete option still works in this release but to avoid this warning and to ensure compatibility with future releases, remove the obsolete option from your script.
*** Starting Verify Geometry (MEM: 1858.1) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 103.5M)

```

2. DRC

```

"
# enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure_color min_step protrusion min_area out_of_die} list, default= , user setting
#-exclude_pg_net true # bool, default=false, user setting
#-ignore_trial_route true # bool, default=false, user setting
#-report instr mem.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 1961.6) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 48.760 46.800} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***

```

3. CONNECTIVITY

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 20:19:56 2021

Design Name: instr_mem
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (48.7600, 46.8000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 20:19:56 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

4. TIMMING

```

-----  

 optDesign Final Summary  

-----  

Setup views included:  

worst_case  

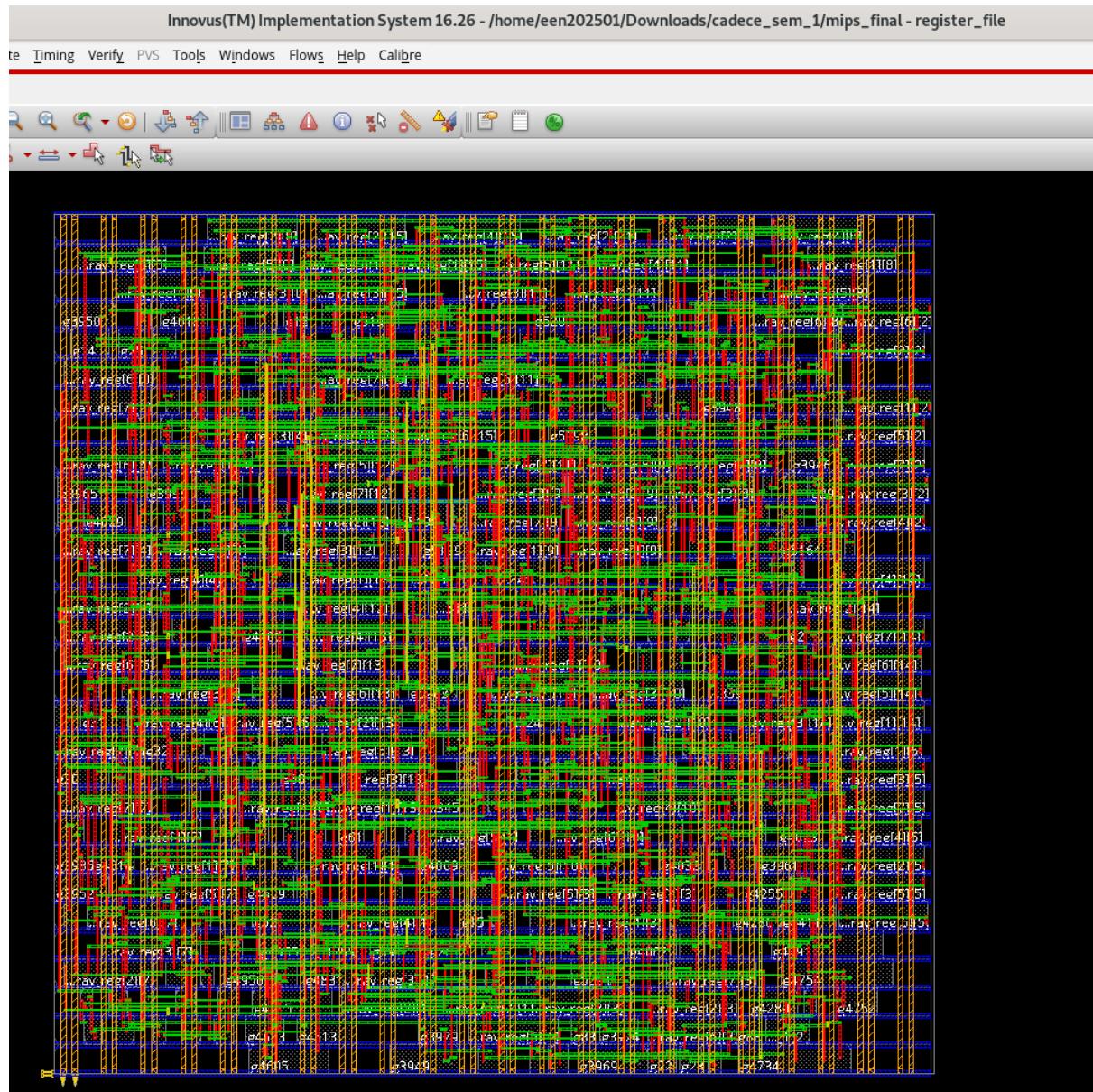
Hold views included:  

best_case  

+-----+-----+-----+
|   Setup mode | all    | default |
+-----+-----+-----+
|       WNS (ns):| 0.000  | 0.000 |
|       TNS (ns):| 0.000  | 0.000 |
| Violating Paths:| 0      | 0      |
| All Paths:| 0      | 0      |
+-----+-----+-----+
+-----+-----+-----+
|   Hold mode | all    | default |
+-----+-----+-----+
|       WNS (ns):| 0.000  | 0.000 |
|       TNS (ns):| 0.000  | 0.000 |
| Violating Paths:| 0      | 0      |
| All Paths:| 0      | 0      |
+-----+-----+-----+
+-----+-----+-----+
|           Real          |           Total          |
|           | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| DRVs      | 0 (0)        | 0.000    | 0 (0)        |
| max_cap   | 0 (0)        | 0.000    | 0 (0)        |
| max_tran  | 0 (0)        | 0        | 0 (0)        |
| max_fanout| 0 (0)        | 0        | 0 (0)        |
| max_length| 0 (0)        | 0        | 0 (0)        |
+-----+-----+-----+-----+
Density: 67.062%
Routing Overflow: 0.00% H and 0.00% V
-----
**optDesign ... cpu = 0:00:07, real = 0:00:12, mem = 2075.7M, totSessionCpu=0:02:29 **
*** Finished optDesign ***
innovus 3>
innovus 3> innovus 3> []

```

REGISTER_FILE



1. GEOMETRY

```

innovus 1> *** Starting Verify Geometry (MEM: 1935.2) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
    VERIFY GEOMETRY ..... Starting Verification
    VERIFY GEOMETRY ..... Initializing
    VERIFY GEOMETRY ..... Deleting Existing Violations
    VERIFY GEOMETRY ..... Creating Sub-Areas
        ..... bin size: 2880
    VERIFY GEOMETRY ..... SubArea : 1 of 1
    VERIFY GEOMETRY ..... Cells : 0 Viols.
    VERIFY GEOMETRY ..... SameNet : 0 Viols.
    VERIFY GEOMETRY ..... Wiring : 0 Viols.
    VERIFY GEOMETRY ..... Antenna : 0 Viols.
    VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
    Cells : 0
    SameNet : 0
    Wiring : 0
    Antenna : 0
    Short : 0
    Overlap : 0
End Summary

    Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.2 MEM: 108.1M)

innovus 1> 

```

2. DRC

```

innovus 1> #-disable_rules " color cut_spacing enclosure eol_spacing min_area min_cut min_step protrusion
"
                                         # enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure
re color min_step protrusion min_area out_of_die} list, default= , user setting
#-exclude_pg_net true                  # bool, default=false, user setting
#-ignore_trial_route true             # bool, default=false, user setting
#-report register_file.drc.rpt       # string, default="", user setting
*** Starting Verify DRC (MEM: 2043.3) ***

    VERIFY DRC ..... Starting Verification
    VERIFY DRC ..... Initializing
    VERIFY DRC ..... Deleting Existing Violations
    VERIFY DRC ..... Creating Sub-Areas
    VERIFY DRC ..... Using new threading
    VERIFY DRC ..... Sub-Area: {0.000 0.000 55.165 54.000} 1 of 1
    VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

    Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***

```

3. CONNECTIVITY

```
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 20:29:29 2021

Design Name: register_file
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (55.1650, 54.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

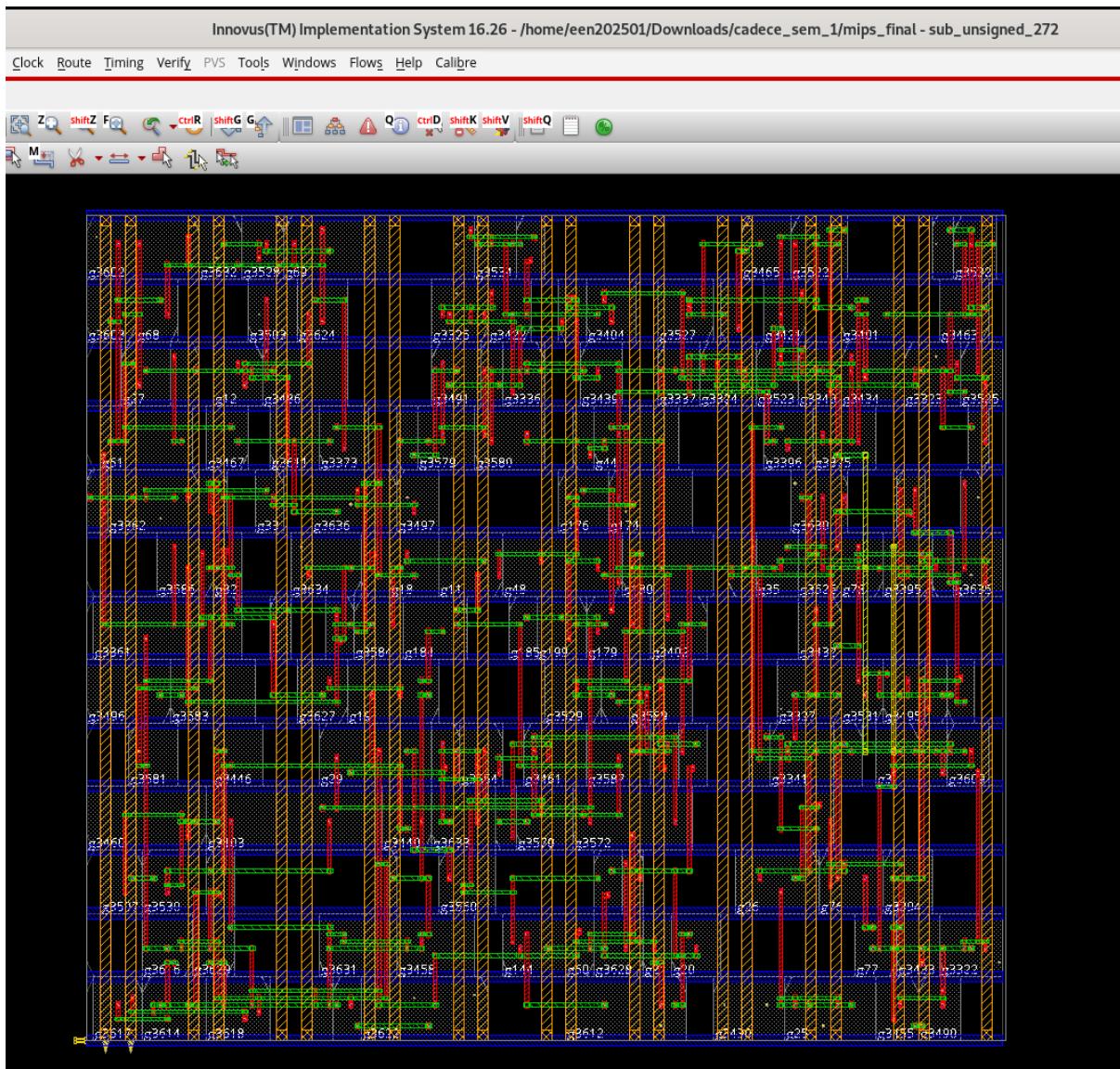
Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 20:29:29 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0  MEM: 0.000M)
```

4. TIMMING

SUB_UNSIGNED



1. GEOMETRY

```

innovus l> *** Starting Verify Geometry (MEM: 1849.5) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this
release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.

VG: elapsed time: 0.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.1 MEM: 106.6M)

```

2. DRC

```

"
# enums={jog2jog_spacing eol_spacing cut_spacing min_cut enclosure_color min_step protrusion min_area out_of_die}_list, default= , user setting
-exclude_pg_net true # bool, default=false, user setting
-ignore_trial_route true # bool, default=false, user setting
-report sub_unsigned 272.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 1956.1) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 26.090 23.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***
]
```

3. CONNECTIVITY

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar 5 20:40:57 2021

Design Name: sub_unsigned_272
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (26.0900, 23.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar 5 20:40:57 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 1> 
```

4. TIMMING

```
-----  

          optDesign Final Summary  

-----  

Setup views included:  

worst_case  

Hold views included:  

best_case  

-----  

+-----+-----+-----+  

|   Setup mode   |   all   | default |  

+-----+-----+-----+  

|       WNS (ns):|  0.000  |  0.000  |  

|       TNS (ns):|  0.000  |  0.000  |  

| Violating Paths:|    0    |    0    |  

| All Paths:     |    0    |    0    |  

+-----+-----+-----+  

-----  

+-----+-----+-----+  

|   Hold mode    |   all   | default |  

+-----+-----+-----+  

|       WNS (ns):|  0.000  |  0.000  |  

|       TNS (ns):|  0.000  |  0.000  |  

| Violating Paths:|    0    |    0    |  

| All Paths:     |    0    |    0    |  

+-----+-----+-----+  

-----  

+-----+-----+-----+  

|           Real           |           Total           |  

|      | Nr nets(terms) | Worst Vio | Nr nets(terms) |  

|      +-----+-----+-----+  

| max_cap |    0 (0)    |  0.000  |    0 (0)    |  

| max_tran |   0 (0)    |  0.000  |   0 (0)    |  

| max_fanout |  0 (0)    |    0    |  0 (0)    |  

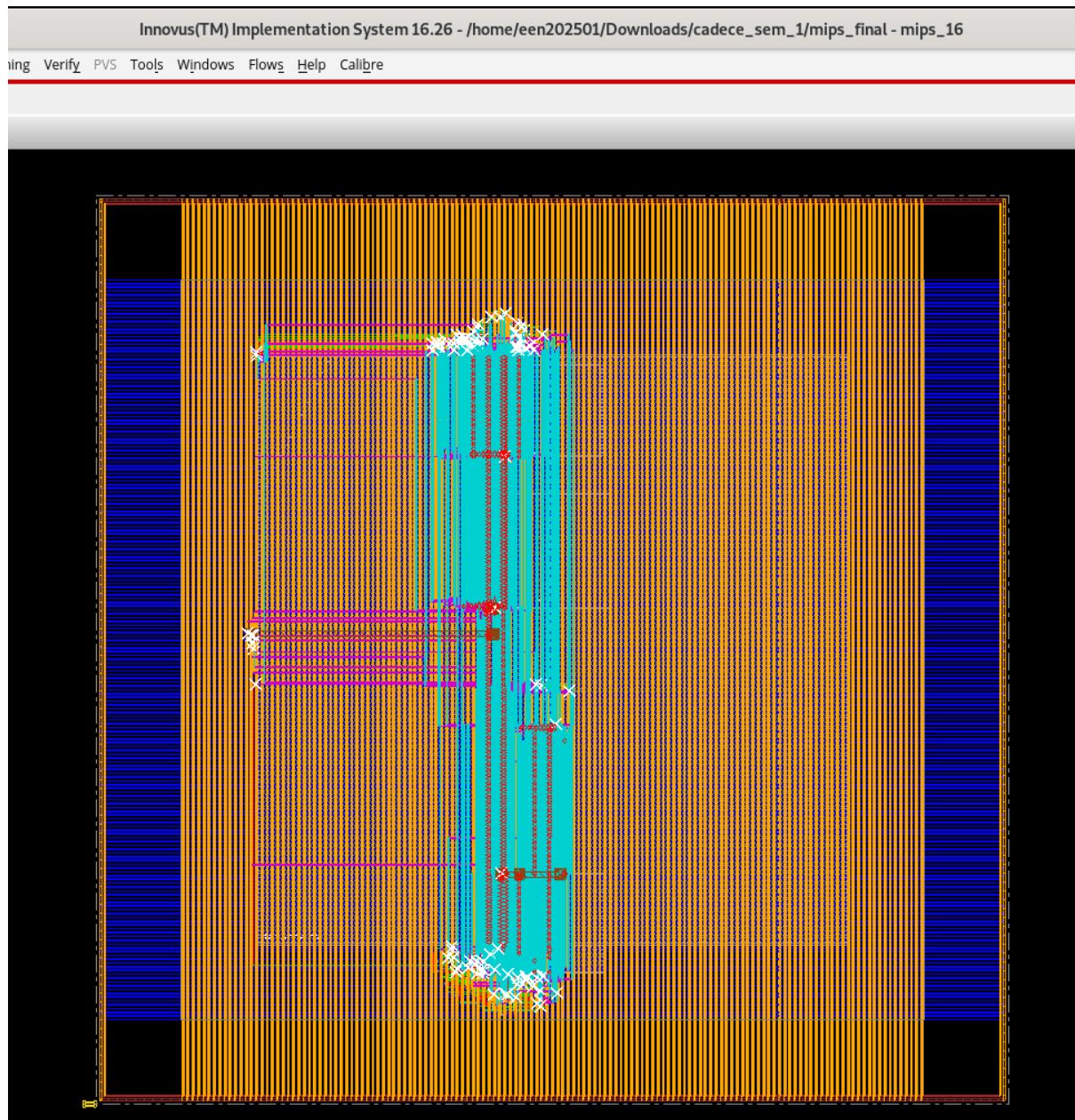
| max_length |  0 (0)    |    0    |  0 (0)    |  

+-----+-----+-----+  

Density: 68.225%
Routing Overflow: 0.00% H and 0.00% V
-----  

**optDesign ... cpu = 0:00:07, real = 0:00:27, mem = 2079.2M, totSessionCpu=0:02:26 **
*** Finished optDesign ***
innovus 3>
innovus 3> innovus 3> 
```

Mips_16(FINAL)



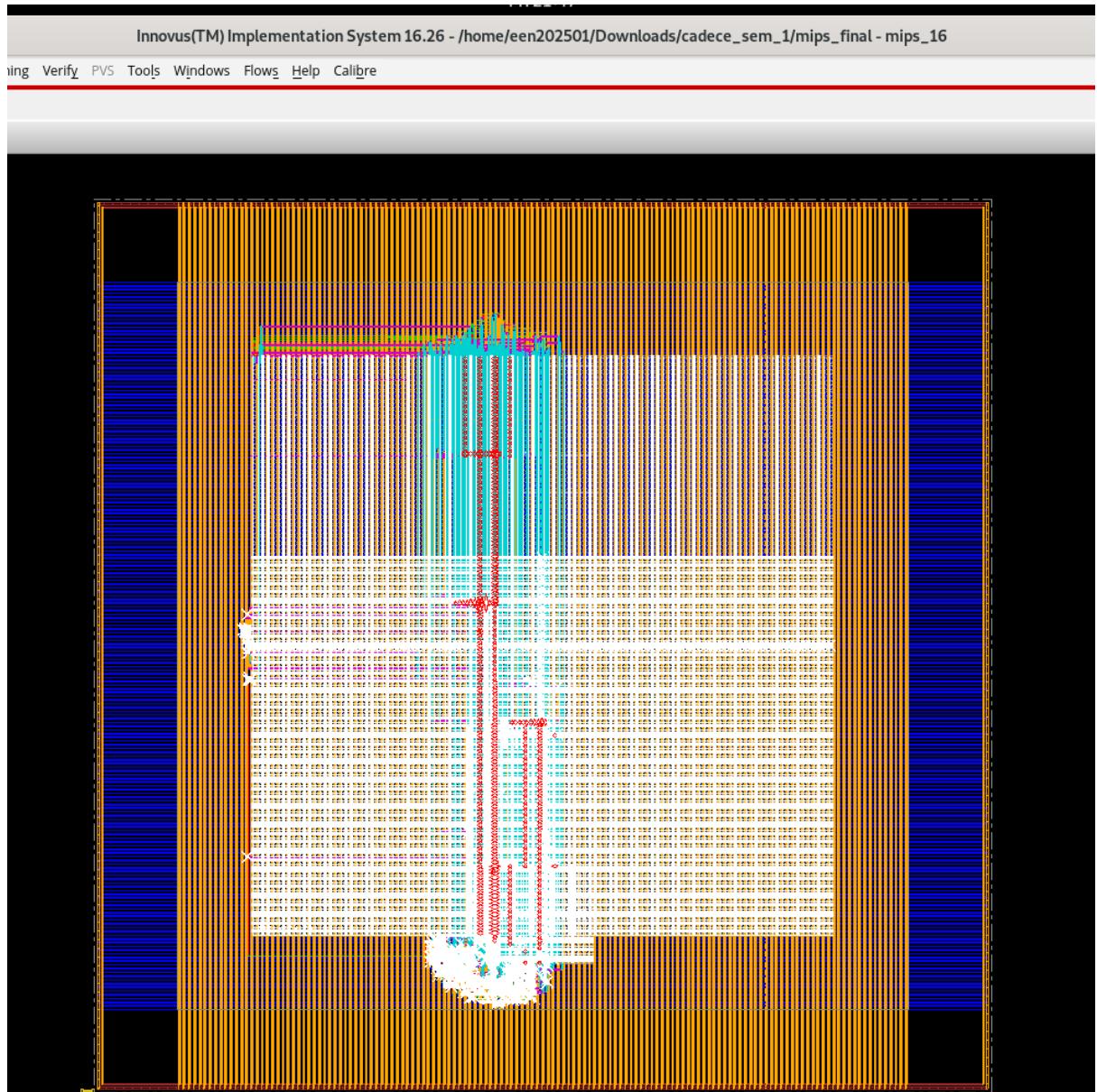
1. GEOMETRY

```

innovus l> *** Starting Verify Geometry (MEM: 2390.6) ***
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Generating Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
VERIFY GEOMETRY ..... bin size : 2880
VERIFY GEOMETRY ..... SubArea : 1 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 75 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... SubArea : 1 complete 75 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 2 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 7 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... SubArea : 2 complete 7 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 3 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 109 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... SubArea : 3 complete 109 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 4 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 4 complete 0 Viols. 0 Wrngs.
VG: Elapsed time: 0.00
Begin Summary
Cells : 0
SameNet : 191
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 191 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.5 MEM: 0.0M)
innovus l> []

```

2. DRC



3. CONNECTIVITY

```
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 21:48:01 2021

Design Name: mips_16
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (432.0000, 431.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 21:48:01 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)
```

4. Timing

```

-----
optDesign Final Summary
-----

Setup views included:
worst_case
Hold views included:
best_case

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| -0.725 | -0.725 | 1.045 |
| TNS (ns):| -2.326 | -2.326 | 0.000 |
| Violating Paths:| 6 | 6 | 0 |
| All Paths:| 32 | 16 | 16 |
+-----+-----+-----+-----+

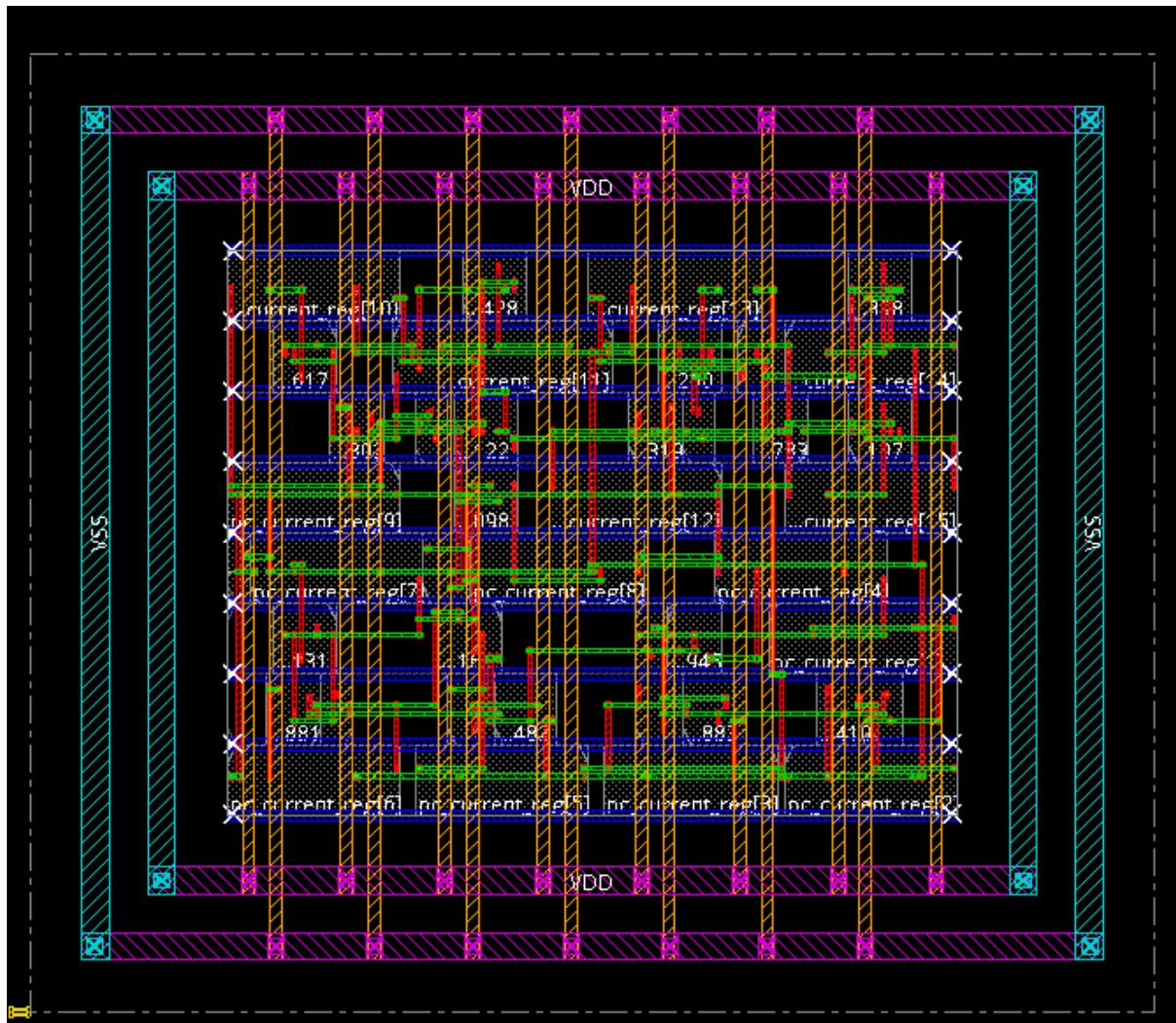
+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| 0.016 | 0.132 | 0.016 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 32 | 16 | 16 |
+-----+-----+-----+-----+

+-----+-----+-----+-----+
| DRVs | Real | Total |
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 1 (1) | -0.011 | 1 (1) |
| max_tran | 1 (17) | -0.330 | 1 (17) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

Density: 1.652%
Routing Overflow: 0.35% H and 3.11% V
-----
**optDesign ... cpu = 0:00:08, real = 0:00:09, mem = 2444.8M, totSessionCpu=0:03:55 ***
*** Finished optDesign ***
0
innovus 3>
innovus 3> innovus 3> []

```

MIPS_16(ONLY)



```
innovus 1> Begin checking placement ... (start mem=1999.4M, init mem=1999.4M)
*info: Placed = 43
*info: Unplaced = 0
Placement Density:69.22%(185/268)
Placement Density (including fixed std cells):69.22%(185/268)
Finished checkPlace (cpu: total=0:00:00.1, vio checks=0:00:00.0; mem=1999.4M)
innovus 1> █
```

```

timeDesign Summary

Setup views included:
worst_case

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | -0.127 | -0.127 | 1.411 |
| TNS (ns): | -0.155 | -0.155 | 0.000 |
| Violating Paths: | 2 | 2 | 0 |
| All Paths: | 30 | 15 | 15 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 69.22%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 0.49 sec
Total Real time: 1.0 sec
Total Memory Usage: 2055.839844 Mbytes
innovus 1> █

```

```

optDesign Final Summary

Setup views included:
worst_case

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.056 | 0.056 | 2.084 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 30 | 15 | 15 |
+-----+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+

```

```

-----  

          timeDesign Summary  

-----  

Hold views included:  

  best_case  

+-----+-----+-----+-----+
|     Hold mode    |   all   | reg2reg | default |
+-----+-----+-----+-----+
|       WNS (ns): | -0.119  |  0.057  | -0.119  |
|       TNS (ns): | -1.769  |  0.000  | -1.769  |
| Violating Paths: |    15    |    0    |    15    |
|   All Paths:    |    30    |    15   |    15   |
+-----+-----+-----+-----+
Density: 74.059%
Routing Overflow: 0.00% H and 0.00% V
-----  

Reported timing to dir timingReports
Total CPU time: 0.35 sec
Total Real time: 1.0 sec
Total Memory Usage: 2290.917969 Mbytes
innovus 1> 
```

```

-----  

          optDesign Final Summary  

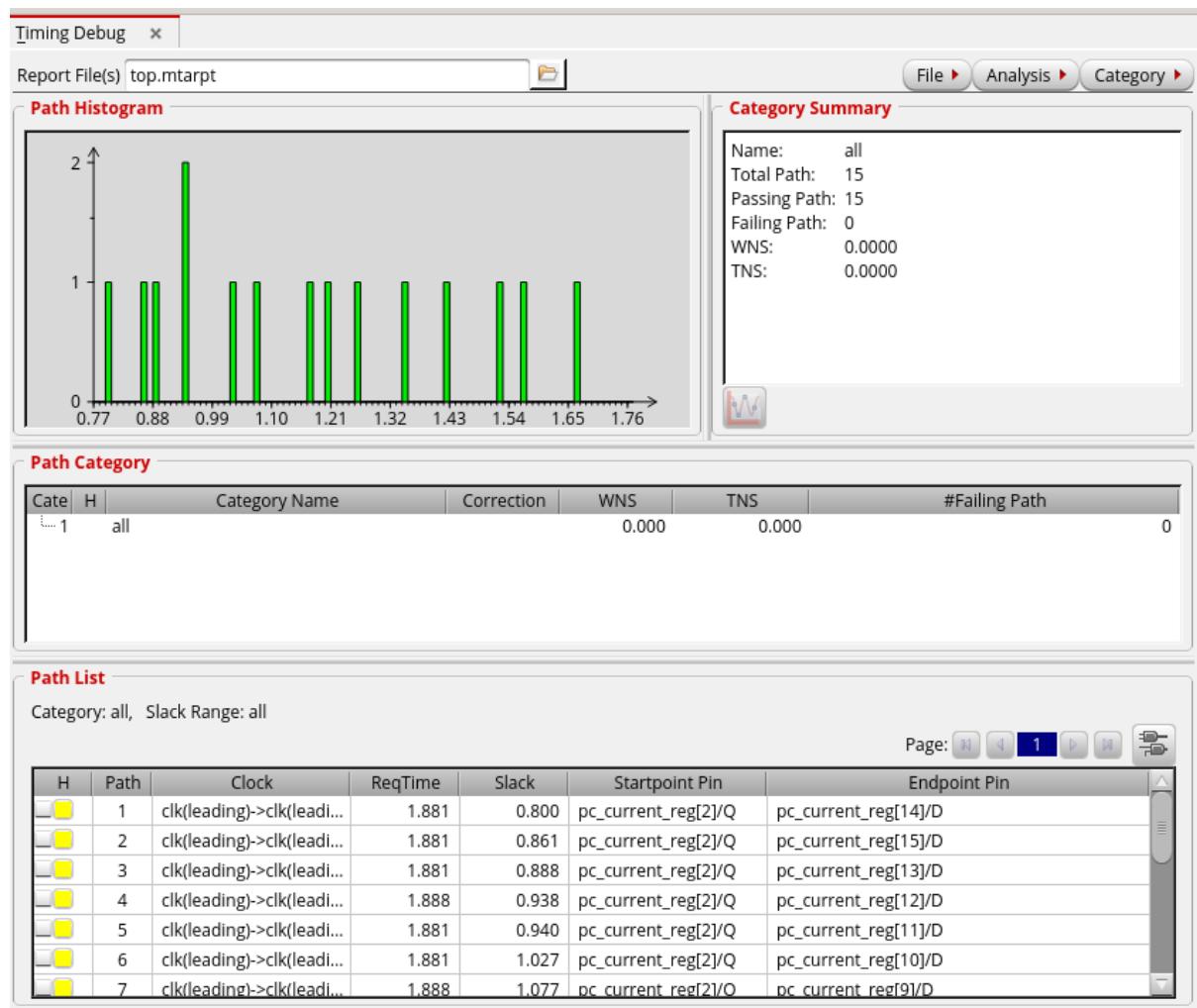
-----  

Setup views included:  

  worst_case
Hold views included:  

  best_case  

+-----+-----+-----+-----+
|     Setup mode    |   all   | reg2reg | default |
+-----+-----+-----+-----+
|       WNS (ns): |  0.056  |  0.056  |  1.269  |
|       TNS (ns): |  0.000  |  0.000  |  0.000  |
| Violating Paths: |    0    |    0    |    0    |
|   All Paths:    |    30   |    15   |    15   |
+-----+-----+-----+-----+
+-----+-----+-----+-----+
|     Hold mode    |   all   | reg2reg | default |
+-----+-----+-----+-----+
|       WNS (ns): |  0.005  |  0.057  |  0.005  |
|       TNS (ns): |  0.000  |  0.000  |  0.000  |
| Violating Paths: |    0    |    0    |    0    |
|   All Paths:    |    30   |    15   |    15   |
+-----+-----+-----+-----+
+-----+-----+-----+-----+
|           |          Real          |          Total          | |
|   DRVs    |          |          |          |
|           |  Nr nets(terms)  | Worst Vio |  Nr nets(terms)  |
+-----+-----+-----+-----+
| max_cap  |    0 (0)    |  0.000  |    0 (0)    |
| max_tran |    0 (0)    |  0.000  |    0 (0)    |
| max_fanout |    0 (0)    |    0    |    0 (0)    |
| max_length |    0 (0)    |    0    |    0 (0)    |
+-----+-----+-----+-----+
Density: 75.134%
Routing Overflow: 0.00% H and 0.00% V
**optDesign ... cpu = 0:00:07, real = 0:00:08, mem = 2365.3M, totSessionCpu=0:18:12 **
```



```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar 5 01:15:53 2021

Design Name: mips_16
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (28.6000, 24.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar 5 01:15:53 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 01:15:53 2021

Design Name: mips_16
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (28.6000, 24.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 01:15:53 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

```
-report mips_16.drc.rpt          # string, default="", user setting
*** Starting Verify DRC (MEM: 2748.4) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 28.600 24.400} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Mar  5 01:15:53 2021

Design Name: mips_16
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (28.6000, 24.4000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Mar  5 01:15:53 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```