universität freiburg

ReTI-Tools: A VSCode Extension for ReTI Assembly Programming

Bachelorthesis for the B. Sc. Informatik at University of Freiburg

Presenter: Malte Pullich

Chair of Computer Architecture

Examiner: Prof. Dr. Armin Biere
Adviser: Dr. Mathias Fleury, Tobias Faller
Freiburg, 12.11.2025

Agenda

1. **Motivation:** State of the Art and Usage
2. **Background:** ReTI Architecture and Differences between both Versions
3. **Approach:** Improving on Interactivity and Adding Features
4. **Results:** Improvement on existing Features, new Features
5. **Conclusion:** Goals Reached & Future Work

Motivation

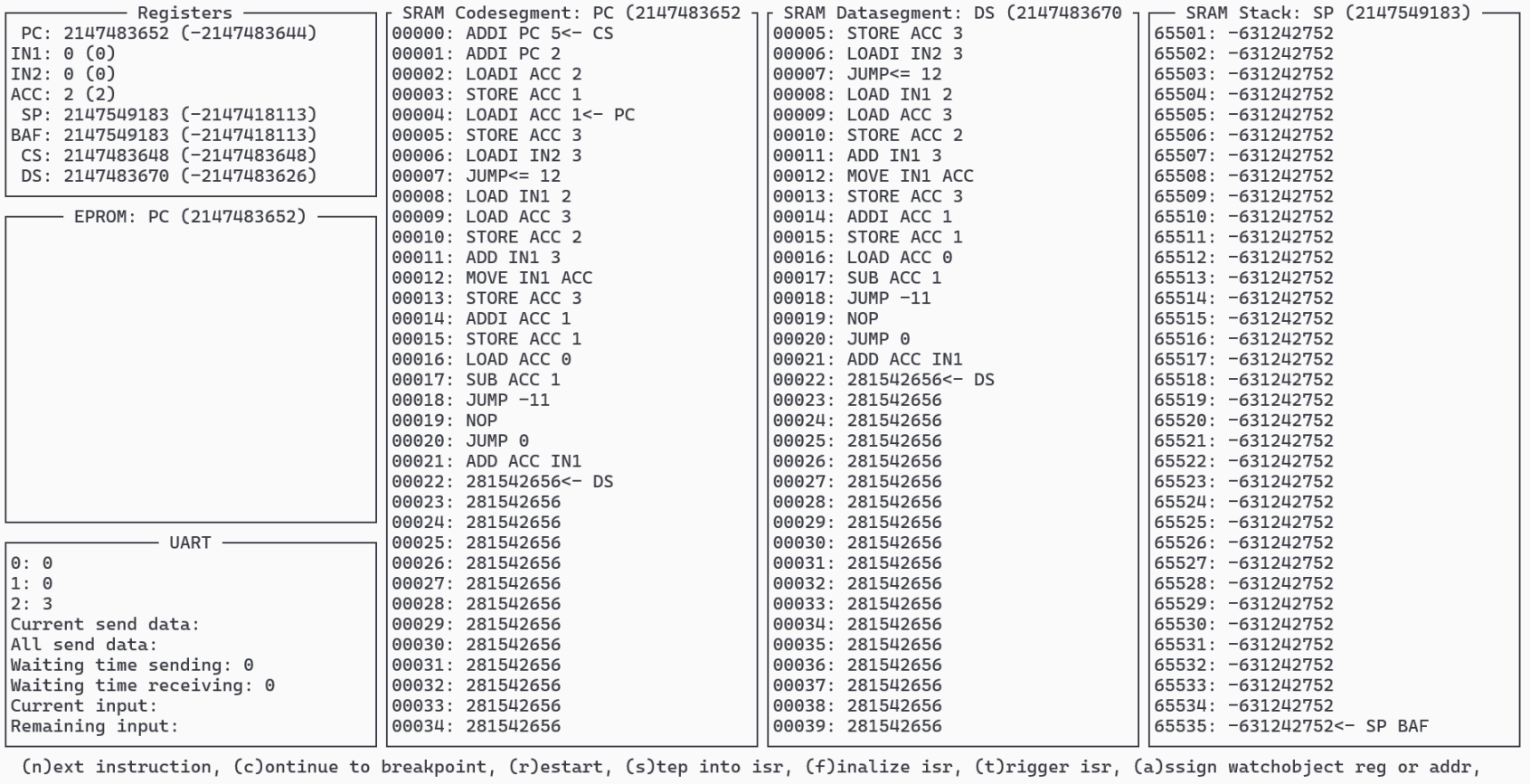

Fig.1 : Screenshot of the Emulator by Jürgen Mattheis [1]

Emulator by Jürgen Mattheis:

- OS-dependent (only Linux support)
- Workflow requires switching between editor and debugger

Motivation

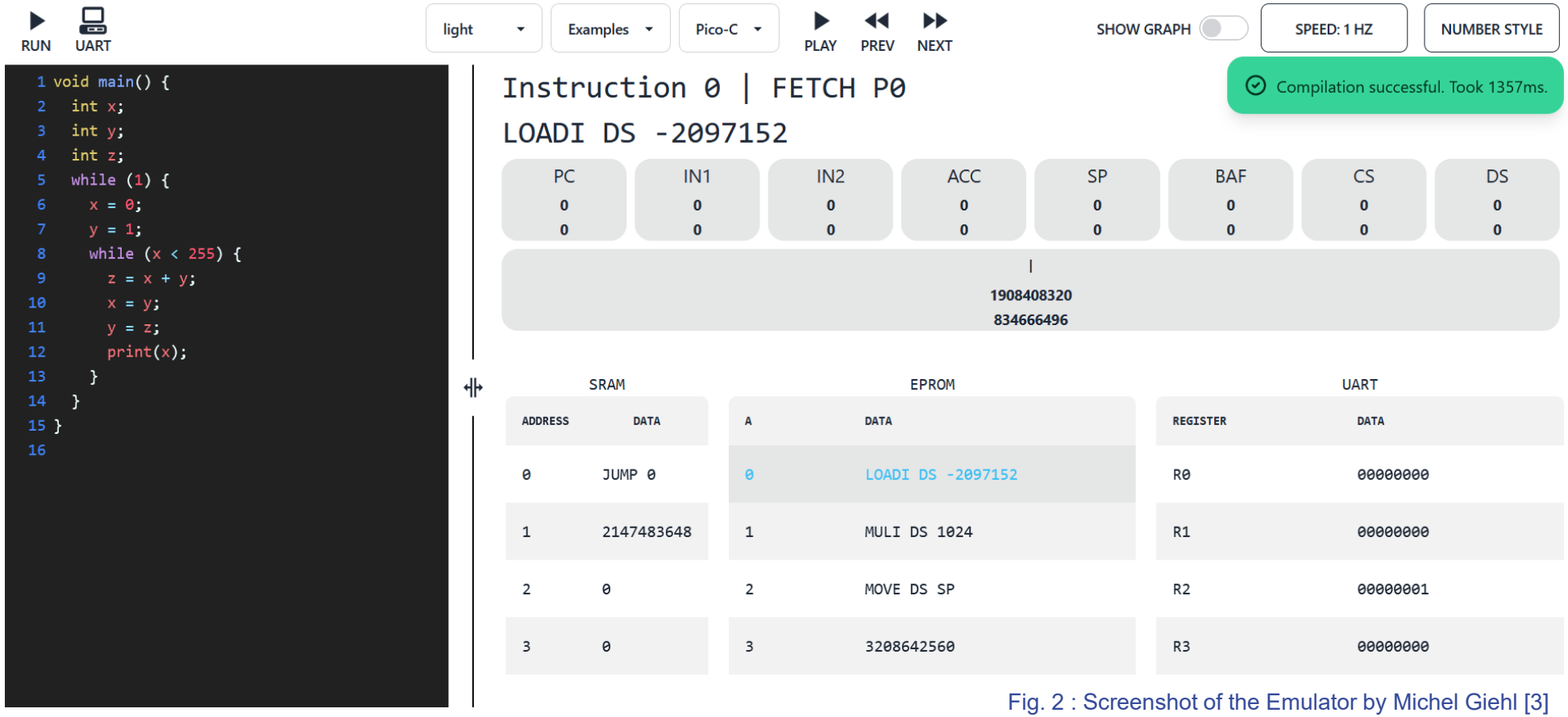

Fig. 2 : Screenshot of the Emulator by Michel Giehl [3]

Emulator by Michel Giehl:

- Web app, as of Monday 10th November, only accessible through Uni network
- Doesn’t support interrupts

ReTi-Architecture

```
JUMP<= 12
    LOAD IN1 2
    LOAD ACC 3
    STORE 2
    ADD IN1 3
    MOVE IN1 ACC
    STORE 3
    ADDI ACC 1
    STORE 1
    ; Check if i <
    LOAD ACC 0
    SUB ACC 1
JUMP -11
NOP
```

Fig: 3 Excerpt of a ReTI program that calculates Fibonacci numbers

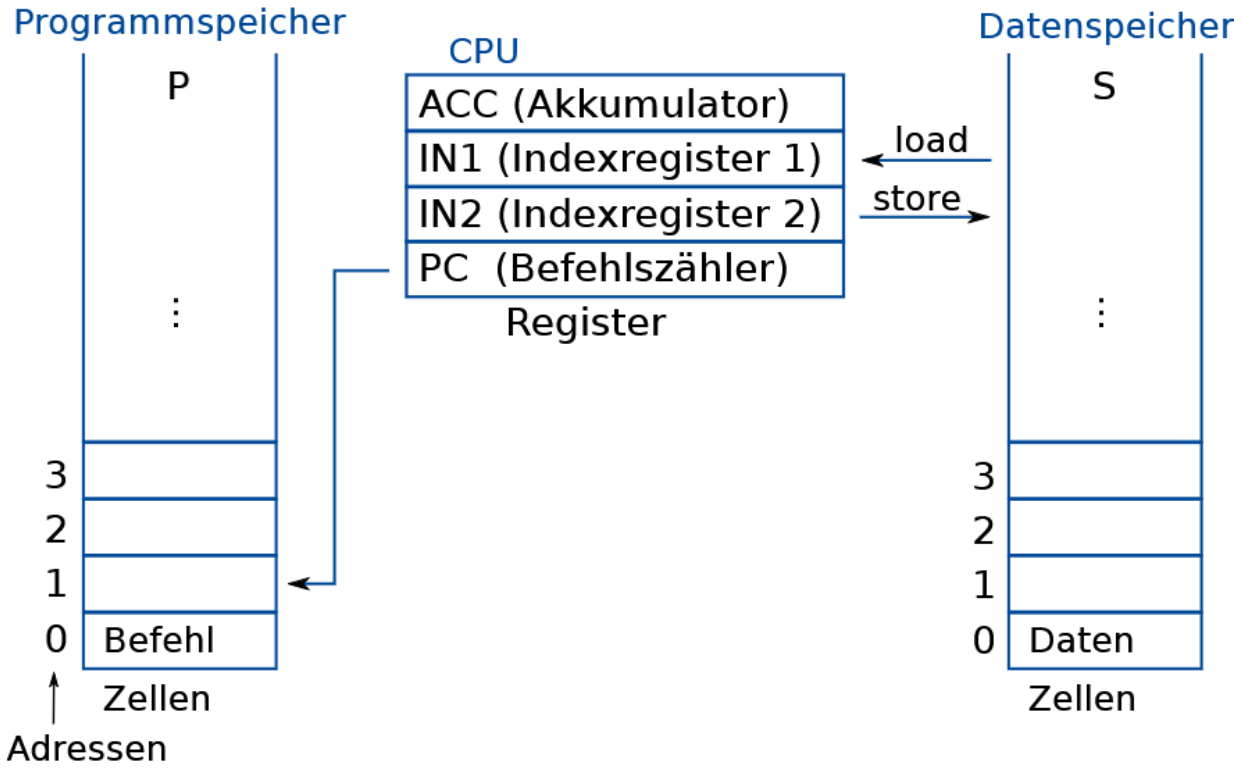

Fig 4: Abstract ReTI architecture [2]

Differences Between the ReTI Variants

ReTI-I (Technical Informatics):

- **Memory is single SRAM**
- **1 new internal registers:**
  - **I,** Instruction Register
- **No Interrupts**

ReTI-II (Operating Systems):

- **Memory split into SRAM, EPROM, UART**
- **4 new user-visible registers:**
  - **SP,** Stack Pointer
  - **BAF,** Begin Active Frame
  - **CS,** (Begin of) Code Segment
  - **DS,** (Begin of) Data Segment
- **Interrupts:**
  - Interrupt controller
  - New register **IVN**
- **New instruction encoding (3 bits for registers)**
- **New instructions (MUL, DIV, MOD)**

Approach

Goal: Improve accessibility and responsiveness to provide a better educational experience.

Extend existing VS Code extension:

- Most used IDE
- OS-independent
- Same tool for both lectures

Identified key features to extend:

- Emulator
- Debugger
- Language Server

Additionally:

- Provide a memory view

Approach

Extension's Architecture

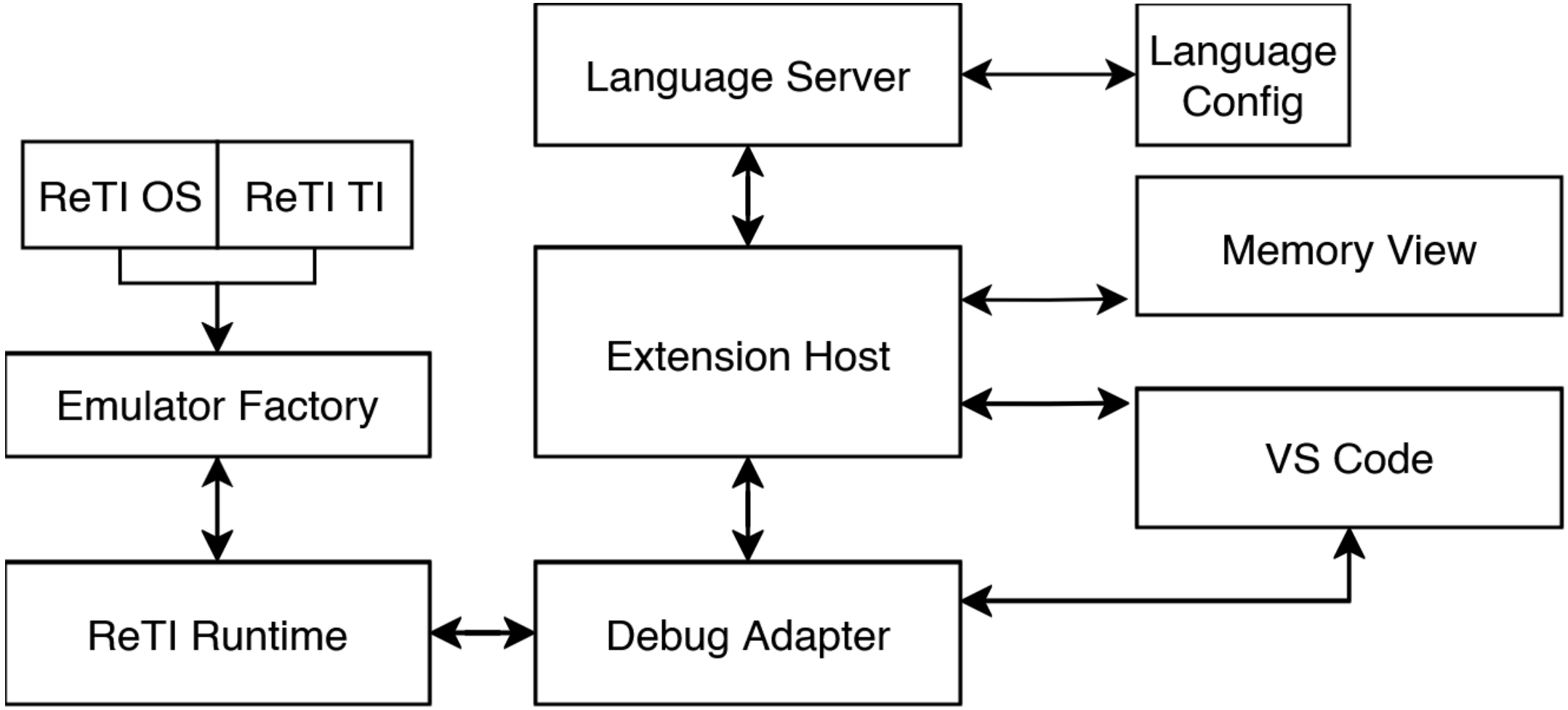

Fig. 5: Diagram illustrating the interaction between the different components of the extension.

Results

Support for Both Architectures

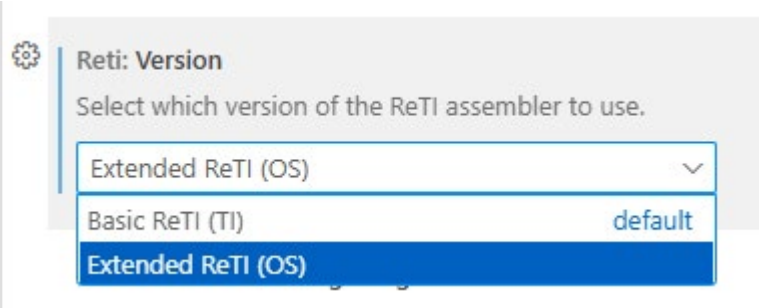

Fig 6: Screenshot of the new setting in VS Code

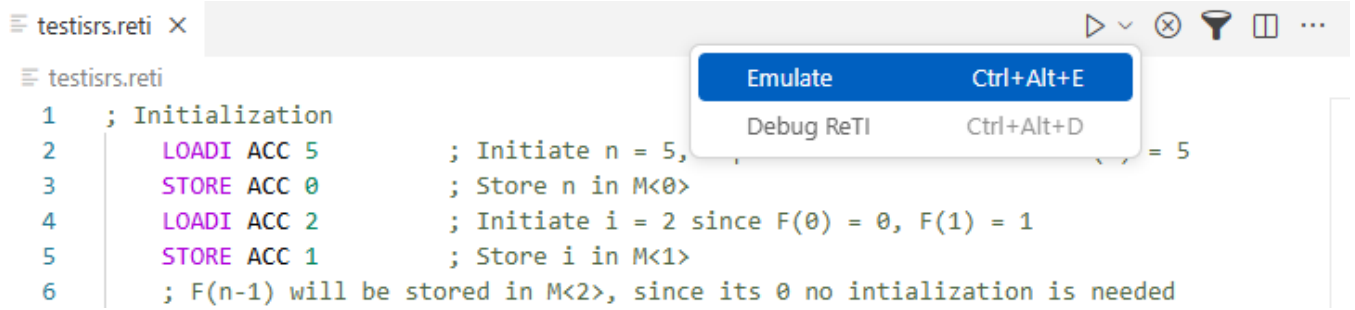

Fig 7: Example Usage of the ReTI Emulation in VS Code

- Added setting to specify desired version
- Affects all features (emulator, debugger, language server) except quiz
- Emulator now callable in .reti files for ReTI-II (OS)

Results

Language Server

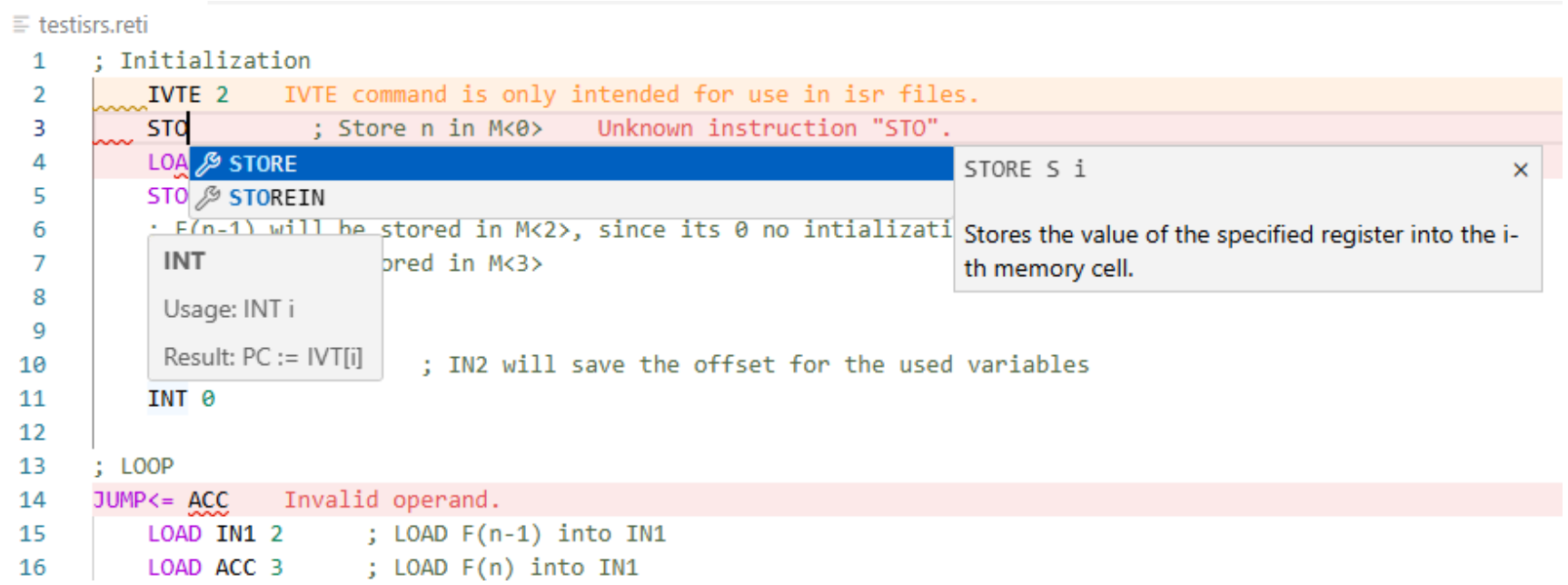

Fig 8: Screenshot from VS Code highlighting LSP Features

Features:

- Syntax Highlighting
- Tooltips (syntax and documentation)
- Realtime compilation and checking
- Autocomplete suggestions

Results

Debugger and Memory View

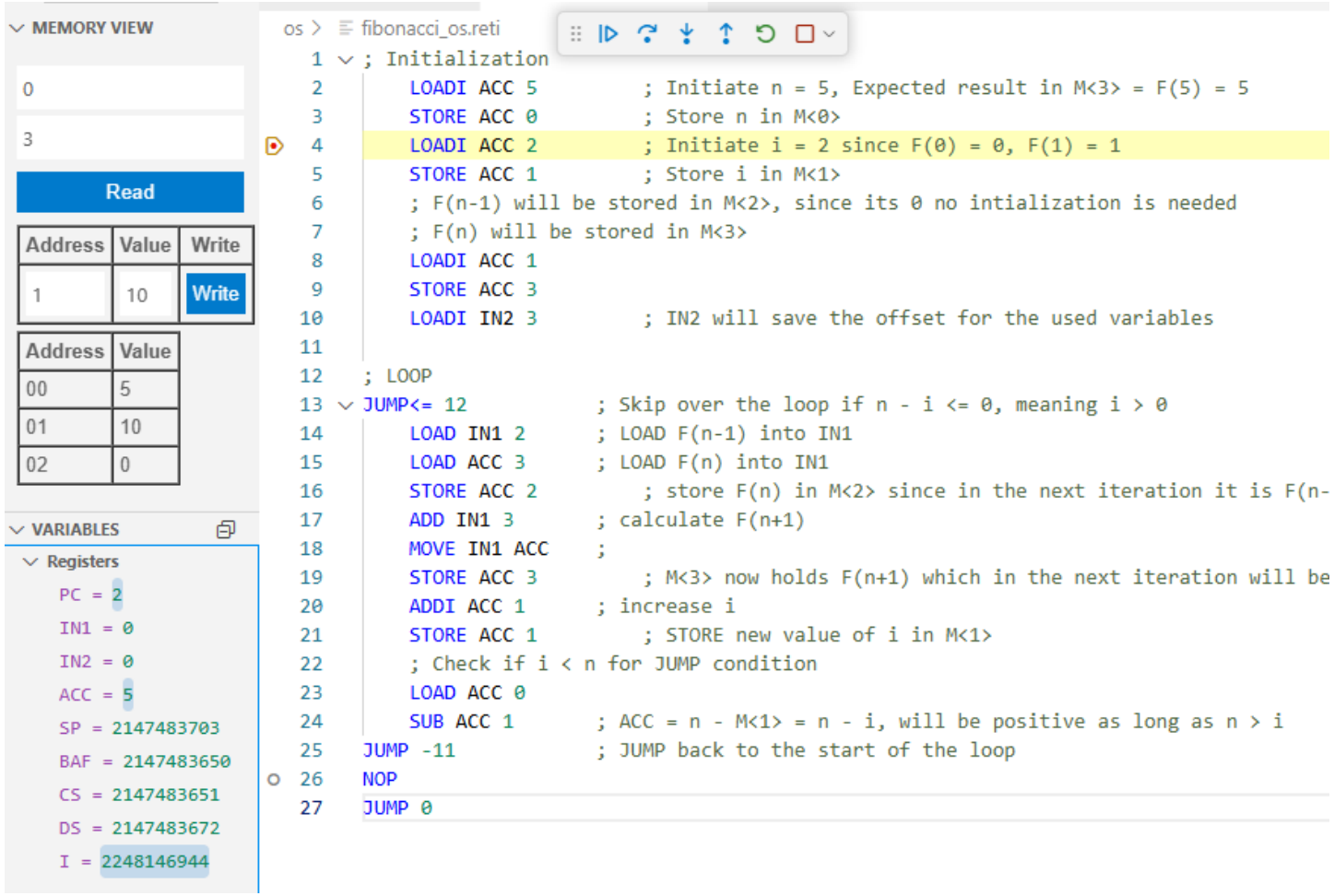

Fig 9: Screenshot of running ReTI-Debug session

Features both architectures:

- Reading and writing register values
- Reading and writing memory
- Breakpoints

Features for the ReTI-II (OS):

- Switching between main program and interrupt service routine file
- Updated Stepping Logic to support interrupts

Results

Debugger, Stepping

testisrs.reti

```
; Initialization
    LOADI ACC 5         ; Initiate n = 5, Expected result in M<3> = F(5) = 5
    STORE ACC 0         ; Store n in M<0>
    LOADI ACC 2         ; Initiate i = 2 since F(0) = 0, F(1) = 1
    STORE ACC 1         ; Store i in M<1>
    ; F(n-1) will be stored in M<2>, since its 0 no intialization is needed
    ; F(n) will be stored in M<3>
    LOADI ACC 1
    STORE ACC 3
    LOADI IN2 3         ; IN2 will save the offset for the used variables
    INT 0

; LOOP
JUMP<= 12           ; Skip over the loop if n - i <= 0, meaning i > 0
    LOAD IN1 2      ; LOAD F(n-1) into IN1
    LOAD ACC 3      ; LOAD F(n) into IN1
    STORE ACC 2         ; store F(n) in M<2> since in the next iteration it is F(n-1)
    ADD IN1 3       ; calculate F(n+1)
    MOVE IN1 ACC    ;
    NOP
    STORE ACC 3         ; M<3> now holds F(n+1) which in the next iteration will be F(n)
    ADDI ACC 1      ; increase i
    STORE ACC 1         ; STORE new value of i in M<1>
    ; Check if i < n for JUMP condition
    LOAD ACC 0
    INT 1
    SUB ACC 1       ; ACC = n - M<1> = n - i, will be positive as long as n > i
JUMP -11            ; JUMP back to the start of the loop
NOP
JUMP 0
```

isrs.reti

```
; Example routine that restores registers
IVTE 0
SUBI SP 7
STOREIN SP IN1 7
STOREIN SP IN2 6
STOREIN SP ACC 5

STOREIN SP CS 2
STOREIN SP DS 1

LOADI IN1 2
LOADI IN2 5
SUB IN2 IN1
LOADI ACC 1

LOADIN SP DS 1
LOADIN SP CS 2
LOADIN SP ACC 5
LOADIN SP IN2 6
LOADIN SP IN1 7
ADDI SP 7
RTI
; Example routine that keeps register values.
IVTE 1
LOADI ACC 2
MOVE ACC IN1
LOADI IN2 5
SUB IN2 IN1
LOADI ACC 1
RTI
```

Fig. 10: Screenshots of running ReTI-Debug session

Conclusion
Goals Reached

- All features (emulator, debugger, language server) extended to cover both versions ✓
- Memory view allows easier monitoring and manipulation of memory ✓
- Debugger and Language Server offer
  - Syntax Highlighting ✓
  - Realtime Compilation ✓
  - Code Completion Suggestions ✓
  - Executing Code and Inspecting/Manipulating ReTI State ✓
- Extension provides familiar programming workflow and OS-independent use ✓

Conclusion

Limitations & Future Work

- **Emulate UART interface**
- **Make debug adapter independent from VS Code (embedding in other editors/tools)**
- **Integrate Pico-C compiler**
- **Add datapaths visualization [3]:**

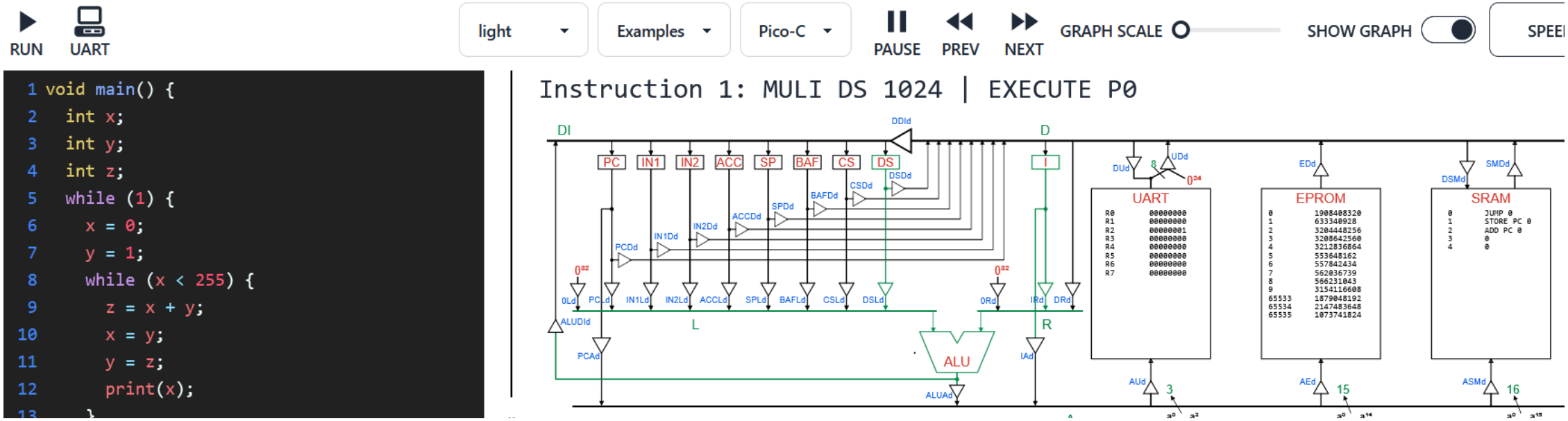

Fig. 11: Screenshot of ReTI-Emulator with Datapath-Visualization [3]

Extra:
Language-Server-Protocol

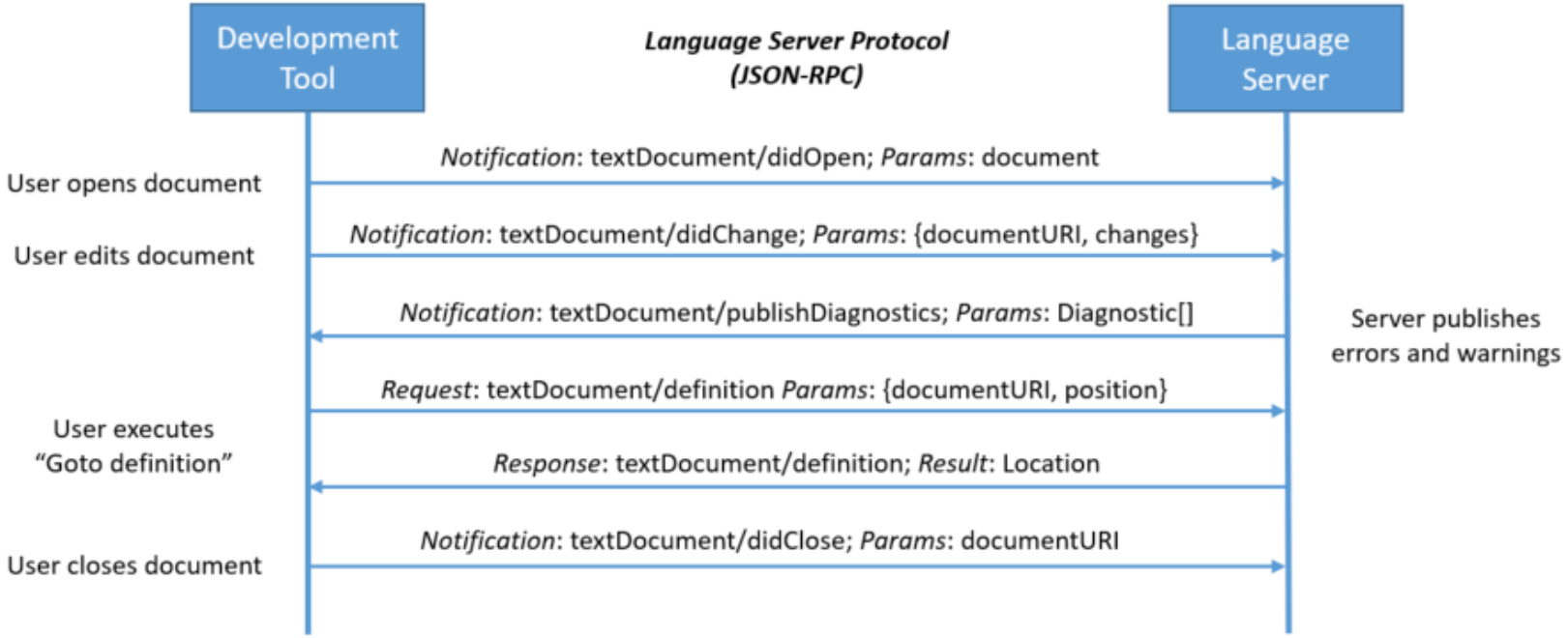

Fig. 12: Example for Communication between Tool and Server in the Language-Server-Protocol [4]

Extra:
Debug-Adapter-Protocol

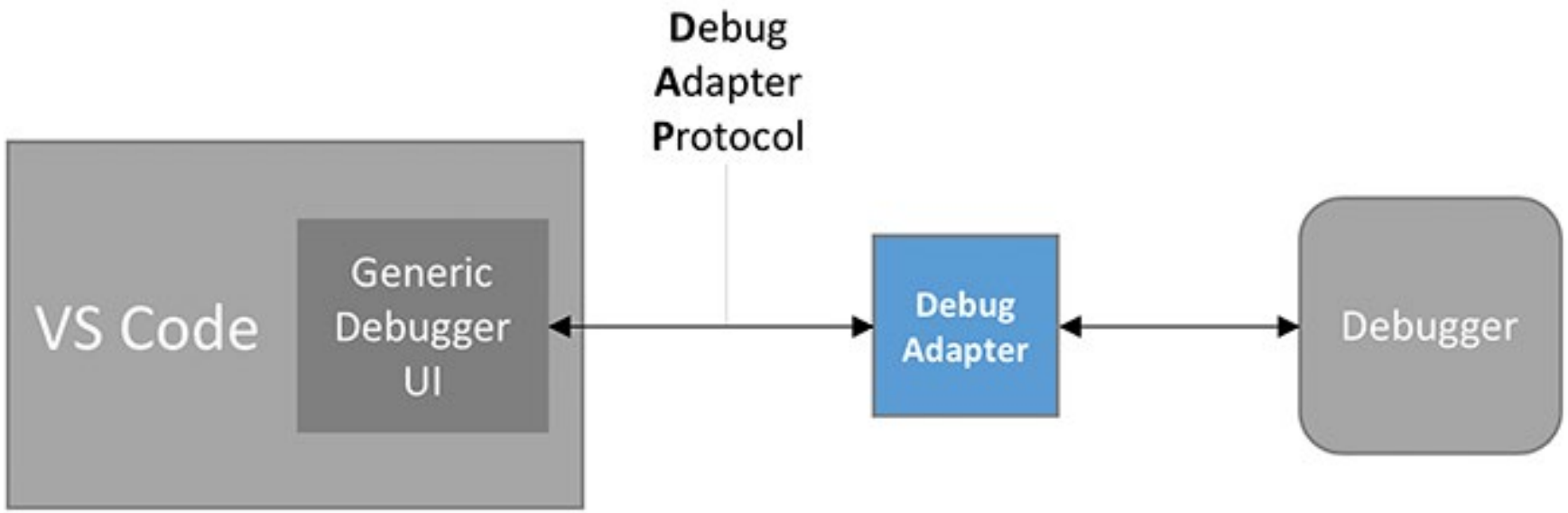

Fig. 13: VS Code Debug Architecture [5]

References

[1]: RETI-Emulator by Jürgen Mattheis, https://github.com/matthejue/RETI-Emulator
[2]: Technische Informatik – Kapitel 2 – Kodierung, Prof. Dr. Armin Biere, University of Freiburg, SS 2024
[3]: RETI-Emulator by Michel Giehl, github.com/michel-giehl/Reti-Emulator
[4]: Microsoft *Language Server Protocol - Sequence Diagram*. Retrieved 13. July 2025, from https://microsoft.github.io/language-server-protocol/overviews/lsp/overview/
[5]:Microsoft. *VS Code Debug Architecture*. Retrieved 13. July 2025, from https://code.visualstudio.com/api/extension-guides/debugger-extension