Khalifa University of Science, Technology and Research

Electronic Engineering Department

ELCE333: Microprocessor Systems Laboratory

Laboratory Experiment No. 6

HCSI2 Interrupts

Lab Partners

Leena ElNeel	100037083
Muna Darweesh	100035522
Shamsah AlNabooda	100036984

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Lab Instructors:

Mahmoud Khonji

Mohammed Ali Saif Al Zaabi

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Pre-Lab Questions:

1. What is the address of the IRQ and the PTH interrupt in the HCS12 interrupt vector table?

For IRQ the address is 0xFFF2U

For PTH the address is 0xFFCCU

2. Upon Reset, IRQ and XIRQ hardware interrupts are ____*edge*_____ (edge**, level) triggered.**
It is edge triggered.

3. True or False. An interrupt is assigned to each bit of PTH, instead of a single interrupt to the entire PTH.
True.

4. True or False. Upon Reset, the PTH interrupt is masked
True.

5. In HCS12, indicate how you enable the peripheral interrupts globally.

In order to globally enable interrupts the assembly command clear global interrupt flag has to be called "`__asm CLI;`".

6.Which register is used to make PTH interrupt level- or edge- triggered?
Some of the HCS12 IO has edge-triggered (rising or falling) interrupt capability such as PTH, In order to enable such interrupt capability of any of PTH bits the corresponding bit has to be set in the PTH Interrupt Enable Register (PIEH).