

## **Module Name: Microprocessor Systems Laboratory**

**Module Code: ELCE333** 

## Laboratory Experiment No. 6

**Pre-Lab Report** 

**Experiment Title:** 

## **HCS12 Interrupts**

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1. What is the address of the IRQ and the PTH interrupt in the HCS12 interrupt vector table? - For IRQ the address is $0xFFF2U$
For PTH the address is 0xFFCCU
2. Upon Reset, IRQ and XIRQ hardware interrupts are (edge, level) triggered Edge
3. True or False. An interrupt is assigned to each bit of PTH, instead of a single interrupt to the entire PTH.  - True
4. True or False. Upon Reset, the PTH interrupt is masked - True
<ul><li>5. In HCS12, indicate how you enable the peripheral interrupts globally.</li><li>GIE: Global Interrupt Enable, enables/disables interrupts globally.</li></ul>

 ${\bf 6. \ Which \ register \ is \ used \ to \ make \ PTH \ interrupt \ level-or \ edge-triggered?}$ 

PEIE: Enable/disable all peripheral interrupts. Use command "\_asm CLI;".

- PIEH