

**Khalifa University of Science, Technology and Research**

**Electronics Engineering Department**

**Module Name: Microprocessor Systems Laboratory**

**Module Code: ELCE332**

**Pre-Laboratory Experiment No. 6**

**HCS12 Interrupts**

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**Date pre-lab submitted:** 4-March-2015

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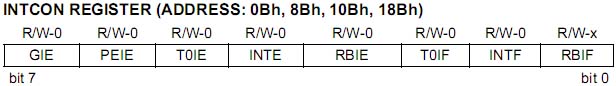
**Spring 2015**

1. **What is the address of the IRQ and the PTH interrupt in the HCS12 interrupt vector table?**

IRQ address: $FFF2:$FFF3

PTH address: $FFCC

1. **Upon Reset, IRQ and XIRQ hardware interrupts are \_\_\_\_**edge**\_\_\_\_\_ (edge, level) triggered.**
2. **True or False. An interrupt is assigned to each bit of PTH, instead of a single interrupt to the entire PTH.** True
3. **True or False. Upon Reset, the PTH interrupt is masked.** True
4. **In HCS12, indicate how you enable the peripheral interrupts globally.**



Through the GIE bit which stands for Global Interrupt Bit, if it’s a 1, unmasked interrupts are enabled. If it’s a 0, interrupts are disabled.

1. **Which register is used to make PTH interrupt level- or edge- triggered?**

In order to set PTH bits, register PIEH must be enabled. Register PPSH (PPSH=0xFF rising edge, PPSH=0x00 Falling edge) is then used to set the interrupt polarity.