**Khalifa University of Science, Technology and Research**

**Microprocessor Systems Laboratory ELCE333**

**Laboratory Experiment No. 6**

**Experiment Title: HCS12 Interrupts**

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**Group 2**

**Date pre Laboratory Performed**: 4th/March/2015

**Date pre Laboratory Submitted**: 4th/March/2015

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**Spring 2015**

**Pre-laboratory 6:**

**1. What is the address of the IRQ and the PTH interrupt in the HCS12 interrupt vector**

**table?**

IRQ has the address of $FFF2:$FFF3, PTH has the address of $FFCC, and the address of the rest is $FFFE: $FFFF.

**2. Upon Reset, IRQ and XIRQ hardware interrupts are \_\_\_\_\_\_\_\_\_ (edge, level)**

**triggered.**

The Reset Level is triggered.

The IRQ Edge is triggered.

The XIRQ Edge is triggered.

**3. True or False. An interrupt is assigned to each bit of PTH, instead of a single interrupt**

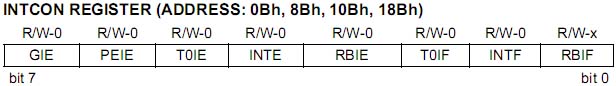
**to the entire PTH.**

Yes it is true.

**4. True or False. Upon Reset, the PTH interrupt is masked**

Yes it is true.

**5. In HCS12, indicate how you enable the peripheral interrupts globally.**



*bit 7 <GIE> : Global interrupt enable bit*

|  |  |
| --- | --- |
|  | 1 : is used to enable unmasked interrupts |
|  | 0 : is used to disable interrupts |

**6. Which register is used to make PTH interrupt level- or edge- triggered?**

To set PTH bits we have to enable the register PIEH also the Register (PPSH=0xFF rising edge, PPSH=0x00 Falling edge) to set the polarity of the interrupt.