CM2723 Programmers Reference Manual

Hardware Module: 1028191R00A Dev1
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member 1.27

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mbr1.25	preRelease-schematic 1.84 + minor changes	Henry Enns	2014-06-23
mbr1.26	preRelease-schematic 1.84 + error on page 1	Henry Enns	2014-06-23

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CAN

Controller Module		Micro				
CM.name	CM.pin	CAN.rx	CAN.tx	CAN.en	CAN.hs	CAN.trm
CAN_HI_1	J1B-9B	PD0	PD1	PH14	PE12	PB2
CAN_LO_1	J1B-8B	PD0	PD1	PH14	PE12	PB2
CAN_HI_2	J1B-14B	PB5	PB6	PH15	PE15	PB7
CAN_LO_2	J1B-20B	PB5	PB6	PH15	PE15	PB7

INTERFACE:

CAN.en
The microcontroller pin should be configured as an GPIO digital output
A high on this pin enables the CAN PHY
A low on this pin disables both Tx and Rx functions
Default state of pin if left as high impedance is logic HIGH or enabled

CAN.hs
The microcontroller pin should be configured as an GPIO digital output
Drive this line low to run at a reduced edge rate for 250Kbit CAN implementations
For higher CAN baud rates (up to 1Mbit) drive this line high to enable the maximum edge rate
Default state of pin if left as high impedance is logic LOW or disabled

CAN.trm
The microcontroller pin should be configured as an GPIO digital output
Drive this line high for normal unterminated CAN
Drive this line low to enable an internal 120 ohm differential CAN termination resistor
Default state of pin if left as high impedance is logic LOW or enabled

NOTES:
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance

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RS232

Controller Module		Micro		
CM.name	CM.pin	232.rx	232.tx	232.en
RS232RX	J1A-25A	PG9	-	PI11
RS232TX	J1A-32A	-	PG14	PI11

INTERFACE:

232.rx RS232 receive output of the RS232 transceiver

232.tx RS232 transmit input of the RS232 transceiver

232.en The microcontroller pin should be configured as an GPIO digital output
A high on this pin enables the RS232 PHY
A low on this pin powers down the PHY
Default state of pin if left as high impedance is logic LOW or disabled

NOTES: The RS232 option uses the same external controller pins as INPUT1 and INPUT2
These options are mutually exclusive
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance

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AIN (Analog IN)

Controller Module			Micro			PCBA properties								
						UP			DOWN			GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.dig_en	IN.v	Rvs	Rpu	Rwet	Rpd1	Rpd2	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT1	AIN01_DIN01	J1A-25A	PH2	PB12	PA0	DNP	2.74 K	0.47 K	51.10 K	DNP	DNP	97 K	3.21 Volt/Volt	77 Hz
INPUT2	AIN02_DIN02	J1A-32A	PH3	PB13	PA1	6.81 K	2.74 K	0.47 K	DNP	DNP	DNP	∞ K	1.00 Volt/Volt	24 Hz
INPUT3	AIN03_DIN03	J1A-33A	PH4	PB15	PA2	DNP	2.74 K	0.47 K	51.10 K	DNP	DNP	167 K	1.67 Volt/Volt	40 Hz
INPUT4	AIN04_DIN04	J1B-1B	PH5	PB15	PA3	DNP	2.74 K	0.47 K	51.10 K	DNP	DNP	97 K	3.21 Volt/Volt	77 Hz

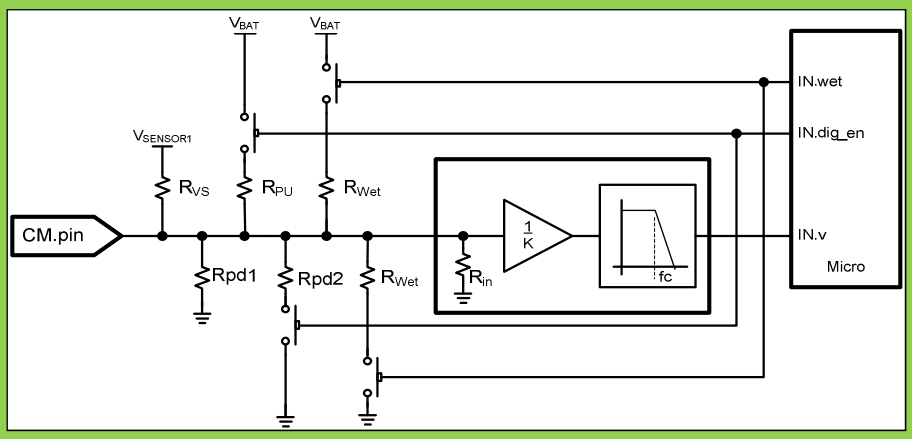
INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.dig_en The microcontroller pin should be configured as an GPIO digital output
Drive this pin high to enable a weak resistor with value and "direction" shown under PCBA properties

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: The RS232 option uses the same external controller pins as INPUT1 and INPUT2
These options are mutually exclusive
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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DIN (Digital IN)

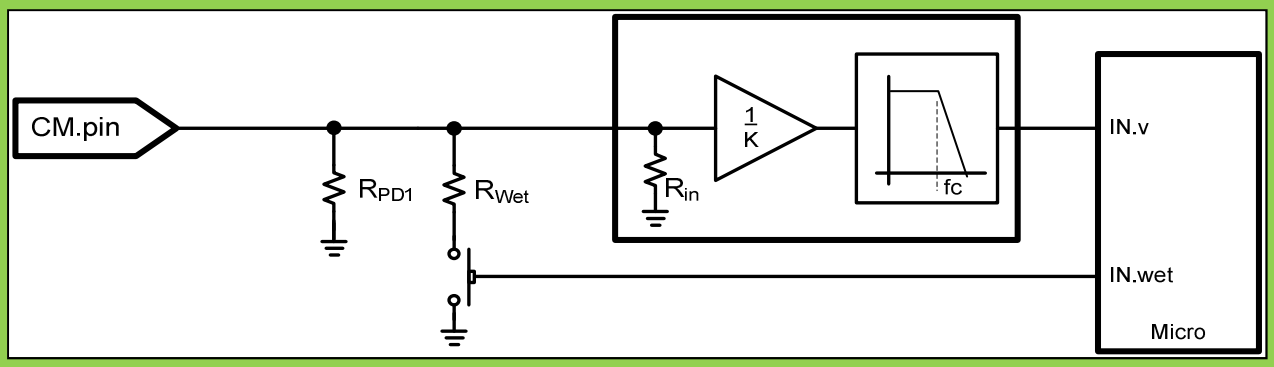
Controller Module			Micro		PCBA properties				
					DOWN		GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	Rpd1	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT5	DIN05	J1A-21A	PI0	PD2	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT6	DIN06	J1A-30A	PI0	PD3	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT7	DIN07	J1A-14A	PI0	PD4	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT8	DIN08	J1A-31A	PI0	PD5	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT9	DIN09	J1A-28A	PI1	PD6	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT10	DIN10	J1A-22A	PI1	PD7	2.74 K	0.47 K	212 K	3.42 Volt/Volt	36 Hz
INPUT18	DIN18	J1A-24A	PI10	PE1	2.74 K	0.47 K	204 K	1.68 Volt/Volt	32 Hz

INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.v The microcontroller pin should be configured as an GPIO digital input
The external CM.pin voltage is determined by mutiplying the voltage at IN.v * K
Therefore CM.Vih would be Micro.Vih * K
and CM.Vil would be Micro.Vil * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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DIN (Digital IN)

Controller Module			Micro			PCBA properties								
CM.name	SLE.name	CM.pin	IN.wet	IN.v	IN.f	SW_{Cfg}	UP	DOWN		GAIN BLOCK				
							Rvs	Rpd1	Rwet	Rin1	K1	Fc1	Rin2	K2	Fc2
INPUT11	DIN11	J1A-13A	PI1	PF5.X0	PC7	Non-Inv	DNP	2.74 K	0.47 K	212 K	3.42 V/V	36 Hz	∞ K	N/A	N/A
INPUT12	DIN12	J1A-29A	PI1	PF5.X1	PD12	Non-Inv	DNP	2.74 K	0.47 K	212 K	3.42 V/V	36 Hz	∞ K	N/A	N/A

INTERFACE:

IN.wet The microcontroller pin should be configured as a PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.f Input is configured as either a frequency input or a TTL compatible logic input
Input is either inverted by TTL compatible gate or non-inverted input signal
Switch SW_{Cfg} is determined by a stuffing option at time of manufacture. It is not a physical switch.

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

PF5.Xx This indicates a 74x4851 analog mux connected to the micro analog input PF5.
The .Xx suffix indicates the mux input pin this signal is connected to.
Micro port PG12 drives mux address line A.
Micro port PG13 drives mux address line B.
Micro port PG15 drives mux address line C.

NOTES: INPUT11, INPUT12 can only be read from input PF5 after driving the mux select lines
tbd useconds must be allowed after driving the mux select lines prior to reading the voltage from the mux
All values in this document are typical unless otherwise stated
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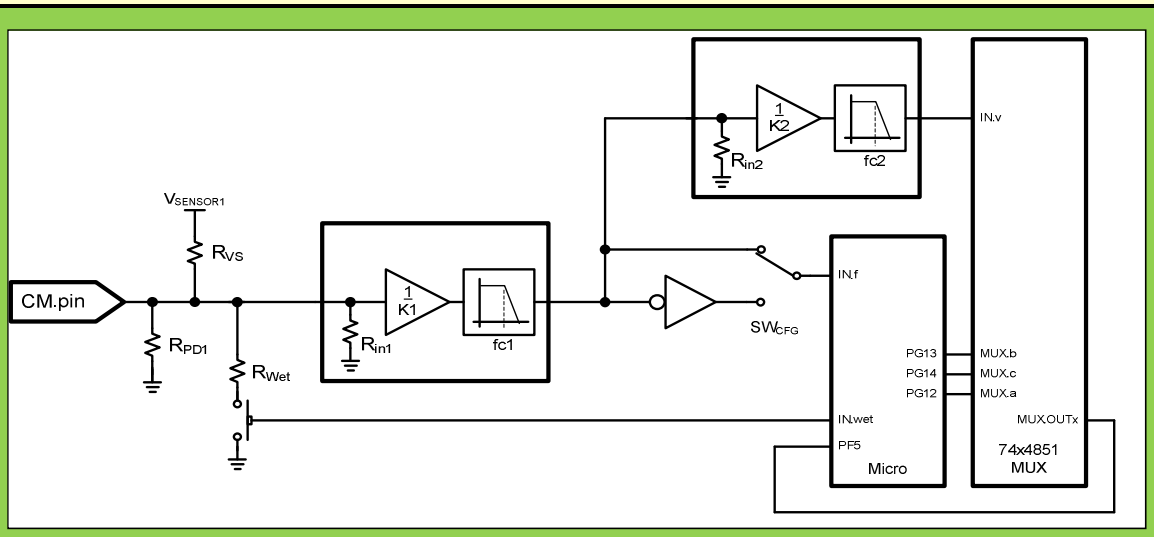

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AIN (Analog IN)

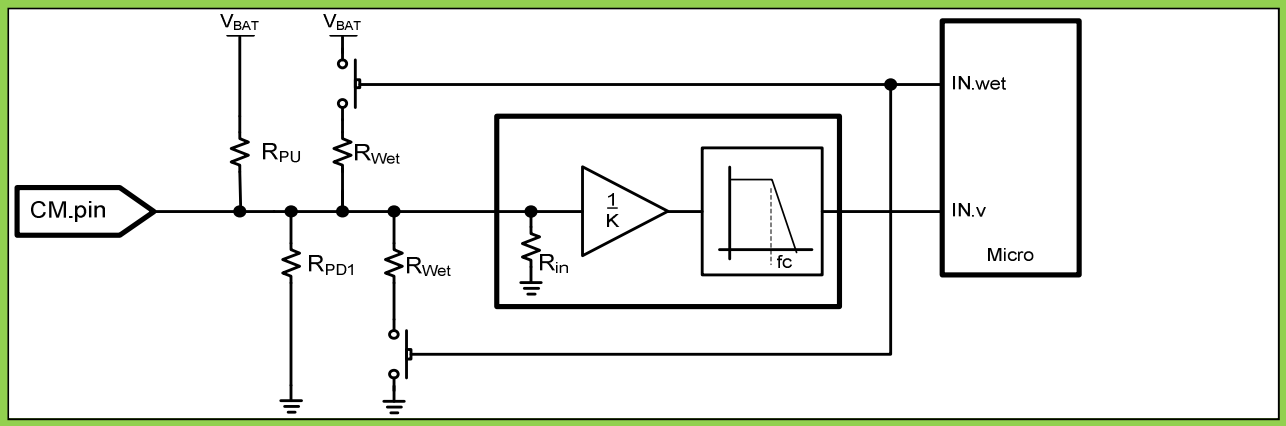
Controller Module			Micro		PCBA properties						
					UP		DOWN		GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	Rpu	Rwet	Rpd1	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT13	DIN13	J1A-16A	PI2	PD8	2.74 K	0.47 K	DNP	DNP	212 K	3.42 Volt/Volt	36 Hz
INPUT14	DIN14	J1A-34A	PI2	PD9	2.74 K	0.47 K	DNP	DNP	212 K	3.42 Volt/Volt	36 Hz
INPUT15	DIN15	J1A-23A	PI2	PD10	2.74 K	0.47 K	DNP	DNP	212 K	3.42 Volt/Volt	36 Hz

INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.v The microcontroller pin should be configured as an GPIO digital input
The external CM.pin voltage is determined by mutiplying the voltage at IN.v * K
Therefore CM.Vih would be Micro.Vih * K
and CM.Vil would be Micro.Vil * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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AIN (Analog IN)

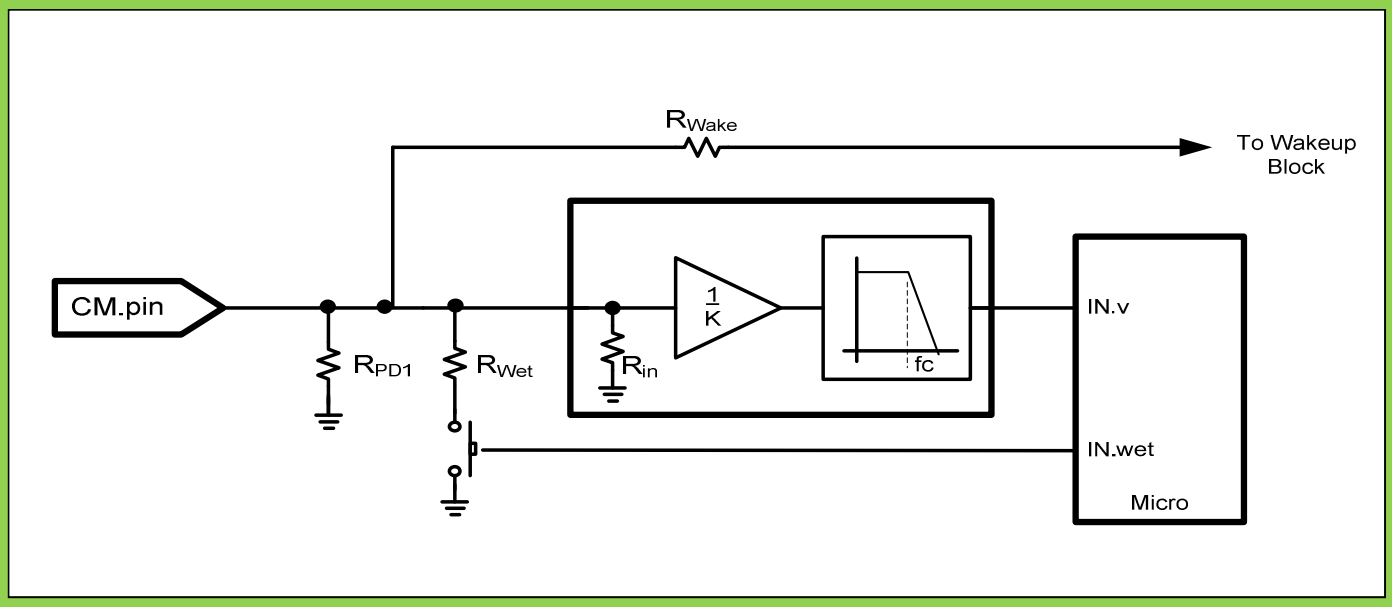
Controller Module			Micro		PCBA properties					
					DOWN			GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	Rpd1	Rwake	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT16	DIN16	J1B-21B	PI3	PD11	2.74 K	2.49 K	0.47 K	204 K	1.68 Volt/Volt	32 Hz
INPUT17	DIN17	J1B-22B	PI3	PE0	2.74 K	2.49 K	0.47 K	204 K	1.68 Volt/Volt	32 Hz

INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.v The microcontroller pin should be configured as an GPIO digital input
The external CM.pin voltage is determined by mutiplying the voltage at IN.v * K
Therefore CM.Vih would be Micro.Vih * K
and CM.Vil would be Micro.Vil * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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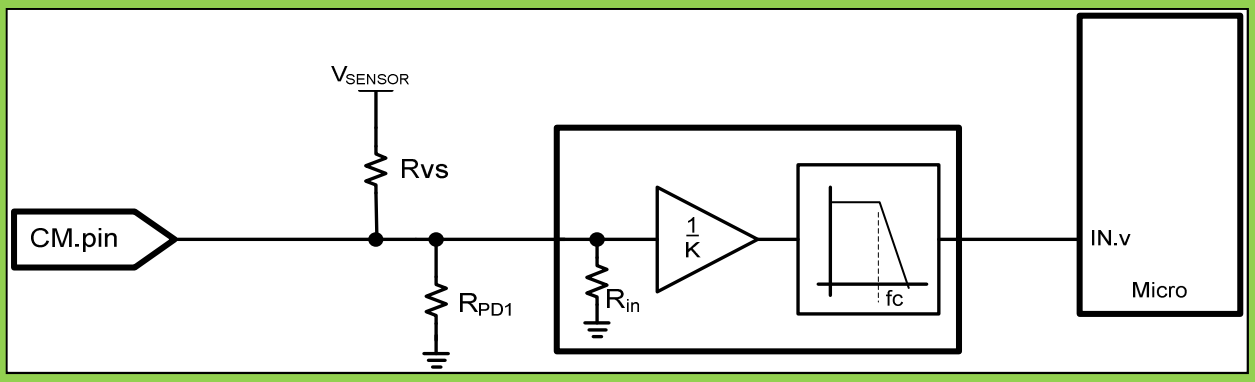
AIN (Analog IN)

Controller Module			Micro	PCBA properties				
				UP	DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.v	Rvs	Rpd1	Rin	K = CM.pin / IN.v	Fc
INPUT19	AIN05	J1B-18B	PC0	6.81 K	DNP	∞ K	1.00 Volt/Volt	24 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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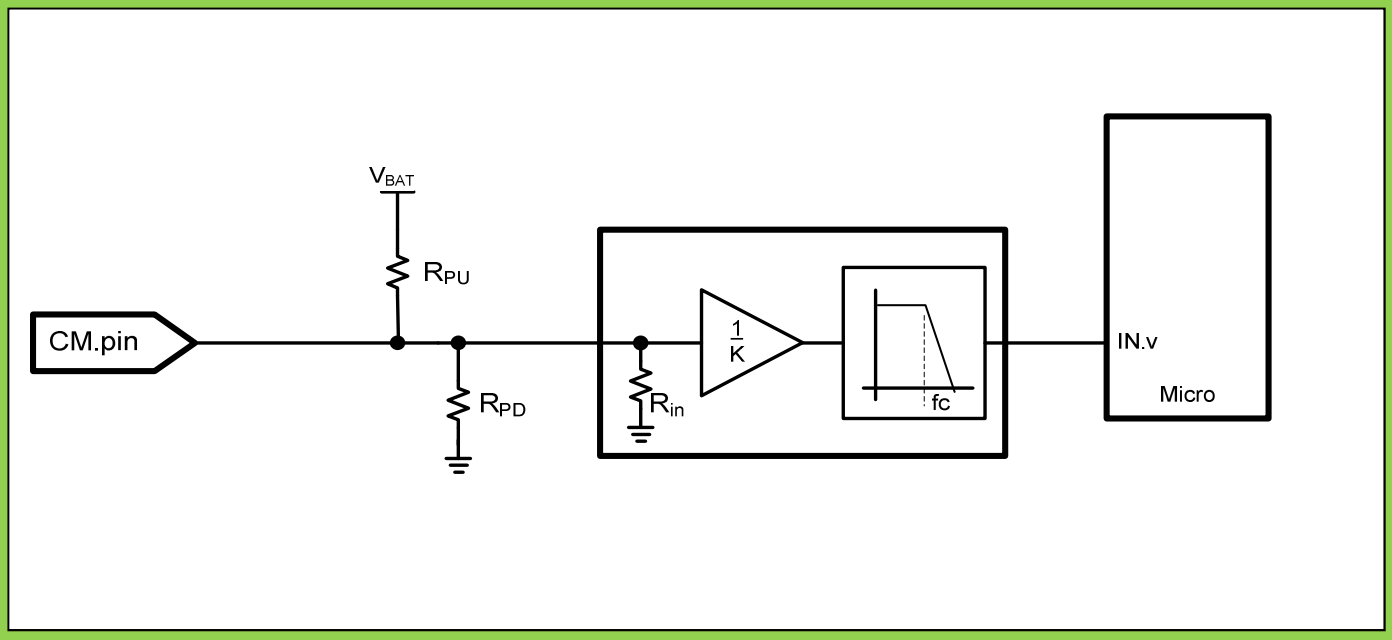
AIN (Analog IN)

Controller Module			Micro	PCBA properties				
				UP	DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.v	Rpu	Rpd1	Rin	K = CM.pin / IN.v	Fc
INPUT20	AIN06	J1B-12B	PC1	2.49 K	DNP	∞ K	1.00 Volt/Volt	24 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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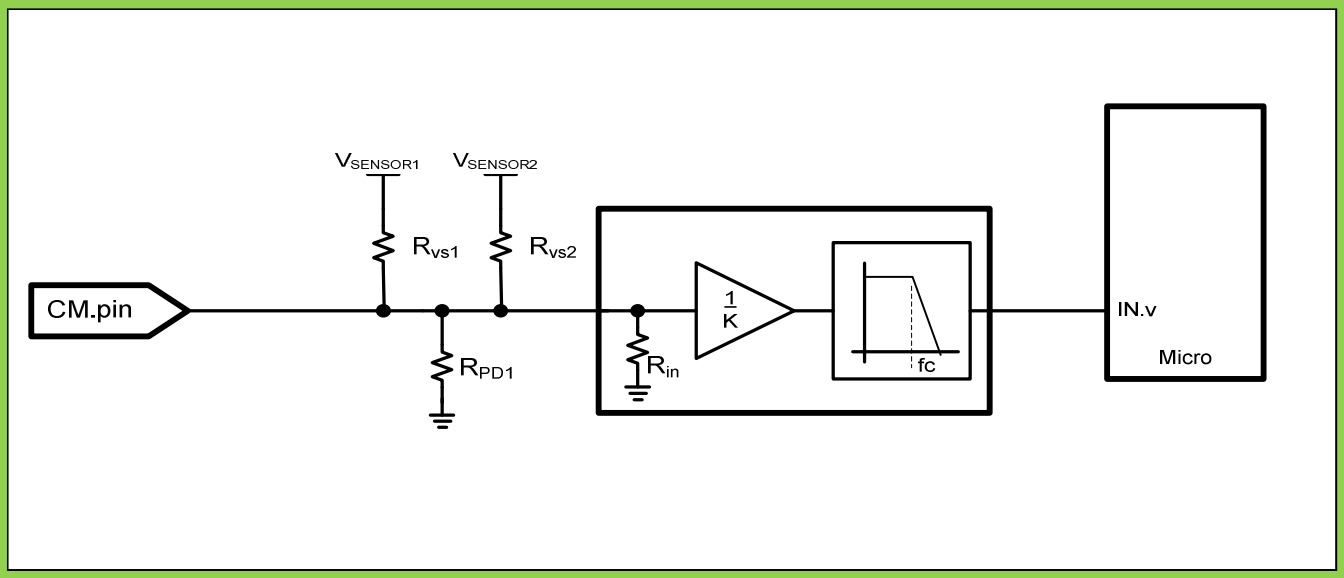
AIN (Analog IN)

Controller Module			Micro	PCBA properties						
				UP		DOWN	GAIN BLOCK			
CM.name	SLE.name	CM.pin	IN.v	Rvs1	Rvs2	Rpd1	Rin	K = CM.pin / IN.v		Fc
INPUT21	AIN07	J1B-11B	PC2	DNP	2.49 K	DNP	97 K	3.21	Volt/Volt	77 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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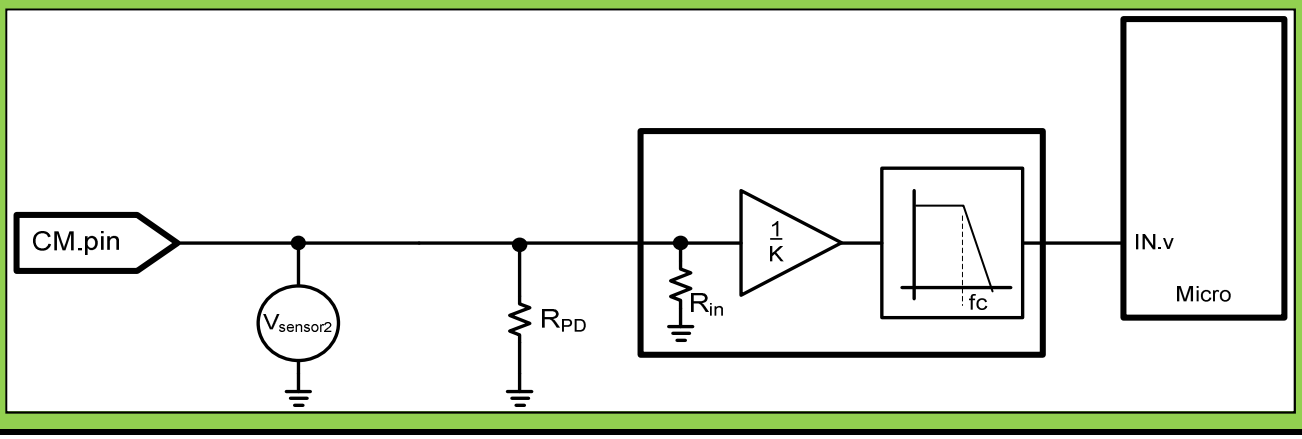
AIN (Analog IN)

Controller Module			Micro	PCBA properties			
				DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.v	Rpd1	Rin	K = CM.pin / IN.v	Fc
INPUT22 VSENSOR2	AIN08 VSENSOR2	J1B-24B	PF4	51.10 K	97 K	3.21 Volt/Volt	77 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: The VSENSOR2 option uses the same external controller pin as INPUT22
When the VSENSOR2 option is installed this will return the VSENSOR2 voltage
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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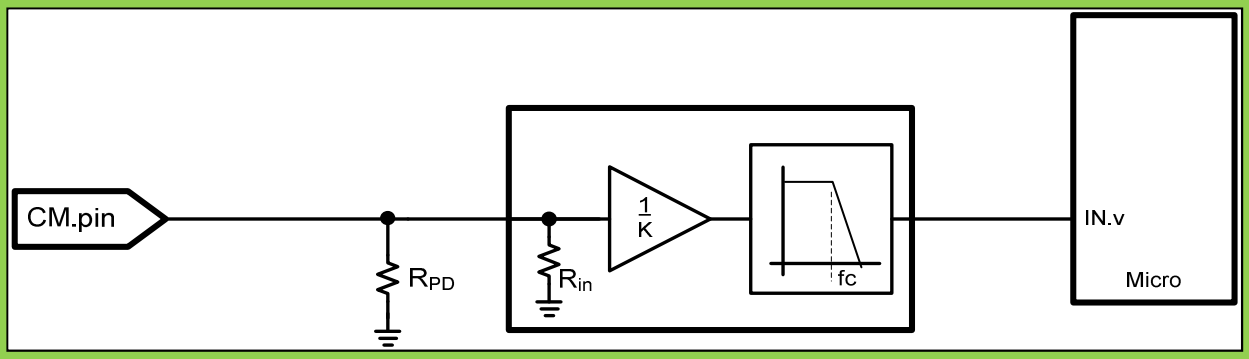
AIN (Analog IN)

Controller Module			Micro	PCBA properties			
				DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.v	`	Rin	K = CM.pin / IN.v	Fc
INPUT23	AIN09	J1B-10B	PC3	51.10 K	167 K	1.67 Volt/Volt	40 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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DIN (Digital IN)

Controller Module			Micro		PCBA properties				
					DOWN		GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	Rpd1	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT24	AIN10	J1A-20A	PI9	PF6	2.74 K	0.47 K	300 K	9.97 Volt/Volt	59 Hz

INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
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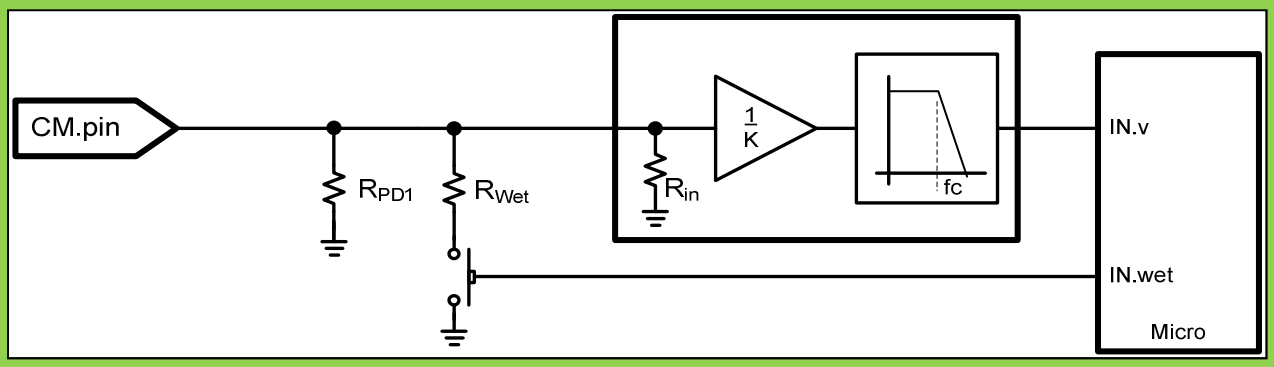

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AIN (Analog IN)

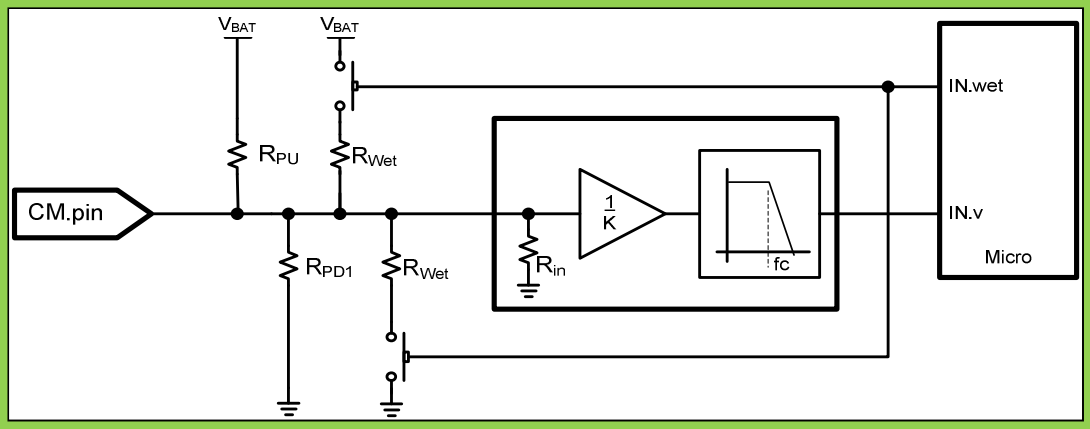
Controller Module			Micro		PCBA properties						
					UP		DOWN		GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	Rpu	Rwet	Rpd2	Rwet	Rin	K = CM.pin / IN.v	Fc
INPUT25	AIN12	J1A-11A	PI4	PF7	DNP	DNP	2.74 K	0.47 K	300 K	9.97 Volt/Volt	59 Hz
INPUT26	AIN13	J1A-12A	PI8	PF8	2.74 K	0.47 K	DNP	DNP	300 K	9.97 Volt/Volt	59 Hz

INTERFACE:

IN.wet The microcontroller pin should be configured as an PWM digital output
Drive this pin high to enable a wetting resistor as indicated under PCBA properties
This should be driven with a PWM limited to a maximum 10 % (TBC) duty cycle

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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DIN (Digital IN)

Controller Module			Micro			PCBA properties				
						UP	DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.wet	IN.v	IN.f	Rvs	Rpd1	Rin	K = CM.pin / IN.v	Fc
INPUT27	FIN1	J1A-15A	N/A	PF5.X2	PD13	10.00 K	DNP	∞ K	2.0 Volt/Volt	0 Hz

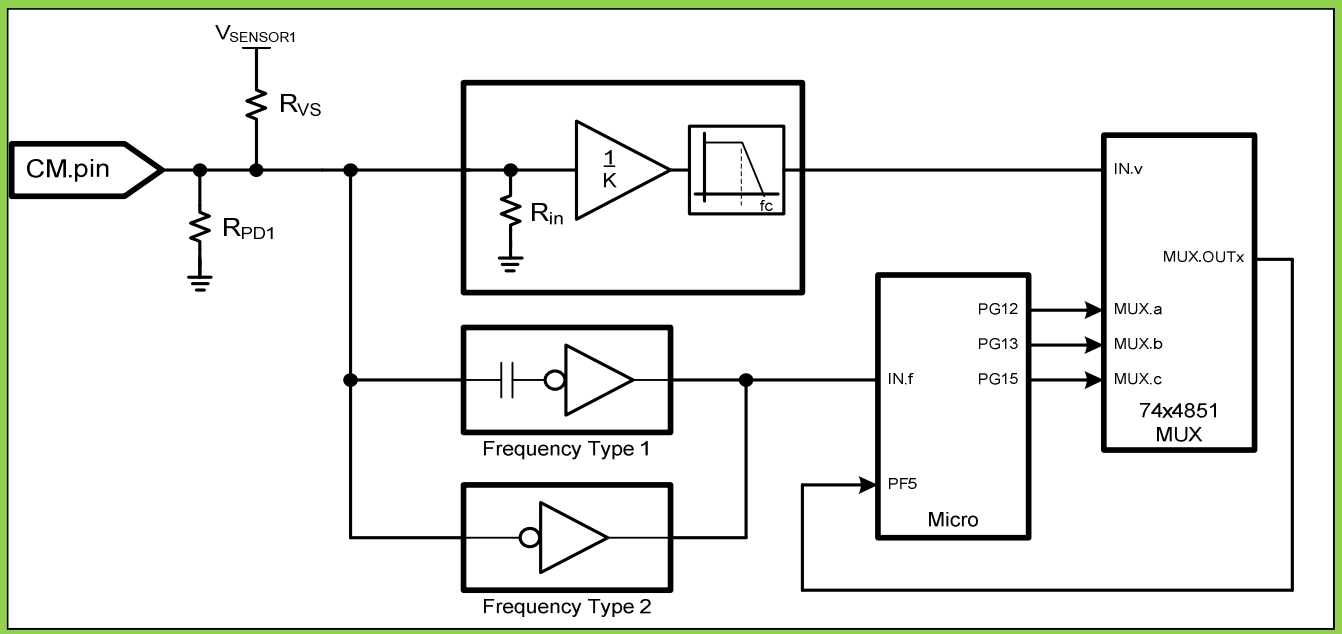
INTERFACE:

IN.f This can be populated as either a DC or AC coupled signal from the input pin, conditioned to the micro levels. Measure the frequency on this pin to determine the input frequency at the controller pin.

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

PF5.Xx This indicates a 74x4851 analog mux connected to the micro analog input PF5.
The .Xx suffix indicates the mux input pin this signal is connected to.
Micro port PG12 drives mux address line A.
Micro port PG13 drives mux address line B.
Micro port PG15 drives mux address line C.

NOTES: INPUT27 can only be read from input PF5 after driving the mux select lines
tbd useconds must be allowed after driving the mux select lines prior to reading the voltage from the mux
The OUTPUT23 option uses the same external controller pin as INPUT28
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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DIN (Digital IN)

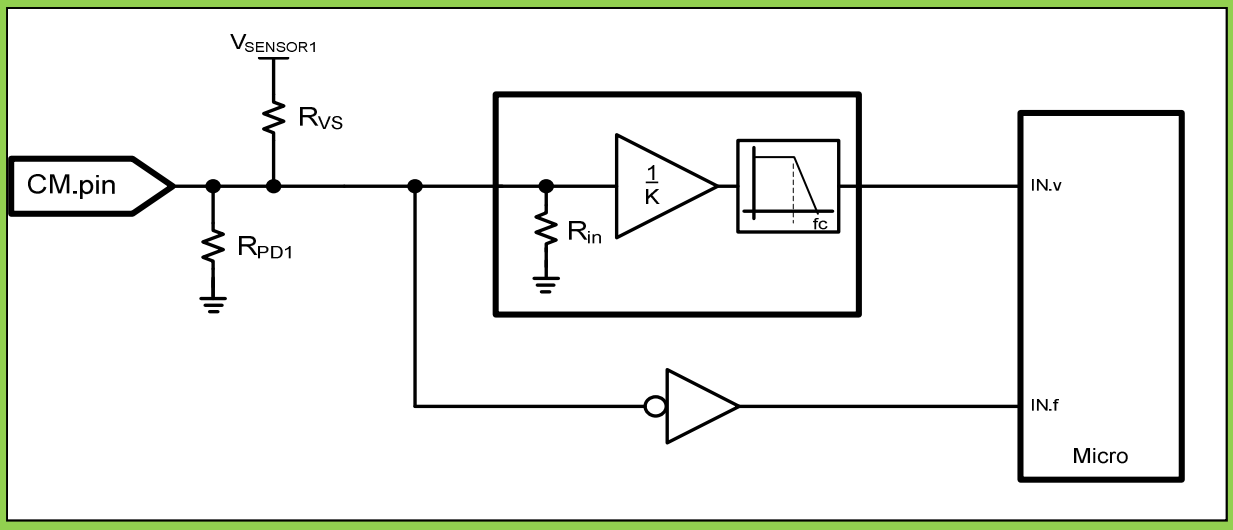
Controller Module					PCBA properties				
					UP	DOWN	GAIN BLOCK		
CM.name	SLE.name	CM.pin	IN.v	IN.f	Rvs	Rpd1	Rin	K = CM.pin / IN.v	Fc
OUTPUT23 INPUT28	AIN11 LC_LSD1	J1A-19A	PF10	PC6	DNP	DNP	∞ K	1.0 Volt/Volt	59 Hz

INTERFACE:

IN.f This is a DC coupled inverted signal with 3V3 logic levels.
Measure the frequency on this pin to determine the input frequency at the controller pin.

IN.v not supported on this variant

NOTES: The OUTPUT23 option uses the same external controller pin as INPUT28
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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HSO (High Side Output)

Controller Module			Micro		PCBA properties						
CM.name	SLE.name	CM.pin	HSO.out	HSO.fbk	K = CM.pin / HSO.fbk	Ropen@ 13.8 V	Rpu	Rpd	Max Out Current	Output Type	Trc
OUTPUT1	HC_HSD1	J1B-4B	PE9	PC5.X0	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT2	HC_HSD2	J1B-5B	PB10	PC5.X1	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT3	HC_HSD3	J1B-6B	PH10	PC5.X2	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT4	HC_HSD4	J1B-7B	PI5	PC5.X3	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT5	HC_HSD5	J1B-13B	PE11	PC5.X4	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT6	HC_HSD6	J1B-19B	PB9	PC5.X5	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT7	HC_HSD7	J1B-26B	PH6	PC5.X6	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms
OUTPUT8	HC_HSD8	J1B-25B	PB8	PC5.X7	7.21	10.90 KΩ	20.0 K	20.2 K	3 Amp	1	0.28 ms

INTERFACE:

HSO.out — Drive this pin high to turn on the high side driver, causing it to pull the output to the battery voltage

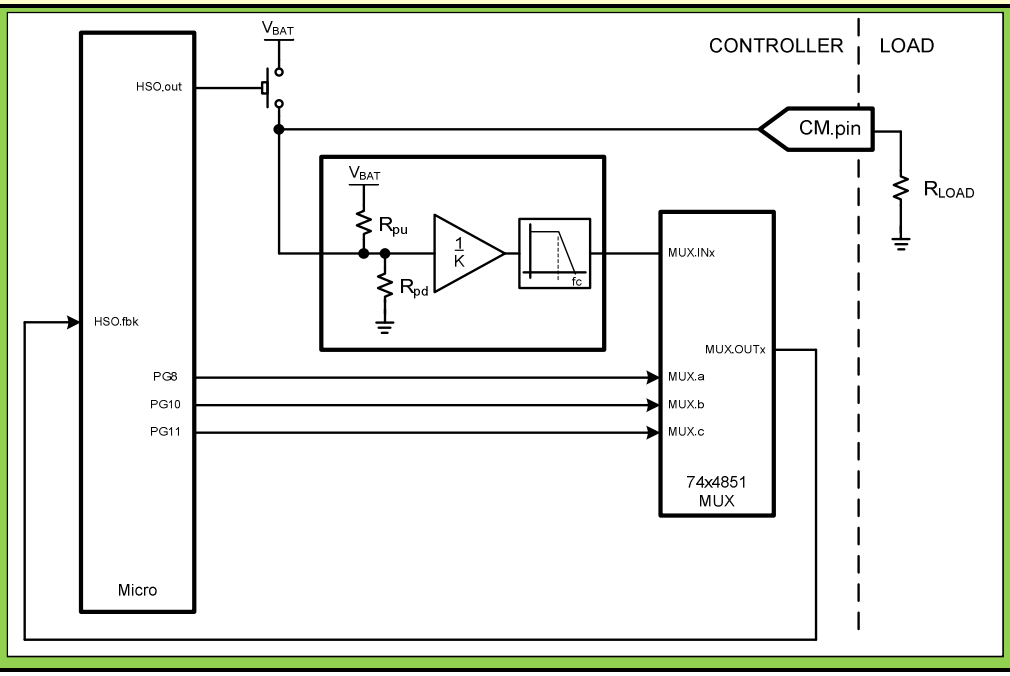
HSO.fbk — The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying HSO.fbk * K

PC5.Xx — This indicates a 74x4851 analog mux connected to the micro analog input PC5.
The .Xx suffix indicates the mux input pin this signal is connected to.
Micro port PG8 drives mux address line A.
Micro port PG10 drives mux address line B.
Micro port PG11 drives mux address line C.

SOFTWARE REQUIREMENT:

When the driver is turned on, check for STG (Short To Ground) periodically with a period not to exceed TBD ms.
If a STG (Short To Ground) is detected, turn off the output and log a STG (Short To Ground) error.

NOTES:
- OUTPUT1 thru OUTPUT8 can only be read from input PC5 after driving the mux select lines.
- tbd useconds must be allowed after driving the mux select lines prior to reading the voltage from the mux
- A delay must be allowed after switching the output state based on Trc
- The Ropen threshold is based on the Vbat shown and a 0.5V software threshold at the micro pin
- All values in this document are typical unless otherwise stated
- Tolerances have been chosen to meet or exceed the original SLE performance



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HSO (High Side Output)

Controller Module			Micro		PCBA properties						
CM.name	SLE.name	CM.pin	HSO.out	HSO.fbk	K = CM.pin / HSO.fbk	Ropen@ 13.8 V	Rpu	Rpd	Max Out Current	Output Type	Trc
OUTPUT9	LC_HSD1	J1A-4A	PB11	PG0	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT10	LC_HSD2	J1A-3A	PC8	PG1	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT11	LC_HSD3	J1A-5A	PE13	PG2	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT12	LC_HSD4	J1A-7A	PH9	PG3	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT13	LC_HSD5	J1A-6A	PC9	PG4	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT14	LC_HSD6	J1A-8A	PE14	PG5	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT15	LC_HSD7	J1A-17A	PH11	PG6	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms
OUTPUT16	LC_HSD8	J1A-9A	PH12	PG7	3.21	2.3 KΩ	10.0 K	119.9 K	0.35 Amp	2	2.6 ms

INTERFACE:

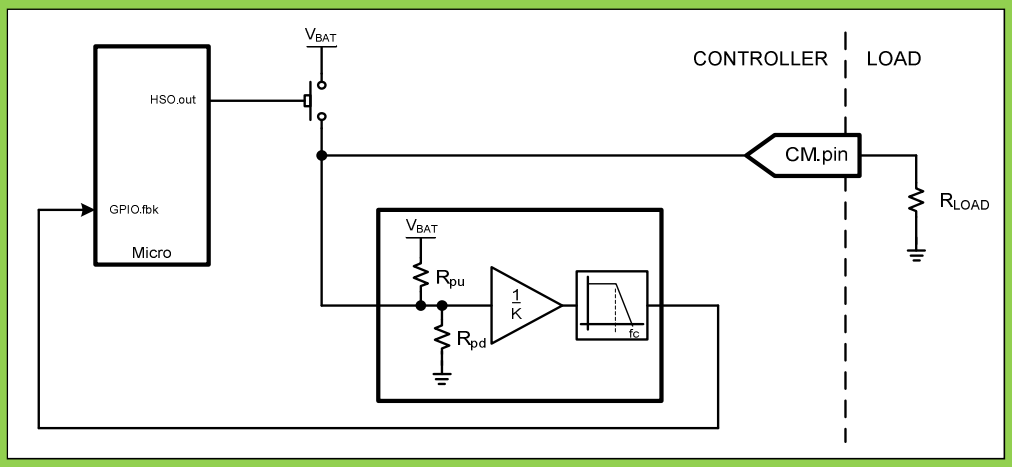
HSO.out Drive this pin high to turn on the high side driver causing it to pull the output to the battery voltage

HSO.fbk The microcontroller pin should be configured as an GPIO digital input
The microcontroller pin HSO.fbk is the voltage at pin CM.pin / K
A load of less resistance than Ropen will NOT generate a high on this pin.
A load of more resistance than Ropen may generate a high on this pin.

SOFTWARE REQUIREMENT:

When the driver is turned on, check for STG (Short To Ground) periodically with a period not to exceed TBD ms.
If a STG (Short To Ground) is detected, turn off the output and log a STG (Short To Ground) error.

NOTES: Intent of feedback is to generate a logic HIGH when output is ON into valid load and a logic LOW when output is OFF into valid load
The Ropen threshold is based on the Vbat shown and a 0.8V Vil threshold at the micro pin
A delay must be allowed after switching the output state based on Trc
All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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LSO (Low Side Output)

Controller Module			Micro		PCBA properties	
CM.name	SLE.name	CM.pin	LSO.out	LSO.ifbk	gm = iCM.pin / LSO.ifbk	Fc
OUTPUT17	HC_LSD1	J1A-2A	PI6	PA4	1.91 Amp/Volt	9.6 Hz
OUTPUT18	HC_LSD2	J1A-1A	PI7	PA5	1.00 Amp/Volt	9.6 Hz
OUTPUT19	HC_LSD3	J1A-10A	PF11	PA6	1.91 Amp/Volt	9.6 Hz
OUTPUT20	HC_LSD4	J1A-18A	PF12	PA7	1.00 Amp/Volt	9.6 Hz
OUTPUT21	HC_LSD5	J1A-26A	PF13	PB0	1.00 Amp/Volt	9.6 Hz
OUTPUT22	HC_LSD6	J1A-27A	PF14	PB1	1.00 Amp/Volt	9.6 Hz

INTERFACE:

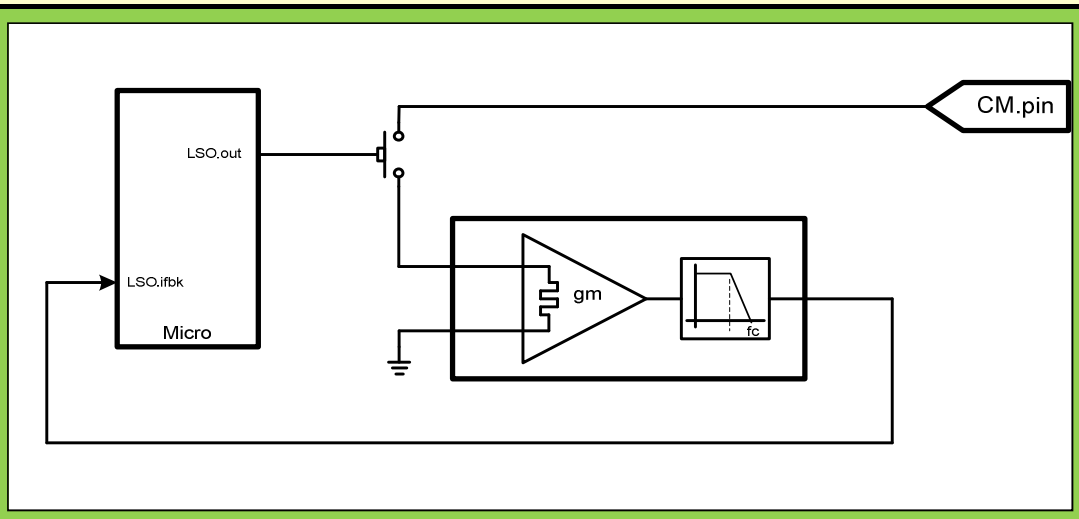
LSO.out Drive this pin high to turn on the low side driver causing it to pull the output to ground.

LSO.ifbk The microcontroller pin should be configured as an ADC input
The external CM.pin current is determined by mutiplying LSO.ifbk * gm

SOFTWARE REQUIREMENT:

Check if the input pin LSO.ifbk has gone above TBD Amps after a TBD delay.
Check if the input pin LSO.ifbk has gone above TBD Amps periodically with a period not to exceed TBD ms.
If the current exceeds the limit, turn off the output and log a STB (Short To Battery) error.

NOTES: All values in this document are typical unless otherwise stated.
Tolerances have been chosen to meet or exceed the original SLE performance.



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LSI (Low Side Current output)

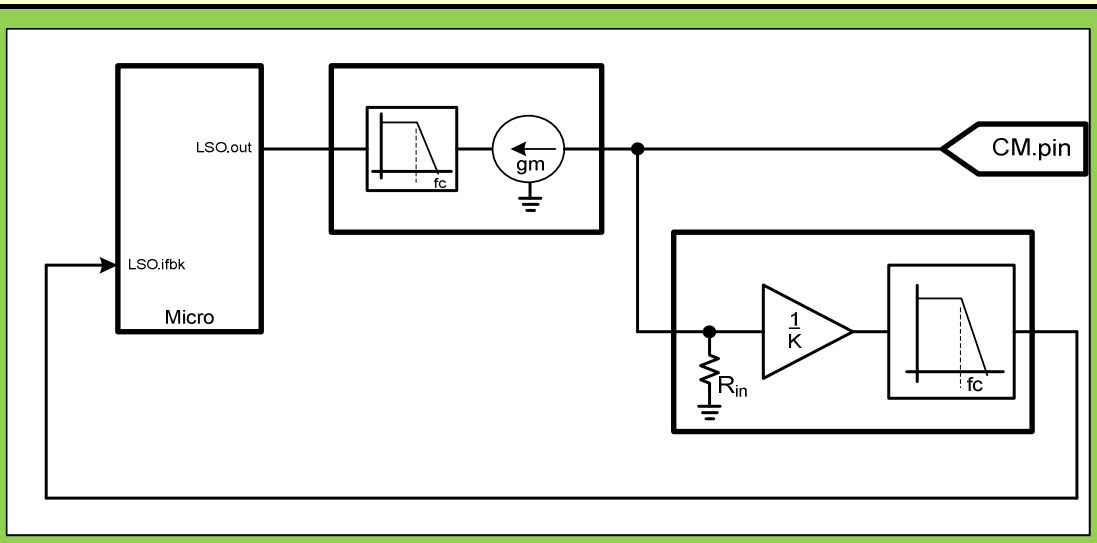
Controller Module			Micro		PCBA properties		
CM.name	SLE.name	CM.pin	LSI.out	LSI.fbk	IoutMax	K = CM.pin / LSI.fbk	fc
OUTPUT23	AIN11 LC_LSD1	J1A-19A	PC6	PF10	50 mA	9.97 Volt/Volt	59 Hz

INTERFACE:

LSI.out PWM this pin to control the output current. The current output will be PWMduty * IoutMax

LSI.fbk The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying LSI.fbk * K

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance



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Misc Internal Analogs

Controller Module				PCBA properties	
				GAIN BLOCK	
CM.name	SLE.name	CM.pin	IN.v	K = CM.pin / IN.v	fc
Vbattery	+12V VBATT	J1B-2B	PF9	9.97 Volt/Volt	59 Hz
Switched Vbattery	Switched Vbattery	internal	PF3	9.97 Volt/Volt	59 Hz
Vsensor1	Vsensor1	J1B-23B	PC4	3.21 Volt/Volt	77 Hz

INTERFACE:

IN.v The microcontroller pin should be configured as an ADC input
The external CM.pin voltage is determined by mutiplying IN.v * K

NOTES: All values in this document are typical unless otherwise stated.
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Misc

Controller Module			Micro		PCBA properties
CM.name	SLE.name	CM.pin	port	function	
				PDR_ON	3.3 Volts nominal
				NRST	0.01uF capacitor
				BOOT0	GND
			PH0	OSC_IN	10.000MHz crystal
			PH1	OSC_OUT	
			PC14	OSC32_IN	32.768KHz crystal
			PC15	OSC32_OUT	
				VREF+	3.0 Volts nominal
			PA8	POWER_HOLD	
			PH8	I2C3_SDA	24LC02 EEPROM
			PH7	I2C3_SCL	
			PF0	I2C2_SDA	24LC64 MMA8451
			PF1	I2C2_SCL	
			PH13	INT1	MMA8451
			PF15	INT2	MMA8451
			PF2	WriteProtect	24LC64

INTERFACE:

PA8 POWER_HOLD should be driven high during boot to turn ON the internal power supply.
POWER_HOLD should be driven low to turn OFF the internal power supply.
This allows the code to perform any required housekeeping operations prior to a SOFT shutdown.

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance

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Debug

Controller Module			Micro	
CM.name	SLE.name	CM.pin	port	function
USB	–	int J2	PA11	USB_FS_DM
USB	–	int J2	PA12	USB_FS_DP
JTAG	–	int J3	PA13	TMS
JTAG	–	int J3	PA14	TCK
JTAG	–	int J3	PA15	TDI
JTAG	–	int J3	PB3	TDO
JTAG	–	int J3	PB4	JRST
JTAG	–	int J3	PE2	TRACECLK
JTAG	–	int J3	PE3	TRACED0
JTAG	–	int J3	PE4	TRACED1
JTAG	–	int J3	PE5	TRACED2
JTAG	–	int J3	PE6	TRACED3

NOTES: All values in this document are typical unless otherwise stated
Tolerances have been chosen to meet or exceed the original SLE performance