به نام خدا

تمرین دوم

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استاد : دکتر صاحب الزمانی

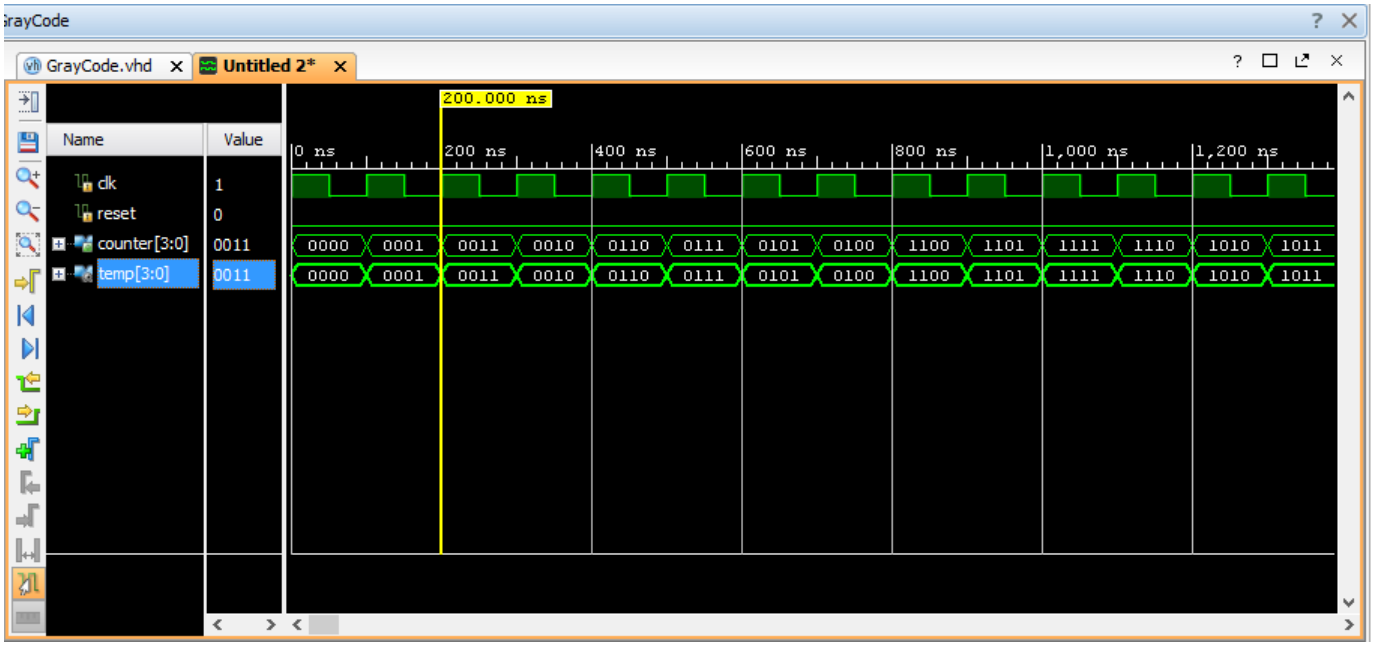
سوال ۸ :

کد این سوال به صورت زیر است :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity GrayCode is  Port (
clk : in std_logic ;
reset : in std_logic ;
counter : out std_logic_vector(3 downto 0)
);
end GrayCode;
architecture RTL of GrayCode is
signal temp : std_logic_vector(3 downto 0);
begin
process(clk)
begin
if( clk'event and clk = '1') then
if( reset = '1' )then
temp <= "0000";
else
case temp is
when "0000" => temp <= "0001";
when "0001" => temp <= "0011";
when "0011" => temp <= "0010";
when "0010" => temp <= "0110";
when "0110" => temp <= "0111";
when "0111" => temp <= "0101";
when "0101" => temp <= "0100";
when "0100" => temp <= "1100";
when "1100" => temp <= "1101";
when "1101" => temp <= "1111";
when "1111" => temp <= "1110";
when "1110" => temp <= "1010";
when "1010" => temp <= "1011";
when "1011" => temp <= "1001";
when "1001" => temp <= "1000";
when "1000" => temp <= "0000";
when others => temp <= "0000";
```

```
end case;
end if;
end if;
end process;
counter <= temp;
end RTL;
```

شکل موج آن به صورت زیر میباشد :



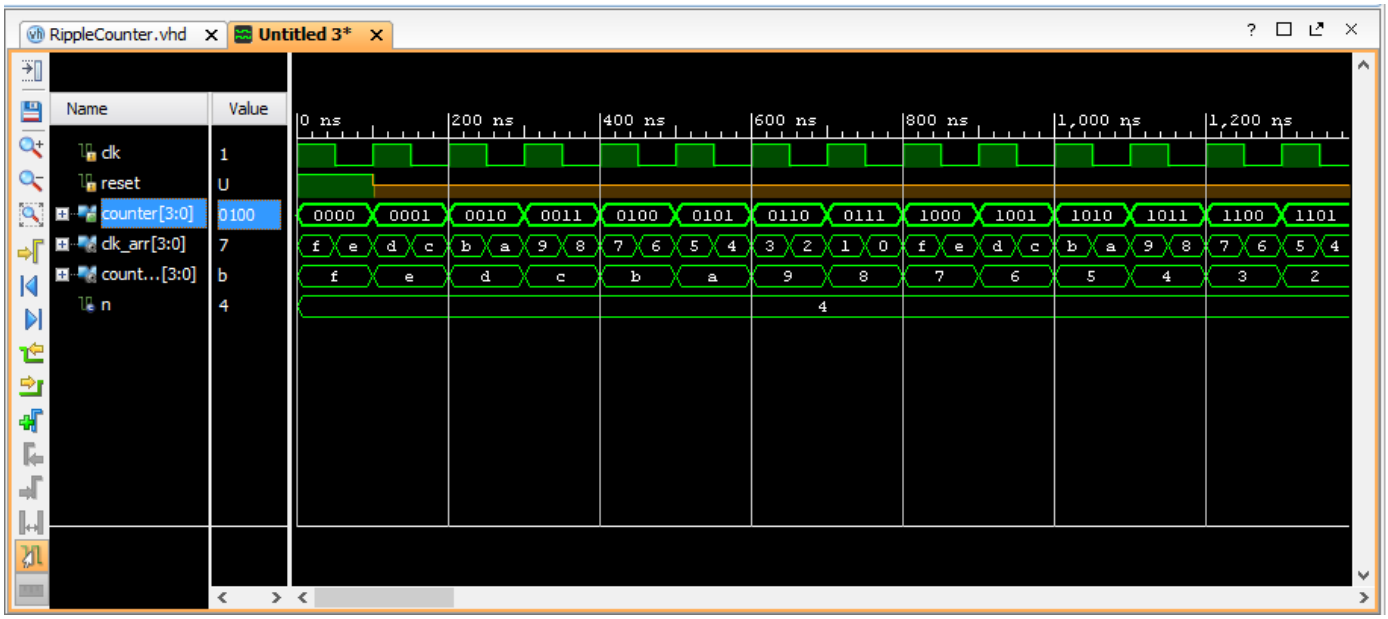
سوال ۹ :

کد آن به صورت زیر است :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_unsigned.ALL;
entity RippleCounter is
  generic (
    n : natural := 4
  );
```

```
  port (
    clk   : in std_logic;
    reset : in std_logic;

    counter  : out std_logic_vector(n-1 downto 0)
  );
end RippleCounter;
architecture RTL of RippleCounter is
  signal clk_arr, counter_arr   : std_logic_vector(n-1 downto 0);
begin
  clk_arr(0)            <= clk;
  clk_arr(n-1 downto 1) <= counter_arr(n-2 downto 0);
  gen_cnt: for i in 0 to n-1 generate
    dff: process(reset , clk_arr(i))
    begin
      if (reset = '1') then
        counter_arr(i) <= '1';
      elsif (clk_arr(i)'event and clk_arr(i) = '1') then
        counter_arr(i) <= not counter_arr(i);
      end if;
    end process dff;
  end generate;
```

شکل موج آن به صورت زیر می باشد :



سوال ۱۰ :

با توجه به اینکه در process آخرین ASSIGNMENT در PROCESS اجرا میشود مقدار X برابر ۱ و مقدار Y برابر ۰ خواهد ماند . همچنین W چون هیچ گاه تغییر نمیکند برابر همان مقدار اولیه یعنی u میماند. Zهم با توجه به تنها انتسابش برابر ۱ خواهد بود.

سوال ۱۱ :

```
Configuration conf_name  of my_module is
 for arch_name
      For MODULE1:M1
            Use entity work.multiplier(sequential);
      End for;
      For others:M1
            Use entity work.multiplier(array)
      End for;
End for;
End conf_name;
```

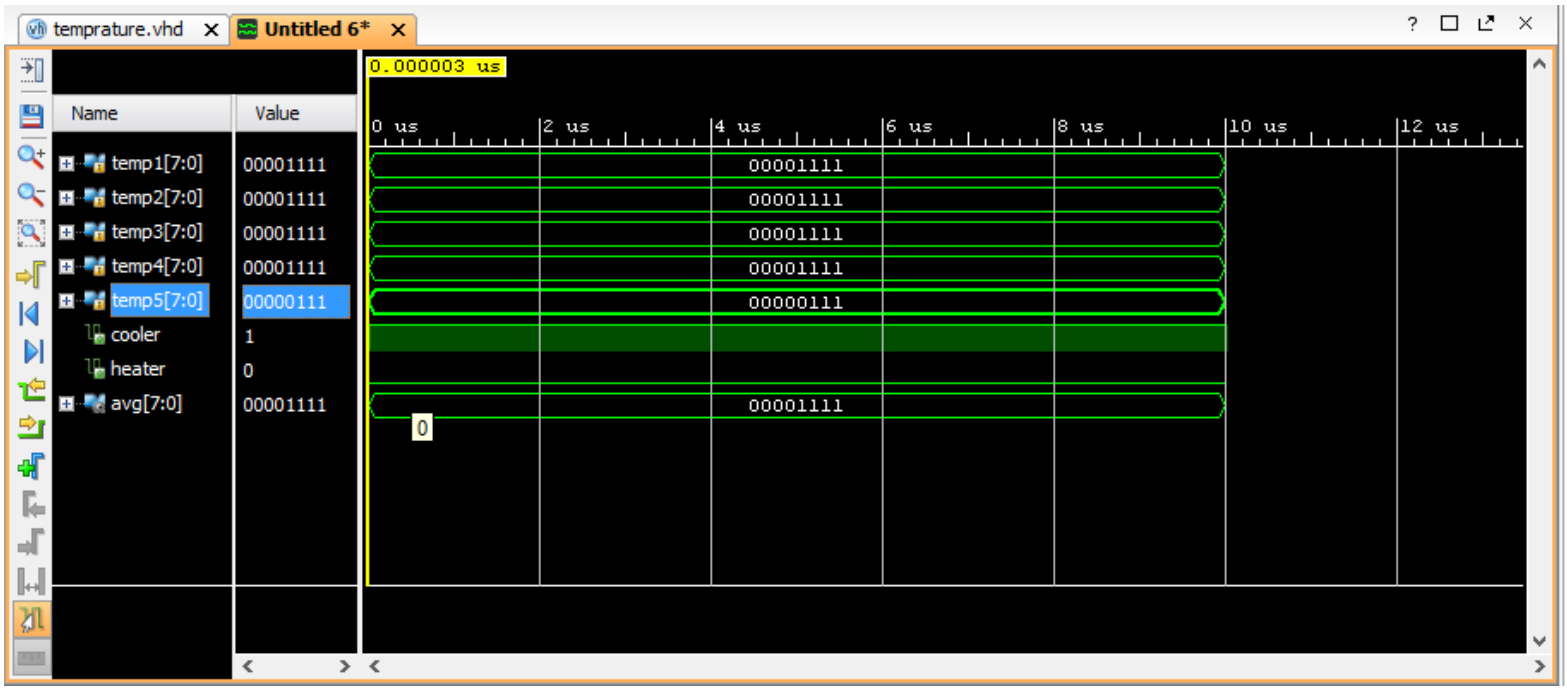
سوال ۱۲ :

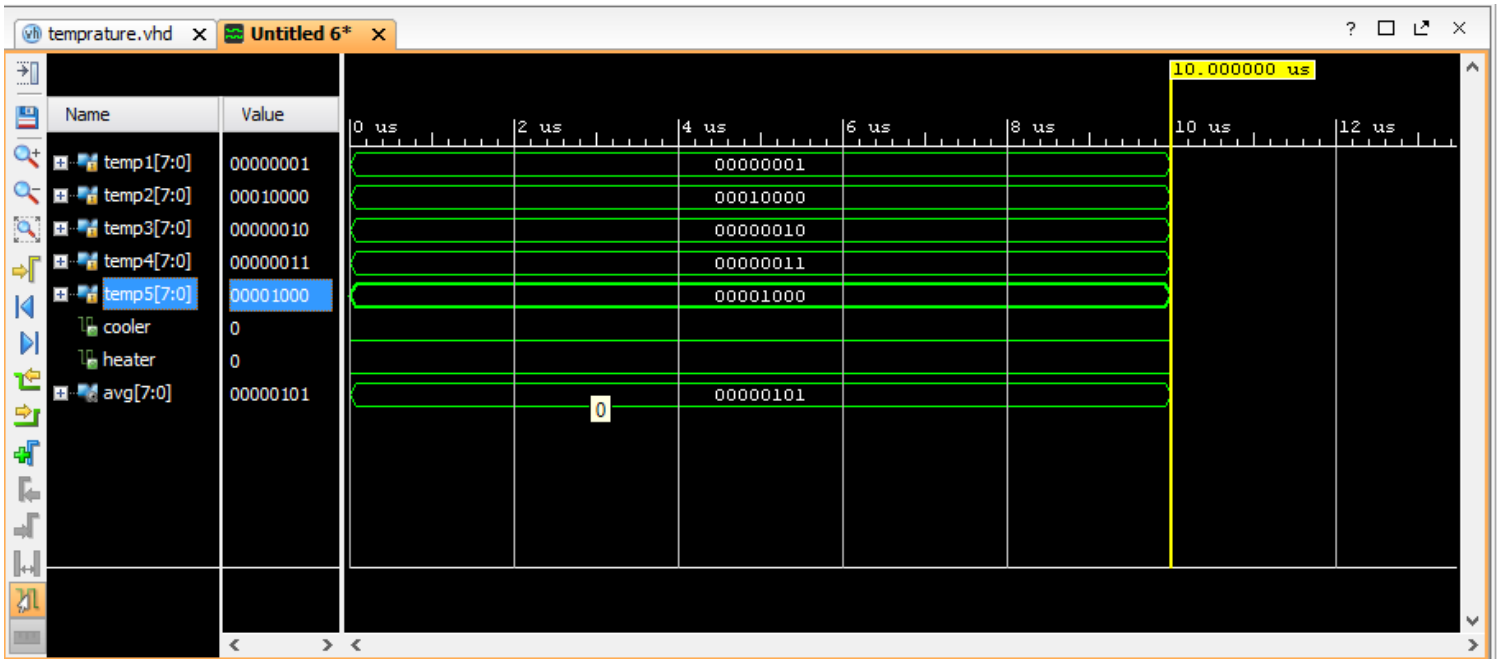
کد این سوال برای هر سه قسمت برابر زیر است :

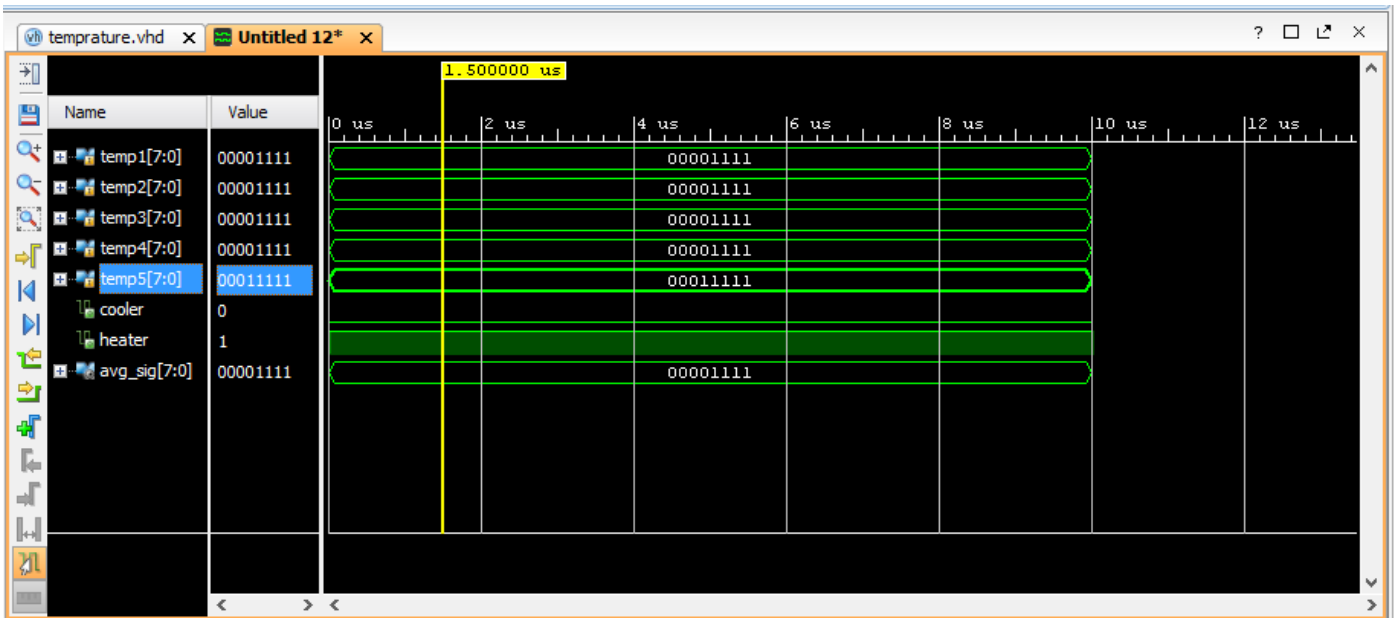
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_unsigned.ALL;
use ieee.numeric_std.all;

entity temprature is Port (
temp1 : in std_logic_vector( 7 downto 0 ) ;
temp2 : in std_logic_vector( 7 downto 0 ) ;
temp3 : in std_logic_vector( 7 downto 0 ) ;
temp4 : in std_logic_vector( 7 downto 0 ) ;
temp5 : in std_logic_vector( 7 downto 0 ) ;
cooler : out  bit ;
heater : out  bit );
```

```
end temprature;

architecture concurrent of temprature is
signal avg : std_logic_vector( 7 downto 0 ) ;
begin

avg <= std_logic_vector(shift_right(unsigned(temp1 + temp2 + temp3 +
temp4) , natural(2)));

cooler <= '0' when avg < temp5 + 4 else
          '0' when avg > temp5 - 4 and avg < temp5 + 4 else
          '1';
heater <= '1' when avg < temp5 - 4 else
          '0' when avg > temp5 - 4 and avg < temp5 + 4 else
          '0';
end concurrent;

architecture sequential of temprature is
signal avg_sig : std_logic_vector( 7 downto 0 ) ;
begin
process(temp1 , temp2 , temp3 , temp4 , temp5)
variable avg : std_logic_vector( 7 downto 0 ) ;
begin
avg := std_logic_vector(shift_right(unsigned(temp1 + temp2 + temp3 +
temp4) , natural(2)));
if( avg  < temp5 - 4 ) then
heater <= '1' ;
cooler <= '0';
elsif( avg > temp5 - 4 and avg < temp5 + 4 ) then
heater <= '0';
cooler <= '0';
else
heater <= '0';
cooler <= '1';
end if;
avg_sig <= avg;
end process;

end sequential;
```

برای کد بالا شکل موج های زیر تولید شده است :


temprature.vhd
Untitled 6*
0.000003 us
Name
Value
temp1[7:0]
00001111
temp2[7:0]
00001111
temp3[7:0]
00001111
temp4[7:0]
00001111
temp5[7:0]
00000111
cooler
1
heater
0
avg[7:0]
00001111
0 us
2 us
4 us
6 us
8 us
10 us
12 us
00001111
00001111
00001111
00001111
00000111
00001111
0


temprature.vhd
Untitled 6*
10.000000 us
Name
Value
temp1[7:0]
00000001
temp2[7:0]
00010000
temp3[7:0]
00000010
temp4[7:0]
00000011
temp5[7:0]
00001000
cooler
0
heater
0
avg[7:0]
00000101
0 us
2 us
4 us
6 us
8 us
10 us
12 us
00000001
00010000
00000010
00000011
00001000
00000101
0



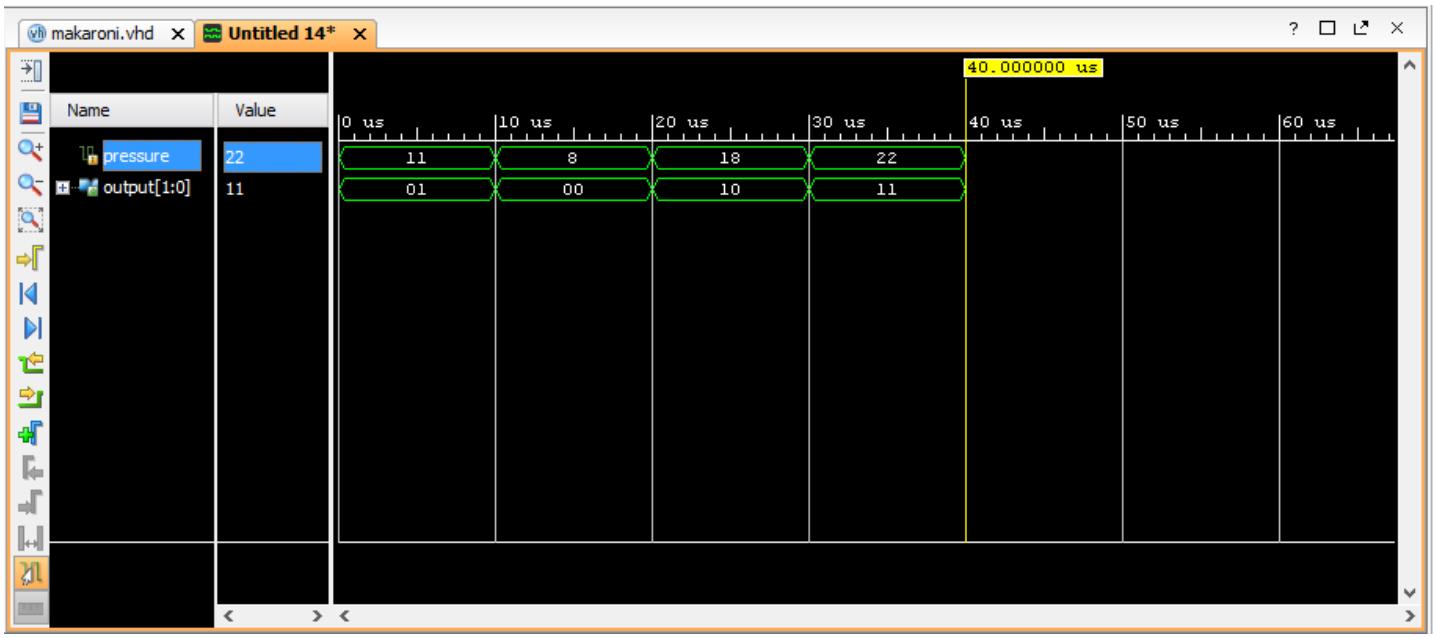
سوال ۱۳ :

کد این مدار به صورت زیر است :

```
entity makaroni is Port (
pressure : in integer ;
output : out std_logic_vector( 1 downto 0)
);
end makaroni;

architecture Behavioral of makaroni is
begin

output <= "00" when pressure >= 5 and pressure <= 10 else
          "01" when pressure > 10 and pressure <= 15 else
          "10" when pressure > 15 and pressure <= 20 else
          "11" when pressure > 20 and pressure <= 25 else
          "00";
```

```
with pressure select
    output <= "00" when 5 to 10,
              "01" when 11 to 15,
              "10" when 16 to 20,
              "11" when 21 to 25,
              "00" when others;
end Behavioral;
```

شکل موج آن به صورت زیر است :



سوال ۱۴ :

```
----------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/02/2017 02:14:36 PM
-- Design Name:
-- Module Name: frequency_divider - Behavioral
```

```
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;


use IEEE.numeric_std.ALL;

entity frequency_divider is
generic (N : integer := 10 );
port (
clk,reset : in std_logic;
clk_out : out std_logic);
end frequency_divider;

architecture Behavioral of frequency_divider is
signal count: integer:=0;
signal tmp : std_logic := '1';
begin
```

```
process(clk,reset)
begin
if(reset='0') then
    count<=0;
    tmp<='1';
elsif(clk'event and clk='1') then
    count <=count+1;
    if (count = N) then
        tmp <= NOT tmp;
        count <= 0;
    end if;
end if;

clk_out <= tmp;
end process;

end Behavioral;
```

شکل موج آن به صورت زیر است :