

Sistemas Críticos

Tema 1:

Selección y configuración de un sistema operativo

Lección 2:

Selección y configuración de la plataforma de ejecución



Contenidos

Tema 1: Selección y configuración de un sistema operativo

Introducción

Fundamentos de *Linux*

Selección de la plataforma y prerequisites del sistema

Diseño de una plataforma de ejecución mínima

Construcción del *kernel* de *Linux*

Construcción del *Device Tree Blob*

Necesidad de un *Root File System*

Construcción de un *Root File System*

Generación del *First Stage Boot Loader*

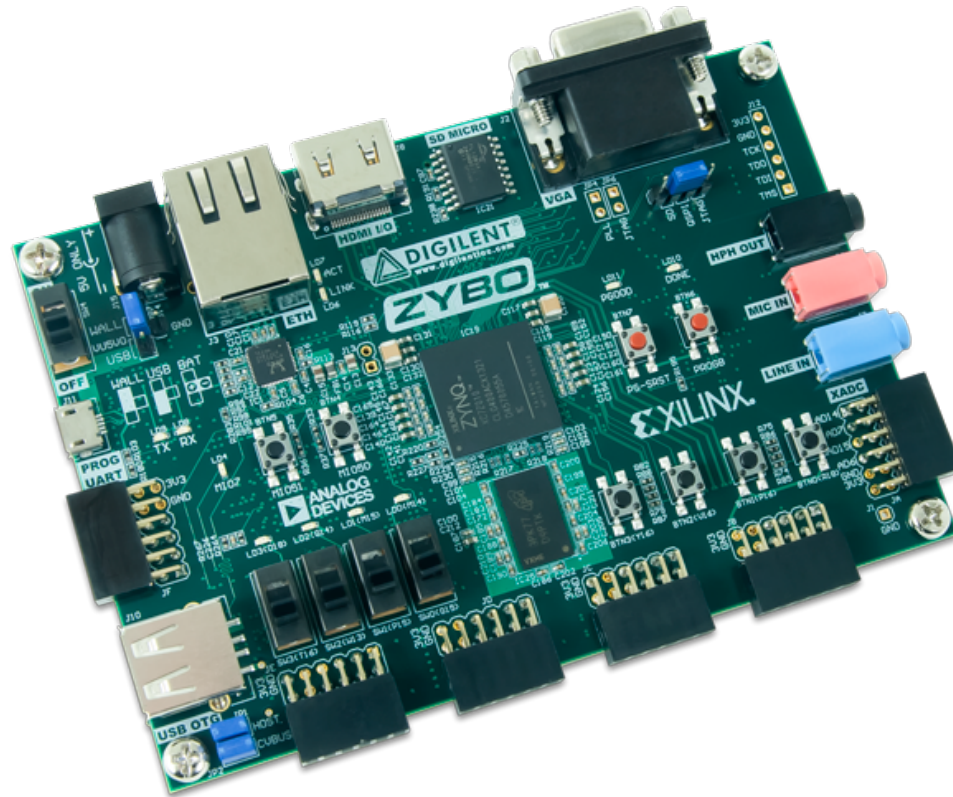
Construcción de *U-Boot*

Preparación de la imagen de arranque

Plataforma

Diligent Zybo

Placa de desarrollo basada en el SoC Zynq de Xilinx.



Simulador

QEMU

Simulador de procesadores y sistemas completos.

Soporta el SoC Zynq de Xilinx **a partir de la versión 2.0**

```
-redir tcp:10023::23 -redir tcp:10080::80 -red...  
[ 2.840573] TCP: cubic registered  
[ 2.841002] NET: Registered protocol family 17  
[ 2.842287] zynq_pm_remap_ocm: OCM pool is not available  
[ 2.842795] zynq_pm_late_init: Unable to map OCM.  
[ 2.843593] Registering SWP/SWPB emulation handler  
[ 2.853919] regulator-dummy: disabling  
[ 2.857294] drivers/rtc/hctosys.c: unable to open rtc device (rtc0)  
[ 2.954007] ALSA device list:  
[ 2.954515]   No soundcards found.  
[ 2.968970] Freeing unused kernel memory: 204K (c06e4000 - c0717000)  
Iniciando rcS...  
loadkmap: can't open console  
++ Montando los sistemas de archivos  
++ Inicializando los dispositivos  
++ Configurando la IP estática IP 192.168.1.10  
[ 5.328829] xemacps e000b000.ethernet: eth0: no PHY setup  
++ Iniciando el demonio telnet  
++ Iniciando el demonio http  
[ 5.879368] NET: Registered protocol family 10  
++ Iniciando el demonio ftp  
rcS completado  
  
ARM-Linux desde cero xilinx_zynq_a9 /dev/ttyPS0  
xilinx_zynq_a9 login: █
```

Prerrequisitos

Herramientas de *Xilinx*

Descargamos *Vivado* and *SDK Standalone Web Install Client*

<http://www.xilinx.com/support/download.html>

Incluimos las herramientas de *Xilinx* en el PATH

```
XILINX_ROOT=/opt/Xilinx  
PATH=$PATH:$XILINX_ROOT/SDK/2014.4/bin  
PATH=$PATH:$XILINX_ROOT/SDK/2014.4/gnu/arm/lin/bin  
PATH=$PATH:$XILINX_ROOT/Vivado/2014.4/bin  
export PATH
```

Herramientas de control de versiones

Git

```
sudo apt-get -y install git
```

Configuración de git para salir a través del *proxy* HTTP de la UGR

```
git config --global http.proxy http://stargate.ugr.es:3128  
git config --global https.proxy https://stargate.ugr.es:3128
```

Gmake

```
sudo ln -s /usr/bin/make /usr/bin/gmake
```

Prerrequisitos

Paquetes necesarios (*Ubuntu*, ya instalados en las aulas)

Para poder construir el RootFS del sistema con permisos de *root*

```
sudo apt-get -y install fakeroot
```

Para poder simular nuestro sistema empotrado

```
sudo apt-get -y install qemu-user qemu-system-arm
```

La versión 2.0 de Qemu se integra a partir de Ubuntu 14.04 (trusty)

Configuración de *wget* para salir a través del *proxy* HTTP de la UGR

Crear el fichero `${HOME}/.wgetrc` con el siguiente contenido

```
use_proxy = on
http_proxy = http://stargate.ugr.es:3128/
https_proxy = http://stargate.ugr.es:3128/
ftp_proxy = http://stargate.ugr.es:3128/
```

Directorio de nuestro proyecto

```
export PRJ_ROOT="${HOME}/zynq-linux"
```

Contenidos

Tema 1: Selección y configuración de un sistema operativo

Introducción

Fundamentos de *Linux*

Selección de la plataforma y prerequisites del sistema

Diseño de una plataforma de ejecución mínima

Construcción del *kernel* de *Linux*

Construcción del *Device Tree Blob*

Necesidad de un *Root File System*

Construcción de un *Root File System*

Generación del *First Stage Boot Loader*

Construcción de *U-Boot*

Preparación de la imagen de arranque

Creamos un proyecto en Vivado



Creamos un proyecto en *Vivado*

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.



Project name:

Project location:

☒ Create project subdirectory

Project will be created at: .../zynq-linux/platform

< Back

Next >

Finish

Cancel

New Project

Project Type

Specify the type of project to create.



- ☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time
- ☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time
- ☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Configure an Example Embedded Evaluation Board Design**
Create a new Vivado project from a predefined IP Integrator template design.

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Next >

Finish

Cancel

Next Page

Creamos un proyecto en *Vivado*

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project.

Index	Name	Library	HDL Source For
-------	------	---------	----------------

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

Target language: **VHDL** Simulator language: **Mixed**

New Project

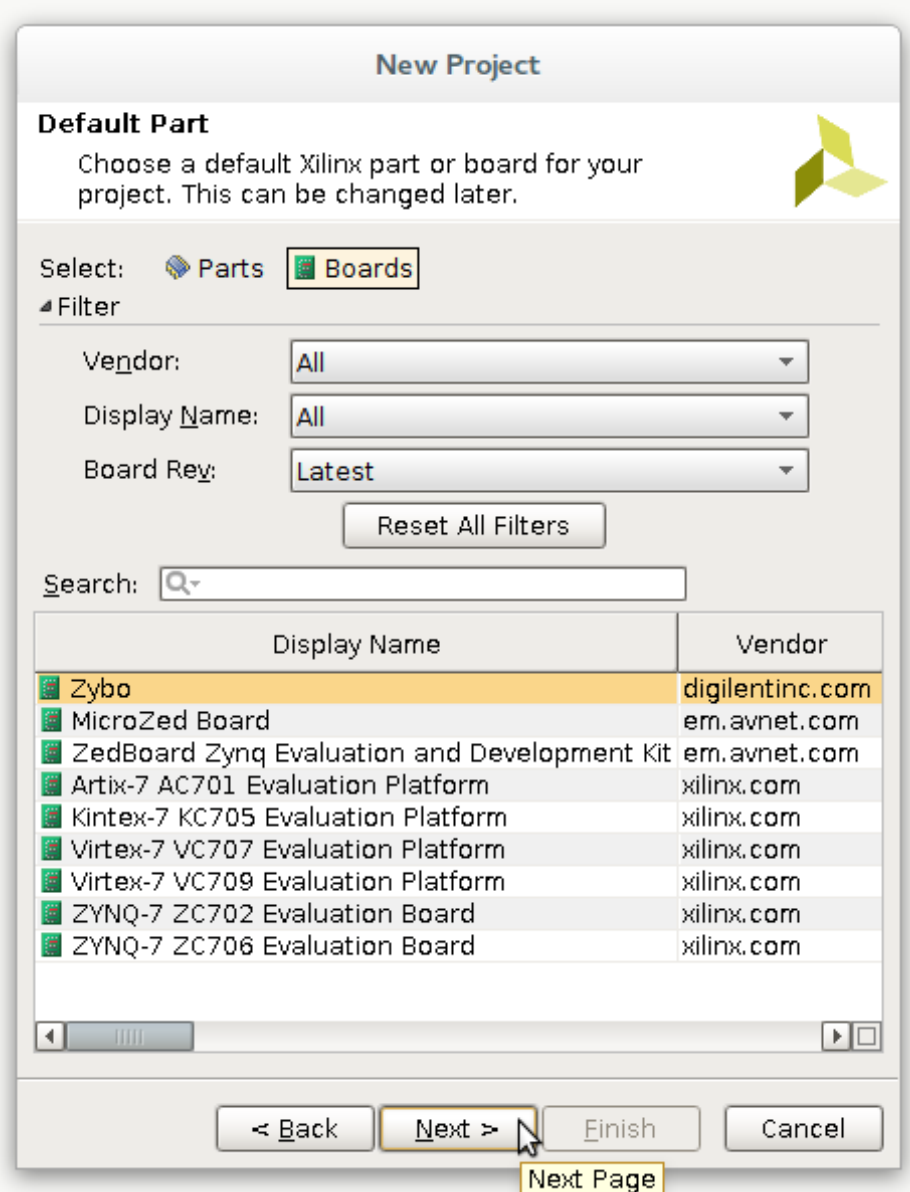
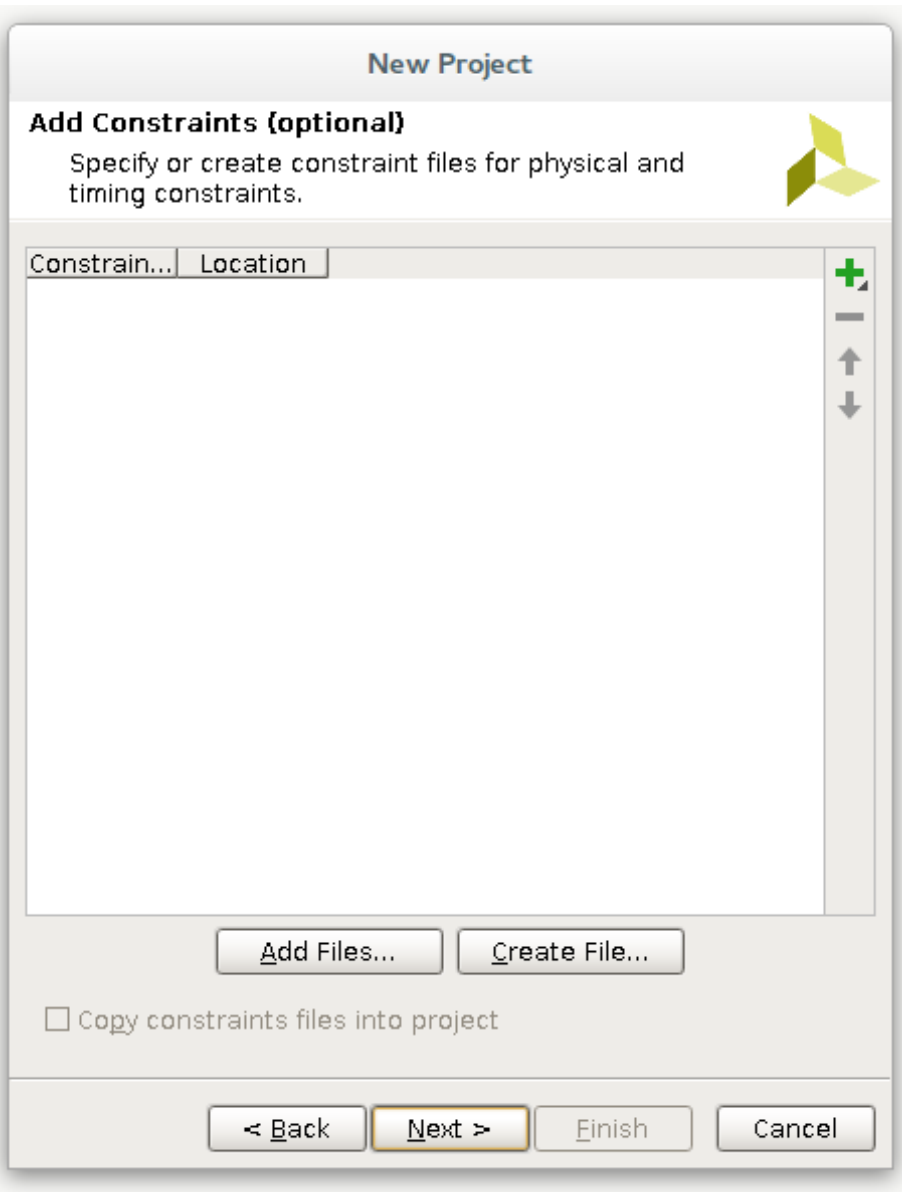
Add Existing IP (optional)

Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.

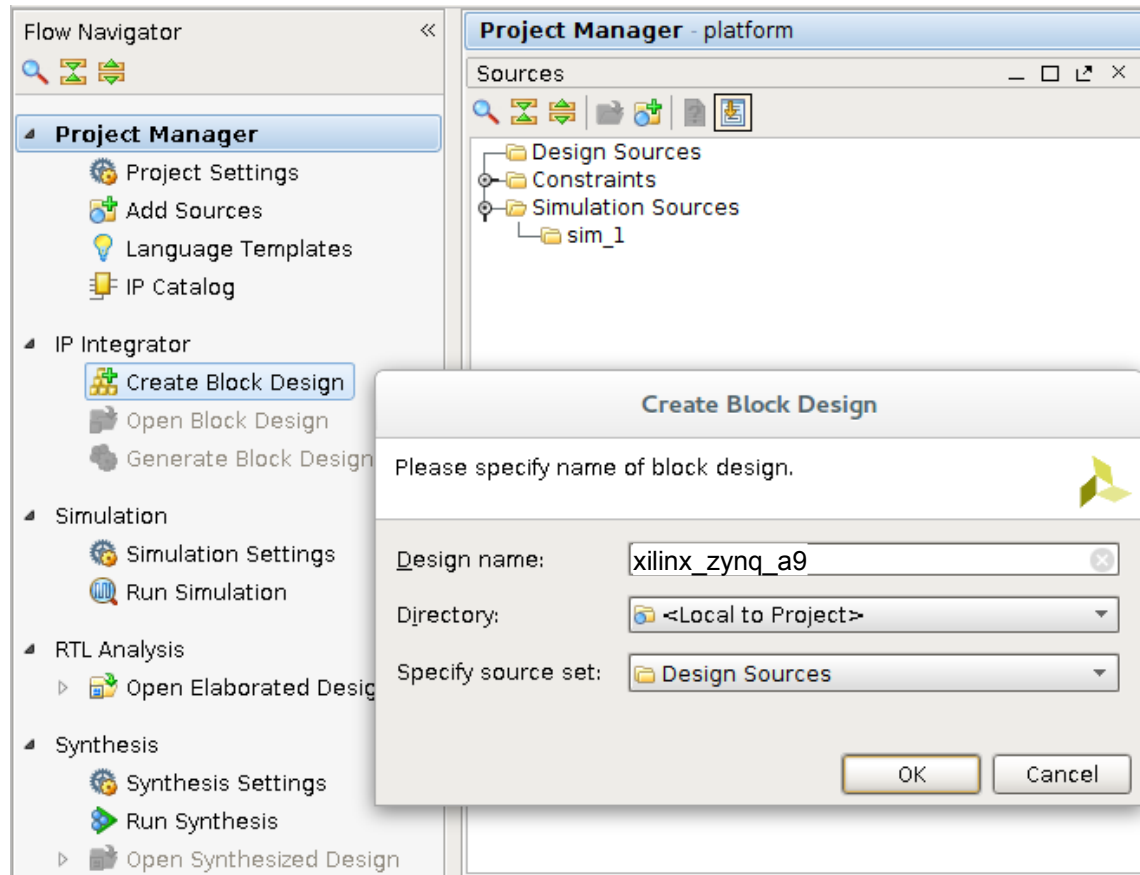
Index	Name	Library	HDL Sour...	Location
-------	------	---------	-------------	----------

☐ Copy sources into project

Creamos un proyecto en *Vivado*



Creamos un diseño mínimo



Añadimos el SoC Zynq de Xilinx

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

Flow Navigator

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 - Bitstream Settings
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Block Design - zynq_platform

Design

zynq_platform

Diagram

This design is empty. To get started, [Add IP](#) from the catalog.

Search: zyn (2 matches)

Name	VLNV
ZYNQ7 Processing System	xilinx.com...
ZYNQ7 Processing System BFM	xilinx.com...

Select and press ENTER or drag and drop, ESC to cancel

Properties

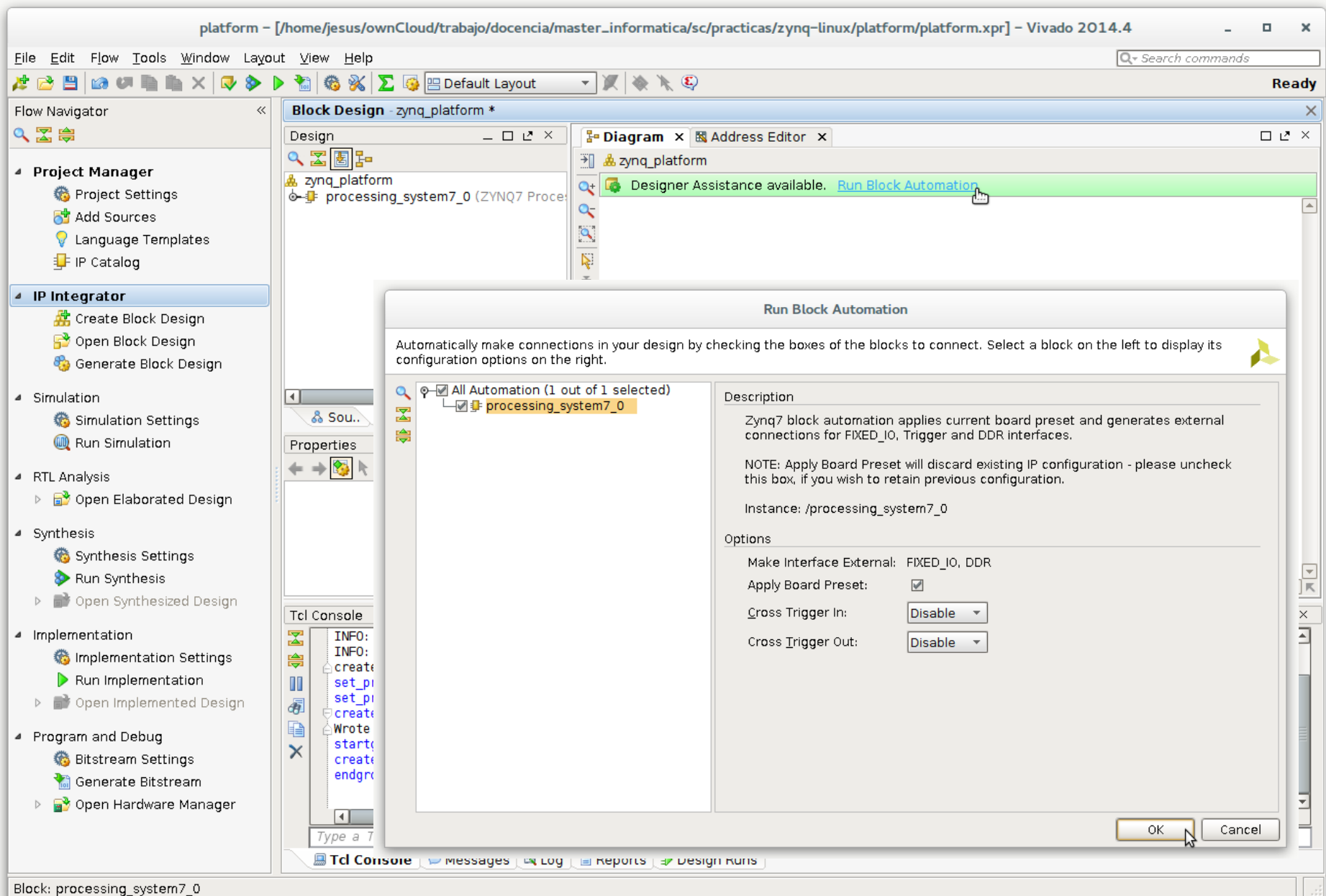
Tcl Console

```
start_gui
create_project platform /home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform -part xc7z010clg400-
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2014.4/data/ip'.
create_project: Time (s): cpu = 00:00:15 ; elapsed = 00:00:07 . Memory (MB): peak = 5734.238 ; gain = 54.902 ; free physical = 207 ; t
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
set_property target_language VHDL [current_project]
create_bd_design "zynq_platform"
Wrote : </home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.srsc/sources_1/bd/zynq_p
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Automatizamos las conexiones



Añadimos el controlador de memoria y el GPIO

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

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Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - processing_system7_0 (ZYNQ7 Processing System)

Diagram

zynq_platform

processing_system7_0

PTP_ETHERNET_0

DDR

FIXED_IO

SDIO_0

USBIND_0

M_AXI_GP0

TTC0_WAVE0_OUT

TTC0_WAVE1_OUT

TTC0_WAVE2_OUT

FCLK_CLK0

FCLK_RESET0_N

M_AXI_GP0_ACLK

ZYNQ

ZYNQ7 Processing System

Add IP

Block Properties

processing_system7_0

Name: processing_system7_0

Parent name: zynq_platform

General Properties IP

Tcl Console

```
create_project: Time (s): cpu = 00:00:15 ; elapsed = 00:00:07 . Memory (MB): peak = 5734.238 ; gain = 54.902 ; free physical = 207 ;
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
set_property target_language VHDL [current_project]
create_bd_design "zynq_platform"
Wrote : </home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.srscs/sources_1/bd/zynq_p
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master
apply_bd_automation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 5831.957 ; gain = 19.367 ; free physical = 38
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Add IP

Automatizamos las conexiones

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyqn-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

Search commands

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Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - axi_bram_ctrl_0 (AXI BRAM Controller:4.0)
 - axi_gpio_0 (AXI GPIO:2.0)
 - processing_system7_0 (ZYNQ7 Processing System)

Diagram

zynq_platform

Designer Assistance available. [Run Connection Automation](#)

axi_bram_ctrl_0

AXI BRAM Controller

axi_gpio_0

AXI GPIO

processing_system7_0

ZYNQ7 Processing System

Block Properties

processing_system7_0

Name: processing_system7_0

Parent name: zynq_platform

General Properties IP

Tcl Console

```
apply_bd_automation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 5831.957 ; gain = 19.367 ; free physical = 38400
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_gpio:2.0 axi_gpio_0
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_bram_ctrl:4.0 axi_bram_ctrl_0
endgroup
set_property location {1 142 154} [get_bd_cells axi_bram_ctrl_0]
set_property location {1 133 223} [get_bd_cells axi_gpio_0]
set_property location {1 144 84} [get_bd_cells axi_bram_ctrl_0]
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Block: processing_system7_0

Automatizamos las conexiones

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

Search commands

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 - Open Hardware Manager

Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - axi_bram_ctrl_0 (AXI BRAM Controller:4
 - axi_gpio_0 (AXI GPIO:2.0)
 - processing_system7_0 (ZYNQ7 Proc

Diagram

zynq_platform

Designer Assistance available. [Run Connection Automation](#)

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

All Automation (5 out of 5 selected)

- axi_bram_ctrl_0
 - BRAM_PORTA
 - BRAM_PORTB
 - S_AXI
- axi_gpio_0
 - GPIO
 - S_AXI

Description

Connect Slave interface (/axi_bram_ctrl_0/S_AXI) to a selected Master address space.

Options

Master: /processing_system7_0/M_AXI_GP0

Clock Connection (for unconnected clks): Auto

OK Cancel

Tcl Console

```
apply_bd_automation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 5831.957 ; gain = 19.367 ; free physical = 38
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_gpio:2.0 axi_gpio_0
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_bram_ctrl:4.0 axi_bram_ctrl_0
endgroup
set_property location {1 142 154} [get_bd_cells axi_bram_ctrl_0]
set_property location {1 133 223} [get_bd_cells axi_gpio_0]
set_property location {1 144 84} [get_bd_cells axi_bram_ctrl_0]
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Block: processing_system7_0

Automatizamos las conexiones

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

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Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - axi_bram_ctrl_0 (AXI BRAM Controller:4
 - axi_gpio_0 (AXI GPIO:2.0)
 - processing_system7_0 (ZYNQ7 Proce

Diagram

zynq_platform

Designer Assistance available. [Run Connection Automation](#)

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

All Automation (5 out of 5 selected)

- axi_bram_ctrl_0
 - BRAM_PORTA
 - BRAM_PORTB
 - S_AXI
- axi_gpio_0
 - GPIO
 - S_AXI

Description

Connect Board Part Interface to IP interface.

Interface: /axi_gpio_0/GPIO

Options

Select Board Part Interface: btns_4bits

- btns_4bits
- leds_4bits
- sws_4bits
- Custom

OK Cancel

Tcl Console

```
apply_bd_automation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 5831.957 ; gain = 19.367 ; free physical = 38
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_gpio:2.0 axi_gpio_0
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_bram_ctrl:4.0 axi_bram_ctrl_0
endgroup
set_property location {1 142 154} [get_bd_cells axi_bram_ctrl_0]
set_property location {1 133 223} [get_bd_cells axi_gpio_0]
set_property location {1 144 84} [get_bd_cells axi_bram_ctrl_0]
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Block: processing_system7_0

Automatizamos las conexiones

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

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Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - axi_bram_ctrl_0 (AXI BRAM Controller:4
 - axi_gpio_0 (AXI GPIO:2.0)
 - processing_system7_0 (ZYNQ7 Proc

Diagram x Address Editor x

zynq_platform

Designer Assistance available. [Run Connection Automation](#)

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

All Automation (5 out of 5 selected)

- axi_bram_ctrl_0
 - BRAM_PORTA
 - BRAM_PORTB
 - S_AXI
- axi_gpio_0
 - GPIO
 - S_AXI

Description

Connect Slave interface (/axi_gpio_0/S_AXI) to a selected Master address space.

Options

Master: /processing_system7_0/M_AXI_GP0

Clock Connection (for unconnected clks): Auto

OK Cancel

Tcl Console

```
apply_bd_automation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 5831.957 ; gain = 19.367 ; free physical = 38
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_gpio:2.0 axi_gpio_0
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:axi_bram_ctrl:4.0 axi_bram_ctrl_0
endgroup
set_property location {1 142 154} [get_bd_cells axi_bram_ctrl_0]
set_property location {1 133 223} [get_bd_cells axi_gpio_0]
set_property location {1 144 84} [get_bd_cells axi_bram_ctrl_0]
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Block: processing_system7_0

Regeneramos el *layout* del diseño

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyqn-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

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Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - Nets
 - axi_bram_ctrl_0 (AXI BRAM Controller)
 - BRAM_PORTA
 - BRAM_PORTB
 - S_AXI
 - s_axi_aclk
 - s_axi_aresetn
 - axi_bram_ctrl_0_bram (Block Memory Generator)
 - axi_gpio_0 (AXI GPIO:2.0)
 - GPIO

Block Properties

axi_gpio_0

Name: axi_gpio_0

Parent name: zynq_platform

General Properties IP

Diagram

zynq_platform

Address Editor

rst_processing_system7_0_100M

Processor System Reset

processing_system7_0

ZYNQ

ZYNQ7 Processing System

processing_system7_0_axi_periph

AXI Interconnect

axi_gpio_0

AXI GPIO

- axi_bram_ctrl_0
- AXI BRAM Controller
- axi_bram_ctrl_0_bram
- Block Memory Generator
- leds_4bits
- DDR
- FIXED_IO

Tcl Console

```
redo
INFO: [Common 17-16] redo 'startgroup'
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GP0" Clk "Au
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "leds_4bits" } [get_bd_intf_pi
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GP0" Clk "Au
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "New Blk_Mem_Gen" } [get_bd_intf_pir
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "Blk_Mem_Gen of BRAM_PORTA" } [get_b
INFO: [Common 17-16] redo 'endgroup'
redo: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 5877.082 ; gain = 2.004 ; free physical = 299 ; free virtual
regenerate_bd_layout
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Block: rst_processing_system7_0_100M

Fijamos el tamaño máximo de la BRAM

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

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Block Design - zynq_platform *

Design

- axi_bram_ctrl_0 (AXI BRAM Controller:4)
- BRAM_PORTA
- BRAM_PORTB
- S_AXI
 - s_axi_aclk
 - s_axi_aresetn
- axi_bram_ctrl_0_bram (Block Memory Generator)
- axi_gpio_0 (AXI GPIO:2.0)
 - GPIO
 - S_AXI
 - s_axi_aclk
 - s_axi_aresetn
- processing_system7_0 (ZYNQ7 Processing System)

Diagram

Address Editor

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 4G)					
axi_gpio_0	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
axi_bram_ctrl_0	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF

Address Segment Properties

SEG_axi_bram_ctrl_0_Mem0

Name: SEG_axi_bram_ctrl_0

Full name: processing_system7_0

Slave Interface: axi_bram_ctrl_0/S

Tcl Console

```
redo
INFO: [Common 17-16] redo 'startgroup'
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GP0" Clk "Au
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "leds_4bits" } [get_bd_intf_pi
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GP0" Clk "Au
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "New Blk_Mem_Gen" } [get_bd_intf_pir
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "Blk_Mem_Gen of BRAM_PORTA" } [get_t
INFO: [Common 17-16] redo 'endgroup'
redo: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 5877.082 ; gain = 2.004 ; free physical = 299 ; free virtual
regenerate_bd_layout
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Address Segment: SEG_axi_bram_ctrl_0_Mem0

Validamos el diseño

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyqnx-linux/platform/platform.xpr] - Vivado 2014.4

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 - Open Hardware Manager

Block Design - zynq_platform *

Design

- axi_bram_ctrl_0 (AXI BRAM Controller:4)
- BRAM_PORTA
- BRAM_PORTB
- S_AXI
- s_axi_aclk
- s_axi_aresetn
- axi_bram_ctrl_0_bram (Block Memory Generator)
- axi_gpio_0 (AXI GPIO:2.0)
- GPIO
- S_AXI
- s_axi_aclk
- s_axi_aresetn
- processing_system7_0 (ZYNQ7 Process)

Address Segment Properties

SEG_axi_bram_ctrl_0_Mem0

Name: SEG_axi_bram_ctrl_0

Full name: processing_system7_0

Slave Interface: axi_bram_ctrl_0

Diagram

zynq_platform

Validate Design (F6)

Validate and display errors and critical warnings in this design.

Tcl Console

```
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GPIO" Clk "Acl
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:board -config {BoardInterface "leds_4bits" } [get_bd_intf_pi
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:axi4 -config {Master "/processing_system7_0/M_AXI_GPIO" Clk "Acl
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "New Blk_Mem_Gen" } [get_bd_intf_pir
INFO: [Common 17-16] redo 'apply_bd_automation -rule xilinx.com:bd_rule:bram_cntlr -config {BRAM "Blk_Mem_Gen of BRAM_PORTA" } [get_t
INFO: [Common 17-16] redo 'endgroup'
redo: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 5877.082 ; gain = 2.004 ; free physical = 299 ; free virtual
regenerate_bd_layout
set_property range 64K [get_bd_addr_segs {processing_system7_0/Data/SEG_axi_bram_ctrl_0_Mem0}]
regenerate_bd_layout
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Validate and display errors and critical warnings in this design

Generación de los ficheros HDL

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyng-linux/platform/platform.xpr] - Vivado 2014.4

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 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Block Design - zynq_platform *

Design

- zynq_platform
 - External Interfaces
 - Interface Connections
 - Nets
 - axi_bram_ctrl_0 (AXI BRAM Controller)
 - BRAM_PORTA
 - BRAM_PORTB
 - S_AXI
 - s_axi_aclk
 - s_axi_aresetn
 - axi_bram_ctrl_0_bram (Block Memory Generator)
 - axi_gpio_0 (AXI GPIO:2.0)
 - GPIO

Diagram

zynq_platform

Generate Output Products

The following output products will be generated.

Preview

- zynq_platform.bd
 - Synthesis
 - Implementation
 - Simulation

Out-of-Context Settings...

Generate Cancel

Tcl Console

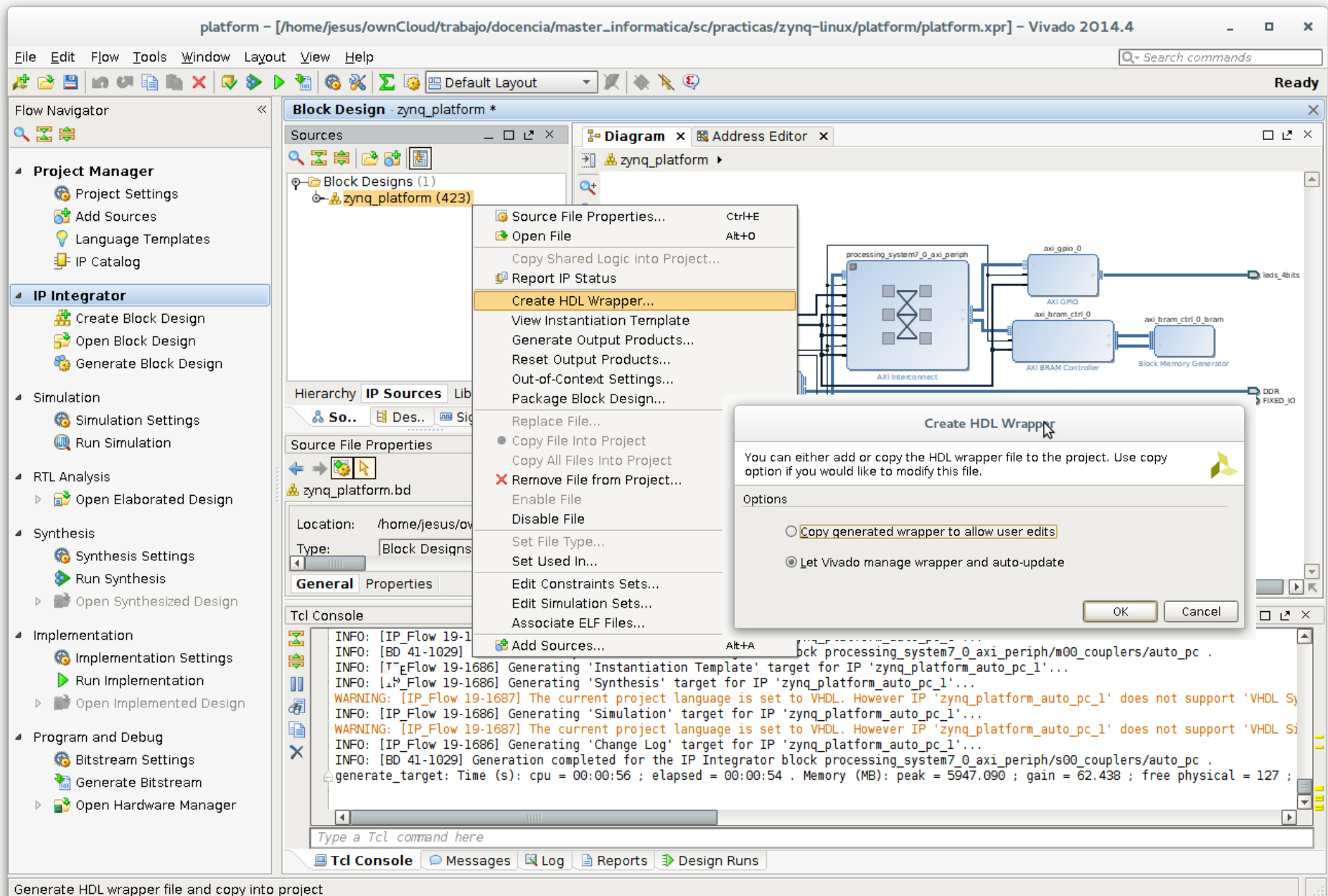
```
INFO: [Common 17-16] redo 'apply_bd_automation -rule 'Generate' -args {}'
INFO: [Common 17-16] redo 'apply_bd_automation -rule 'Generate' -args {}'
INFO: [Common 17-16] redo 'apply_bd_automation -rule 'Generate' -args {}'
INFO: [Common 17-16] redo 'endgroup'
redo: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 5877.082 ; gain = 2.004 ; free physical = 299 ; free virtual = 1023.916
regenerate_bd_layout
set_property range 64K [get_bd_addr_segs {processing_system7_0/Data/SEG_axi_bram_ctrl_0_Mem0}]
regenerate_bd_layout
validate_bd_design
validate_bd_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:07 . Memory (MB): peak = 5882.652 ; gain = 0.000 ; free physical = 161 ; free virtual = 1023.916
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Generate outputs needed for synthesis, simulation and implementation

Creamos el HDL Wrapper para el SDK



Generate HDL wrapper file and copy into project

Síntesis del diseño

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyng-linux/platform/platform.xpr] - Vivado 2014.4

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- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Block Design - zynq_platform

Sources

- Design Sources (1)
 - zynq_platform_wrapper - STR
 - zynq_platform_i - zynq_platform
 - zynq_platform - STRUCTURE
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Hierarchy

Source File Properties

zynq_platform.bd

Location: /home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyng-linux/platform/platform.xpr

Type: Block Designs

General Properties

Run Synthesis

Run synthesis on your project source files.

Implementation

catch { write_hwdef -file zynq_platform_wrapper.hwdef }
synth_design -top zynq_platform_wrapper -part xc7z010 -package fgga900 -mode gw
Command: synth_design -top zynq_platform_wrapper -part xc7z010 -package fgga900 -mode gw
Starting synth_design
Attempting to get a license for fpga
INFO: [Common 17-349] Got license

Starting RTL Elaboration : Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak = 951.086 ; gain = 190.566 ; free physical =

Synthesis Implementation Simulation

Tcl Console Messages Log Reports Design Runs

Diagram

zynq_platform

Diagram showing the Zynq platform architecture, including the Processor System Reset, AXI Interconnect, AXI GPIO, AXI BRAM Controller, and Block Memory Generator.

Synthesis Completed

Synthesis successfully completed.

Next

- ☒ Run Implementation
- ☐ Open Synthesized Design
- ☐ View Reports

☐ Don't show this dialog again

OK Cancel

Implementación y generación del *bitstream*

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyq-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

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 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Block Design - zynq_platform

Sources

- Design Sources (1)
 - zynq_platform_wrapper - STR
 - zynq_platform_i - zynq_platform
 - zynq_platform - STRUCTURE
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Hierarchy

Source File Properties

zynq_platform.bd

Location: /home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyq-linux/platform/platform.xpr

Type: Block Designs

General Properties

Implementation Completed

Implementation successfully completed.

Next

- ☐ Open Implemented Design
- ☒ Generate Bitstream
- ☐ View Reports
- ☐ Don't show this dialog again

OK Cancel

Run Synthesis

Run synthesis on your project source files.

```
# catch { write_hwdef -file zynq_platform_wrapper -top zynq_platform }
# synth_design -top zynq_platform
Command: synth_design -top zynq_platform
Starting synth_design
Attempting to get a license for fpga
INFO: [Common 17-349] Got license
```

Starting RTL Elaboration : Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak = 951.086 ; gain = 190.566 ; free physical =

Synthesis Implementation Simulation

Tcl Console Messages Log Reports Design Runs

Run synthesis on your project source files

Implementación y generación del *bitstream*

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyq-linux/platform/platform.xpr] - Vivado 2014.4

File Edit Flow Tools Window Layout View Help

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Block Design - zynq_platform

Sources

- Design Sources (1)
 - zynq_platform_wrapper - STR
 - zynq_platform_i - zynq_platform
 - zynq_platform - STRUCTURE
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Hierarchy

Source File Properties

zynq_platform.bd

Location: /home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zyq-linux/platform/platform.xpr

Type: Block Designs

General Properties

Run Synthesis

Run synthesis on your project source files.

Implementation

Run synthesis on your project source files.

Starting synth_design

Attempting to get a license for f

INFO: [Common 17-349] Got license

Starting RTL Elaboration : Time (s): cpu = 00:00:20 ; elapsed = 00:00:21 . Memory (MB): peak = 951.086 ; gain = 190.566 ; free physical =

Diagram

zynq_platform

Diagram showing the Zynq platform architecture, including the Processor System Reset, AXI Interconnect, AXI GPIO, AXI BRAM Controller, and Block Memory Generator.

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

- ☒ Open Implemented Design
- ☐ View Reports
- ☐ Open Hardware Manager

☐ Don't show this dialog again

OK Cancel

Synthesis Implementation Simulation

Tcl Console Messages Log Reports Design Runs

Run synthesis on your project source files

Implementación y generación del *bitstream*

platform - [/home/jesus/ownCloud/trabajo/docencia/master_informatica/sc/practicas/zynq-linux/platform/platform.xpr] - Vivado 2014.4

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Search commands

write_bitstream Complete

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 - Implementation Settings
 - Run Implementation
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 - Constraints Wizard
 - Edit Timing Constraints
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 - Report Clock Networks
 - Report Clock Interaction
 - Report DRC
 - Report Noise

Implemented Design - xc7z010clg400-1 (active)

Netlist

- zynq_platform_wrapper
 - Nets (138)
 - Leaf Cells (4)
 - zynq_platform_i (zynq_platform)

Sources Netlist

Properties

Project Summary x Device x

Timing - Timing Summary - impl_1

This is a [saved report](#)

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.112 ns	Worst Hold Slack (WHS): 0.042 ns	Worst Pulse Width Slack
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints
Total Number of Endpoints: 4450	Total Number of Endpoints: 4450	Total Number of Endpoints

All user specified timing constraints are met.

Report Timing Summary
Specify analysis options and create a timing summary report.

Timing Summary - impl_1 x

Tcl Console Messages Log Reports Design Runs Timing

Specify analysis options and create a timing summary report

Automatización del diseño mediante *scripts*

Creación de un fichero tcl para nuestro diseño

Editar el fichero `vivado.jou` (generado por *Vivado* al hacer el diseño anterior)

Quitar los comentarios del principio (lineas comenzando con el carácter #)

Quitar (si existe) la ejecución del *script* `init.tcl` (se ejecuta al iniciar *Vivado*)

Quitar la orden `start_gui` (no vamos a usar el IDE de *Vivado*)

Reemplazar todas las ocurrencias de la ruta absoluta del proyecto por `$env(PLATFORM_DIR)`

(Ej. `/home/jesus/zynq-linux/my_platform` → `$env(PLATFORM_DIR)`)

Reemplazar todas las ocurrencias del nombre del proyecto por `$env(PLATFORM)`

(Ej. `my_platform` → `$env(PLATFORM)`)

Guardar el fichero resultante con extensión `.tcl` (ej. `platform.tcl`)

Variables de entorno

```
export PLATFORM="xilinx_zynq_a9"
```

```
export PLATFORM_DIR="${PRJ_ROOT}/${PLATFORM}"
```

Generación automática de la plataforma

```
vivado -mode batch -source platform.tcl
```

Lecturas recomendadas

Vivado:

Xilinx. *Vivado Design Suite Tutorial. Design Flows Overview*. UG888 (v 2014.3)
http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/ug888-vivado-design-flows-overview-tutorial.pdf

Xilinx. *Vivado Design Suite User Guide. Using TCL Scripting*. UG894 (v 2014.4)
http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug894-vivado-tcl-scripting.pdf

Zynq:

L. H. Crockett, R. A. Elliot, M. A. Enderwitz y R. W. Stewart. *The Zynq Book. Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC*. Strathclyde Academic Media. <http://www.zynqbook.com/>

Xilinx. *Vivado Design Suite Tutorial. Embedded Processor Hardware Design*. UG940 (v 2014.4)
http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/ug940-vivado-tutorial-embedded-design.pdf

Zybo:

Diligent. *Zybo Reference Manual*.
http://www.digilentinc.com/data/products/zybo/zybo_rm_b_v6.pdf