Chapter 6 - The Operational Amplifier

Lecture 21
Section 6.7

MEMS 0031 Electrical Circuits

Mechanical Engineering and Materials Science Department
University of Pittsburgh

Student Learning Objectives

At the end of the lecture, students should be able to:

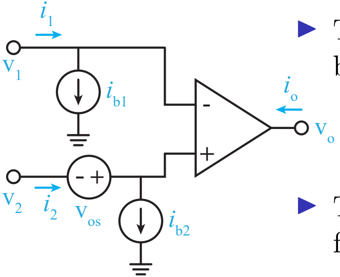
- Use the offsets model, finite gain model, and both the offsets and finite gain model to model the practical behavior of an operational amplifier
- Apply the CMRR model to the finite gain model to increase model fidelity

Practical Op-amps

- The non-ideal parameters of op-amps that we have thus ignored include:
  1. Non-zero bias currents
  2. Non-zero input offset voltage
  3. Finite input resistance
  4. Non-zero output resistance
  5. Finite voltage gain
- Including these increases the fidelity of our models, but the question we must ask: "is it worth it?"

Offsets Model

- The offsets model accounts for non-zero bias current (i_{b1} and i_{b2}) and non-zero input offset voltage (V_{os}), as shown below:



- The equations of behavior become:

$$i_1 = i_{b1}; \quad i_2 = i_{b2};$$
$$V_1 - V_2 = V_{os}$$

- This model does not account for finite input resistance

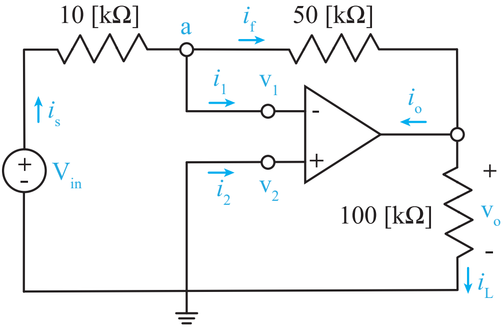
- The input offset current is defined as:

$$i_{os} = i_{b1} - i_{b2}$$

- The input offset bias current is typically on the order of tens of [pA] to tens of [nA], and V_{os} on the order tens of [nV] to tens of [mV]

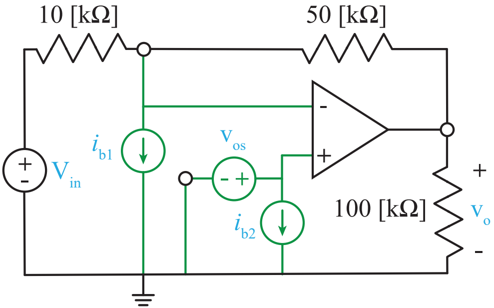
Example #1

- Consider a μA741 op-amp in an inverting configuration, where the gain is 5. Model as an ideal op-amp, and then use the offsets model.

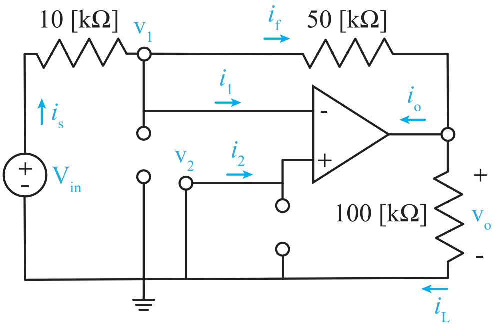


Example #1

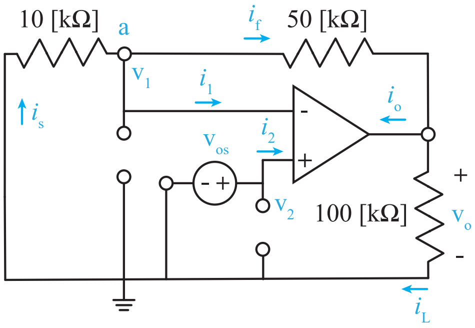
- Consider a μA741 op-amp in an inverting configuration, where the gain is 5. Model as an ideal op-amp, and then use the offsets model.



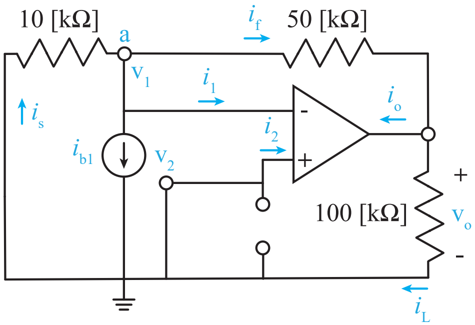
Example #1



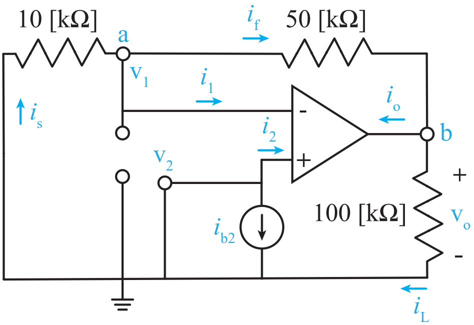
Example #1



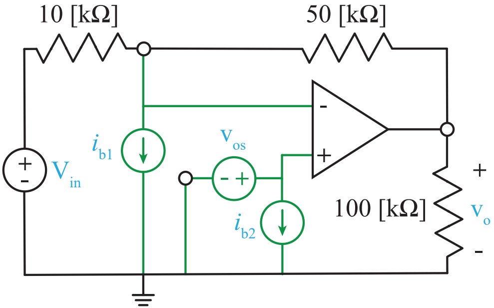
Example #1



Example #1

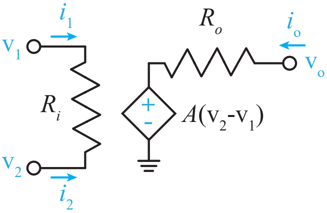


Example #1



Finite Gain Model

- The finite gain model accounts for:
  1. Finite input resistance, R_i;
  2. Non-zero output resistance, R_o;
  3. Finite voltage gain, V_o
- However, it does not include non-zero bias current nor non-zero input offset voltage
- The schematic of the finite gain model is shown below, with governing equations



$$V_o = A(V_2 - V_1) + R_o i_\mathrm{o}$$

$$i_1 = \frac{V_1 - V_2}{R_i}$$

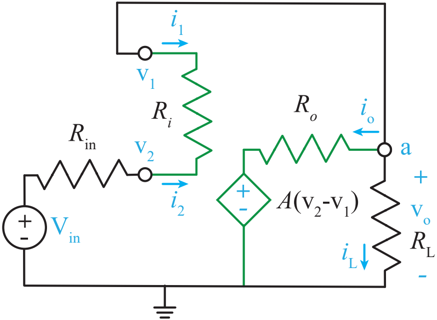
$$i_2 = \frac{V_2 - V_1}{R_i}$$

Example #2

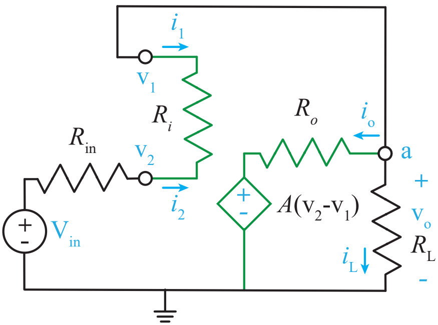
- A voltage follower (see Fig. 6.5-1 c) on pg. 217) acts as a buffer amplifier. The gain associated with a follower is unity. Model this type of amplifier using the finite gain model to quantify the effect of R_i and R_o on V_o, in comparison to the ideal model.

Givens:

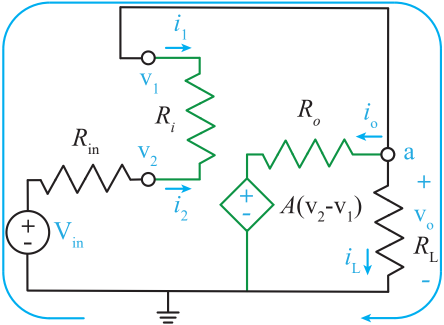
- R_in=1 [kΩ]
- R_L=10 [kΩ]
- R_i=100 [kΩ]
- R_o=100 [Ω]
- A=10^5



Example #2



Example #2



CMRR

- Another important parameter is the Common Mode Rejection Ratio (CMRR), which modifies the output of the op-amp in the finite gain model such that

$$A(V_2 - V_1) \rightarrow A(V_2 - V_1) + A_{\text{cm}}\left(\frac{V_1 + V_2}{2}\right)$$

- The third term is the common mode gain times the common mode input voltage
- Thus, the CMRR is:

$$\text{CMRR} = \frac{A}{A_{\text{cm}}}$$

- Thus, we can modify the finite gain model with

$$A(V_2 - V_1) \rightarrow A\left(\left(1 + \frac{1}{2\text{CMRR}}\right)V_2 - \left(1 - \frac{1}{2\text{CMRR}}\right)V_1\right)$$

Example #3

- Consider a μA741 op-amp. Determine the output of the VCVS using the finite gain model and compare to that using the finite gain model with CMRR.

Student Learning Objectives

At the end of the lecture, students should be able to:

- Use the offsets model, finite gain model, and both the offsets and finite gain model to model the practical behavior of an operational amplifier
  - The offsets model includes provisions for non-zero bias currents (on the order of pico- to nano-amps), and an offset voltage, on the order of nano- to milli-volts
  - The finite gain model considers device resistance and limits the voltage output of the Op-amp
- Apply the CMRR model to the finite gain model to increase model fidelity
  - The CMRR model is a way to quantify the rejection of simultaneous terminal inputs

Suggested Problems

- 6.7-1, 6.7-2, 6.7-3, 6.7-4