A Third-order MAF Based QT1-PLL That is Robust against Harmonically Distorted Grid Voltage with Frequency Deviation

Mohamed Mellouli, Mahmoud Hamouda, Senior *Member, IEEE*, Jaleleddine Ben Hadj Slama, *Senior Member, IEEE*, and Kamal Al-Haddad, *Life Fellow, IEEE*

***Abstract*—The quasi-type-l phase-locked loop (QT1-PLL) is a grid synchronization technique that has become very popular in recent years thanks to its attractive performance such as easy implementation, fast dynamic response, and good accuracy in steady-state operation. However, it is still vulnerable to operation under harmonically distorted grid voltages with frequency drift. This paper proposes a novel QT1-PLL based synchronization algorithm that makes an appropriate combination of two filters' types: an in-loop third-order moving average filter (MAF) with a reduced window width, and a simplified second-order fast delayed signal cancellation (FDSC) based prefiltering stage. The proposed PLL is named third-order MAF based QT1-PLL (TQT1-PLL). Though both TQT1-PLL's filters do not need any adaptive algorithm, it is able to reject non-triplen odd-harmonics and the fundamental frequency negative sequence (FFNS) even under grid frequency drift. Its correct operation is confirmed through numerical simulations and real-time implementation on a digital signal processor (DSP). Moreover, the obtained results confirm its ability to reduce the ripple in the estimated frequency and phase under distorted grid voltages and off-nominal frequency operation. Authors show also through an analytical development that the topology of the proposed TQT1-PLL can be extended to enable the rejection of the DC-offset.**

***Index Terms*— delayed signal cancellation (DSC), distributed power generation, harmonic distortion, moving average filter (MAF), phase-locked loop (PLL), power quality, stability.**

I. Introduction

The power injection from a renewable energy source (RES) into the grid is performed through a power electronic interface referred to as grid side converter (GSC) [1]. Due to high penetration level of RES into the grid, many countries updated their grid codes to ensure high quality of the injected power and a better stability of the power system. Consequently, the GSC's controller must involve a fault ride through (FRT) system to support the grid voltage under symmetrical and asymmetrical grid faults. Moreover, the GSC of RES is requested to injected high quality of ac current under normal and abnormal grid voltages [1-4].

To enable the proper operation of the GSC under non-ideal grid conditions (voltage unbalance, harmonic distortion, etc), advanced and non-complex current controllers are needed to inject with accuracy and fast dynamic response asymmetrical currents involving selected components for harmonic compensation [5-8]. Among the existing control techniques, the multiple proportional resonant compensators (PR) were utilized in the (α,β) stationary reference frame with resonant frequencies tuned at the fundamental frequency and a group of harmonic components [6]. The performance of PR compensators depends on the grid frequency estimation, performed by a frequency-locked loop system (FLL) [5]. On the other hand, proportional integral (PI) compensators have been implemented in multiple dq synchronous reference frames (MSRF) [7,8] to achieve an accurate tracking of current references (fundamental positive and negative sequences) and compensate low-order harmonic components in the grid currents. The appropriate operation of PI compensators in MSRF needs an accurate transformation of all state variables (current, voltage) from the abc to the dq reference frames. A key element of the abc to dq reference frames transformation is the estimation of the grid voltage phase angle at the point of common coupling (PCC), performed by a phase-locked loop (PLL) system. The latter should provide a fast and an oscillation-free estimation of the grid voltage phase angle under normal and abnormal grid conditions [5]. This will enable accurate reference frames' transformations. Moreover, reference currents could be generated without low-frequency ripple due to harmonic distortion [1]. Accordingly, advanced PLL based synchronization systems are needed for the proper operation of GSC including dedicated harmonic current compensators and operating under harmonic distortion of the grid voltages [9].

Several PLL schemes have been developed in the recent research literature to achieve synchronization with the grid voltages under normal and abnormal grid conditions. The synchronous-reference frame PLL (SRF-PLL) [10] is the basic algorithm that has been widely utilized owing to its simple implementation and fast dynamic response. However, its performance deteriorates dramatically under harmonic distortion or unbalance of grid voltages. A possible solution to

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M. Mellouli and J. Ben Hadj Slama are with the Research Laboratory LATIS, ENISO, University of Sousse, P.O 264 Erriadh City 4023 Sousse, Tunisia. (e-mail: mohamedellmellouli@gmail.com; bhslama@yahoo.fr).

M. Hamouda is with the Research Laboratory LATIS, ENISO, University of Sousse, P.O 264 Erriadh City 4023 Sousse, Tunisia and Canada Research Chair in Energy Conversion and Power Electronics, ETS de Montreal, Quebec H3C1K3, Canada (e-mail: mahmoudhamouda@yahoo.fr)

K. Al-Haddad is with Canada Research Chair in Energy Conversion and Power Electronics, ETS de Montreal, Quebec H3C1K3, Canada (e-mail: kamal.al-haddad@etsmtl.ca)

tackle this limitation is to add filtering stages with the aim to mitigate the effect of harmonic components of the grid voltage. For instance, a simple low-pass filter (LPF) can be incorporated in the SRF-PLL control loop to enhance its steady state performance in terms of robustness and accuracy. However, the added filter worsens the dynamic behavior of the PLL, leading to a higher settling time response. Notice that the performance of PLL systems can be enhanced through the following two main steps:

1) The design of an appropriate LPF, able to remove the harmonic components without affecting the fundamental component waveform amplitude and phase angle. Typically, ideal LPFs such the moving average filter (MAF) [11] or the delayed signal cancellation (DSC) [3,12] are preferred to completely reject all harmonic contents in highly distorted grid voltages and not only attenuate them.

2) Optimization of the dynamic performance of the whole PLL system. In this framework, several techniques have been developed to achieve this goal. For instance, one can cite the phase-lead compensator (PLC) [13], filters' combination, the reduced PLL control type that uses a simple gain based controller [14], etc.

In the recent literature, the moving average filter PLL (MAF-PLL) based on the incorporation of a first-order MAF filter in the control loop of the SRF-PLL has received considerable attention. This is because of its attractive performance such as simple implementation, low computational burden, higher rejection rate of harmonics, and better accuracy [11]. However, additional efforts are still needed to improve its dynamic performance that it is affected by the MAF's phase delay. In [13], the authors added a PLC in the control loop of the MAF-PLL to compensate for the phase delay caused by the MAF filter. The aforementioned algorithms are classified as type-2 PLLs since PI controllers are used in the control loop. Though the integral term provides an accurate steady state response, however it increases the settling time and worsens the stability margin [11]. In [14], the authors proposed to use a simple gain based controller with the aim to overcome the sluggish effect of the integral term in the PI controller. Though this algorithm referred to as quasi-type-l PLL (QT1-PLL) provides a faster dynamic response, but the removal of the integral term worsens the disturbance rejection capability under grid frequency drift condition.

Based on recent review papers which deeply investigated and evaluated the performance of MAF based PLL algorithms [15,16], most of type-2 PLLs provide a non-satisfactory transient response due to the use of a MAF and the integral term of the PI controller. Moreover, it has been widely approved that the QT1-PLL is the best MAF-PLL technique in terms of dynamic performance and disturbance rejection capability. However, the performance of the QT1-PLL is still poor in case of frequency deviation under harmonically distorted grid voltages. This weakness is due to the non-frequency adaptive behavior of the MAF. Therefore, an adaptive QT1-PLL algorithm has been developed in [14] to adjust in real-time the MAF's window width to the estimated grid frequency. This proposed solution suffers in turn from the following two drawbacks:

- A large memory space is needed to store the filter's coefficients.
- The computational cost is more important and considerably increases under a frequent change of the fractional delay.

This paper proposes a novel synchronization algorithm with the aim to enhance the performance of the conventional QT1-PLL under harmonic distortion and unbalance of the grid voltages with frequency drift. It is based on a hybrid filtering technique that makes an appropriate combination of an in-loop third-order MAF with a reduced window width and a prefiltering stage. The latter consists of a simplified second-order fast convergence delayed signal cancellation (FDSC). The used filters (in-loop and prefiltering stage) do not need any adaptive algorithm and provide a high rejection capability of non-triplen odd-harmonics components and the fundamental frequency negative sequence (FFNS) even under frequency drift. The proposed PLL is named third-order MAF based QT1-PLL (TQT1-PLL) since it uses an in-loop third-order MAF. Its performances are tested with numerical simulations and real-time implementation on a digital signal processor (DSP). The obtained results confirm its ability to estimate the grid phase even under harmonic distortion and unbalance of the grid voltage with frequency deviation from its nominal value.

The paper is therefore organized as follows. A brief overview of the conventional and adaptive QT1-PLL algorithms is provided in section II. The proposed TQT1-PLL technique is described in detail in Section III. Stability analysis based on a small-signal model of the TQT1-PLL is performed in section IV. Numerical simulations in frequency and time domains as well as real-time implementation results are given and discussed in section V. Finally, some concluding remarks are given in section VI.

II. Overview of the Conventional and Adaptive QT1-PLL Algorithms

A. First-order MAF and its limitation against disturbed grid voltages

The MAF is a kind of finite-impulse response low–pass filter used to extract the fundamental components of the grid voltages. Equations (1) and (2), provide the expressions of the MAF filter's transfer function, gain, and phase angle.

$$MAF(s) = \frac{1 - e^{-T_\omega s}}{T_\omega s} \tag{1}$$

$$G_{MAF}(j\omega) = \left| \frac{\sin(\omega T_\omega / 2)}{(\omega T_\omega / 2)} \right| \angle - \omega T_\omega / 2 \tag{2}$$

T_ω is the time needed to reach the steady-state condition, referred to as window width of the filter.

Unfortunately, the attenuation level of the first-order MAF is not satisfactory under highly distorted grid voltages with non-triplen odd-harmonics and the fundamental frequency negative sequence (FFNS) (see Table I [17]). Indeed, in a dq rotating reference frame synchronized with the fundamental frequency positive sequence (FFPS) of the grid voltage, the latter (FFPS) is transformed into a DC term whereas the non-triplen odd harmonics and the FFNS become even order components. Therefore, to remove all dominant harmonic components and the FFNS, the MAF window width shall be equal to half the grid fundamental period. However, if the

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fundamental grid frequency deviates from its nominal value, the FFNS and all dominant harmonics will fall on the MAF's side lobes, implying they are not entirely rejected by the first-order MAF as illustrated in Fig. 1.

B. Conventional and adaptive QT1-PLL algorithms

Fig. 2 represents the block diagram of the basic QT1-PLL algorithm that uses a simple proportional controller (K_p) in the feed-forward control path. However, the absence of an integral compensator deteriorates the PLL performance in terms of frequency drift tracking. This limitation has been overcome in [14] by adding the signal feeding the input of the compensator block to the estimated value of the phase angle as shown in Fig. 2. Therefore, this synchronization technique can be considered as a type-1 PLL from the point of view structure, but it becomes a type-2 PLL from the control viewpoint [14]. Notice that a type-1(2) PLL has 1(2) pole(s) at the origin in the open-loop transfer function. This hybrid structure also referred to as QT1-PLL provides a faster transient response, good filtering capability and a good stability margin. However, its performance is still poor in case of frequency deviation under harmonically distorted grid voltages. This weakness is due to the non-capability of the conventional MAF to entirely remove the FFNS and all dominant harmonics in case of frequency variation from its nominal value.

The existing solutions to this problem proposed in the recent literature are based on updating the MAF's window width (T_ω) with the instantaneous grid fundamental frequency i.e. make T_ω adaptive with the instantaneous grid frequency. Equation (3) and Fig. 3 show the transfer function of the MAF filter in the z domain and its discrete-time implementation respectively.

TABLE I
VOLTAGE COMPONENTS AND THEIR ASSOCIATED PHASE SEQUENCES

Voltage components	Phase sequence order in abc frame	Phase sequence order in d-q frame
FFPS (fundamental)	1^+	DC
FFNS (unbalanced)	1^-	2^-
Non-triplen odd (+) sequence	$h = (6k+1)^+$	$h = (6k)^+$
Non-triplen odd (-) sequence	$h = (6k-1)^-$	$h = (6k)^-$

With k is a non-zero positive integer

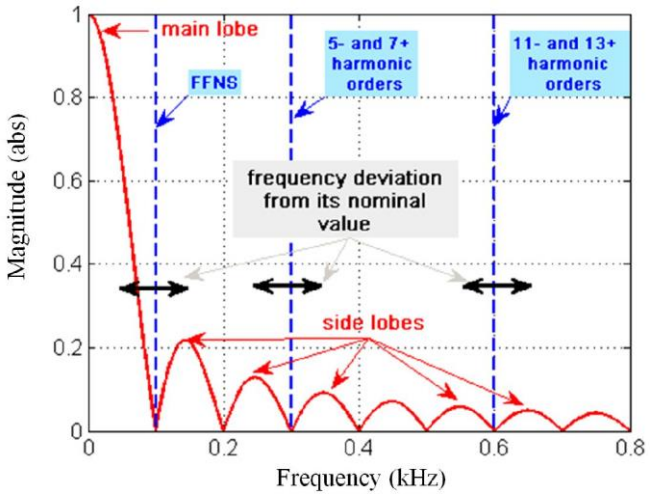

Fig. 1. MAF's gain versus the frequency obtained with $T_\omega = 0.01$s

$$MAF(N) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \tag{3}$$

Where N is an integer such that $T_\omega = N\ T_s$ and T_s is the sampling period of the discrete-time controller. Therefore, making T_ω adaptive with the grid frequency is possible through the following two solutions:

- The real-time adjustment of the sampling period of the PLL algorithm (T_s), which makes the implementation of the overall control algorithm of the GSC more complex. Therefore, this solution is not preferred.
- The real-time adjustment of the samples' number N according to the grid frequency deviation. Many solutions have already been proposed to find the opportune value of N. Some of them use a variable integer number N_i by rounding the quantity T_ω / T_s to the nearest integer (simple rounding, rounding up, etc). Many other solutions are based on linear interpolation which allows replacing N by a variable fractional delay (VFD) namely N_f [18]. Fig. 4 illustrates the non-adaptive and adaptive MAF gains under frequency variation from 290 to 310 Hz. It is clear that the adaptive technique based on linear interpolation provides the best performance since the filter's gain is the closest to zero. Fig. 5 shows the implementation in the discrete domain of the adaptive MAF using VFD. Unfortunately, the real-time implementation of the scheme shown in Fig. 5 is more complex as compared to non-adaptive MAF using a constant integer delay (N). Moreover, it needs a higher computational effort and a larger memory to store the filter's coefficients when N_f changes frequently.

III. PROPOSED TQT1-PLL

The proposed TQT1-PLL algorithm uses a hybrid filtering technique and does not need any adaptive block as shown in Fig. 6. The conventional in-loop MAF filter is replaced by a third-order MAF filter to enhance the PLL robustness against frequency deviation without adding any adaptive algorithm. Moreover, an additional prefiltering stage is utilized to eliminate the FFNS component. The two filtering stages are the main novelty of the proposed TQT1-PLL and will be explained in detail in the remainder of this section.

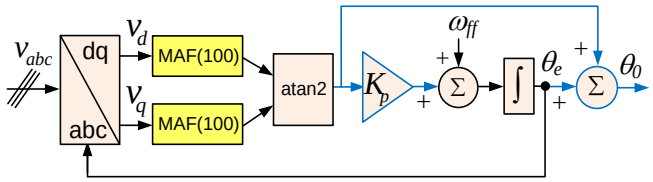

Fig. 2. Block diagram of QT1-PLL

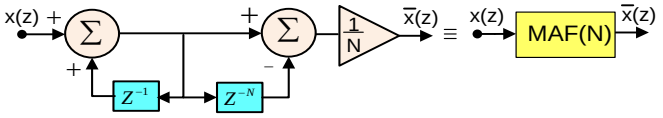

Fig. 3. Discrete-time implementation of the non-adaptive MAF where N is a constant integer. $x(z)$ and $\bar{x}(z)$ are the discrete input and output signals

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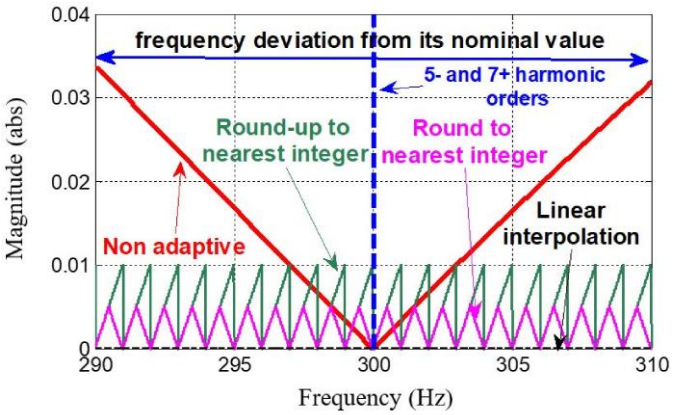

Fig. 4. Gains of adaptive and non-adaptive MAF under frequency variation

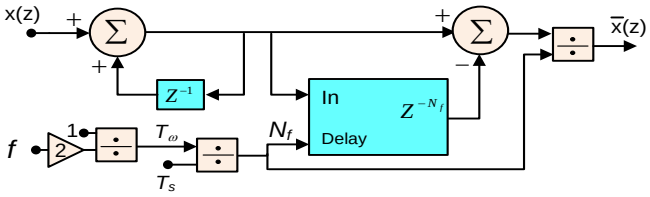

Fig. 5. Realization of an adaptive MAF in z-domain using a VFD (N_f).

A. In-loop third-order MAF

One possible solution to make the QT1-PLL insensitive to frequency deviation is to build a filter with a gain close to zero in the region of dominant harmonic frequencies. In other words, we shall reduce as possible the amplitude of the side lobes so as to keep the MAF's gain close to zero. This objective can be reached by increasing the filter's order while maintaining a small delay response. For this purpose, a third-order MAF filter is constructed by using three conventional MAF filters connected in cascade as shown in Fig. 6. Moreover, each MAF filter's window is divided by three to maintain the same filter's delay response as the conventional MAF. Fig. 7 depicts the gains of the conventional MAF and the proposed third-order MAF versus the frequency. One can clearly observe that all side lobes of the conventional MAF are almost removed. This will obviously improve the harmonic rejection capability under frequency deviation since the gain in the neighborhood of the dominant harmonics (regions within the two large circles) are quite equal to zero. However, this filter is not able to remove the FFNS (unbalanced component) since the gain at the corresponding frequency (region within the small circle) is not close to zero. The solution to this problem will be addressed in section C.

B. Implementation of the third-order MAF

Define f_{ff} as the grid fundamental frequency in ideal operation conditions. Therefore the value of the MAF window width is T_ω = 0.01 s for f_{ff} = 50 Hz. For a sampling period of the discrete-time controller T_s equal to 10^{-4} s, the number of samples N needed to implement the conventional MAF according to (3) is an integer and equal to 100 ($N = T_\omega/T_s$). However, in case of the proposed third-order filter, N becomes non-integer (100/3). In this section, a simple method is proposed to implement a discrete MAF filter with non-integer number of samples.

Equation (4) shows the transfer function of the MAF filter in the z domain with a number of samples N = 33 and N = 34.

$$\begin{cases} MAF(33) = \dfrac{1}{33}\dfrac{1-z^{-33}}{1-z^{-1}} \\ MAF(34) = \dfrac{1}{34}\dfrac{1-z^{-34}}{1-z^{-1}} \end{cases} \tag{4}$$

Since the MAF is an averaging filter, therefore, the average of samples computed by this filter for N = 100/3 can be deduced from the two averages quantities computed with 33 and 34 samples as shown in (5) hereafter. Equation (5) allows therefore the implementation of the discrete-time MAF with a number of samples equal to 100/3 and without using any factional delay estimation block as depicted in Fig. 8.

$$\begin{aligned} MAF\left(\frac{100}{3}\right) &= MAF(33) + \frac{MAF(34) - MAF(33)}{3} \\ &= \frac{2MAF(33) + MAF(34)}{3} \end{aligned} \tag{5}$$

Fig. 9 shows a zoom of the proposed third-order MAF (100/3) gain in the frequency range [290, 310] Hz. This corresponds to ± 10 Hz variation of the 5th and 7th order harmonic frequencies in the dq synchronous reference frame caused by fundamental grid frequency change from 48.33 Hz to 51.66 Hz. As can be seen, the filter's gain remains less than 4 10^{-5} even for this variation of grid frequency. This confirms the performance of the proposed filter even in case of harmonically distorted grid voltage with frequency jump. Table II hereafter summarizes the performance of the proposed third-order MAF as compared to the conventional MAF. The third-order MAF provides a better harmonic rejection capability under frequency jump while keeping the same filter's delay. However, its performance remains poor in terms FFNS (unbalanced component) rejection.

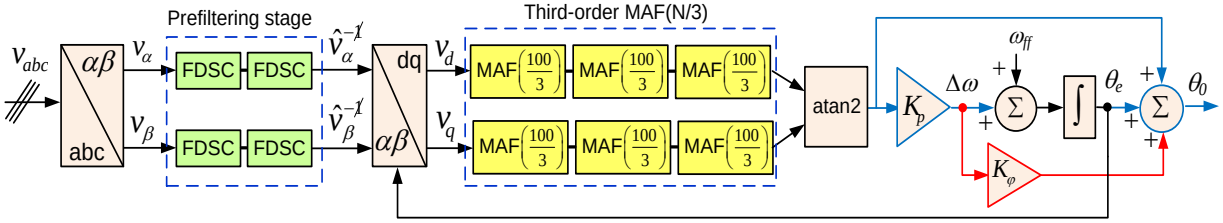

Fig. 6. Simplified block diagram of the proposed TQT1-PLL

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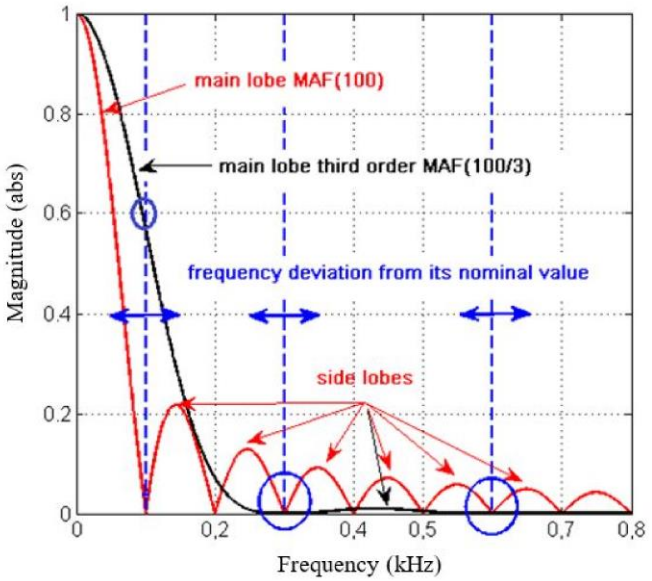

Fig. 7. Gains of the MAF (N) and third-order MAF (N/3) versus the frequency

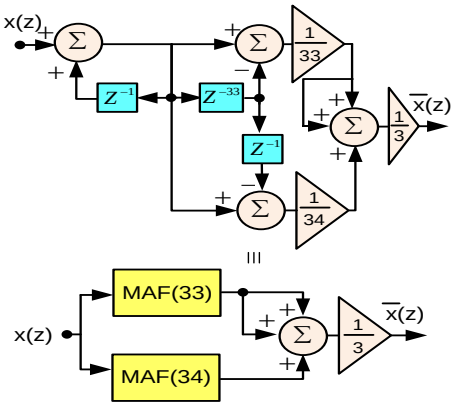

Fig. 8. Discrete-time implementation of the MAF (N/3) with N=100.

TABLE II
PERFORMANCE OF CONVENTIONAL MAF (N) VERSUS THIRD-ORDER MAF (N/3)

	Third-order MAF (N/3)	Conventional MAF (N)
Number of samples	3* (N/3) =N	N
Filter's Delay (s)	$T_\omega = 3*(T_s/3N) = T_s/N$	$T_\omega = T_s/N$
HRC* without frequency jump	Good except the FFNS	Good
HRC* under frequency jump	Good except the FFNS	Poor

*HRC: Harmonic rejection capability

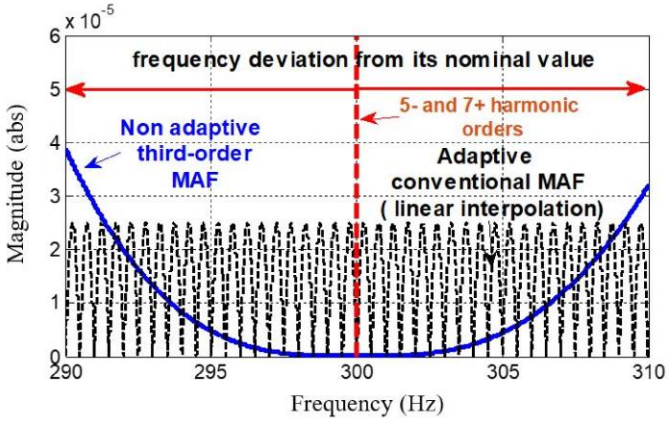

Fig. 9. Gains of adaptive and the proposed non-adaptive MAF under frequency variation from its nominal value

C. FFNS elimination using a second-order FDSC based prefiltering stage

Since the proposed third-order MAF (N/3) filter is not able to remove the FFNS, a prefiltering stage is therefore used to eliminate this component as already shown in Fig. 6. Notice that many filtering techniques for removing the FFNS already exist in the recent literature such as the DSC, resonant filter [19], dual second-order generalized integrator (DSOGI) [20], multiple reference frames (MRF) [7,21],…etc. Among them, the first-order FDSC has been found as the best technique in terms of convergence rapidity. Indeed, it needs the lowest time delay to start the extraction of the FFPS and FFNS. This section provides a simplified version of the FDSC proposed in [22].

According to [22], the αβ components of the grid voltage without the FFNS ($\hat{v}_\alpha^{-1}$ and $\hat{v}_\beta^{-1}$) can be estimated using the instantaneous and delayed signals of the entire grid voltage and specific trigonometric coefficients as given in (6). v_α and v_β are the instantaneous αβ components of the measured grid voltages. θ_d is a delay angle that depends on the number of delayed samples N_d such that $\theta_d = 2\pi f N_d T_s$. f is the grid fundamental frequency. $v_\alpha^{(\theta_d)}$ and $v_\beta^{(\theta_d)}$ are the αβ components of the grid voltages delayed by N_d samples. They are computed as illustrated in (7), where θ the instantaneous grid voltage phase.

$$\begin{cases} v_\alpha^{(\theta_d)} = v_\alpha z^{-N_d} = v_\alpha\left(\theta-\theta_d\right) \\ v_\beta^{(\theta_d)} = v_\beta z^{-N_d} = v_\beta\left(\theta-\theta_d\right) \end{cases} \tag{7}$$

$$\begin{cases} \hat{v}_\alpha^{-1} = \dfrac{v_\alpha - v_\alpha^{(\theta_d)}\cos\theta_d^{ff} - v_\beta^{(\theta_d)}\sin\theta_d^{ff} - \left(v_\alpha - v_\alpha^{(\theta_d)}\cos\theta_d^{ff} - v_\beta^{(\theta_d)}\sin\theta_d^{ff}\right)\cos 2\theta_d^{ff} + \left(v_\beta - v_\beta^{(\theta_d)}\cos\theta_d^{ff} + v_\alpha^{(\theta_d)}\sin\theta_d^{ff}\right)\sin 2\theta_d^{ff}}{2\left(1-\cos 2\theta_d^{ff}\right)} \\ \hat{v}_\beta^{-1} = \dfrac{v_\beta - v_\beta^{(\theta_d)}\cos\theta_d^{ff} + v_\alpha^{(\theta_d)}\sin\theta_d^{ff} - \left(v_\beta - v_\beta^{(\theta_d)}\cos\theta_d^{ff} + v_\alpha^{(\theta_d)}\sin\theta_d^{ff}\right)\cos 2\theta_d^{ff} - \left(v_\alpha - v_\alpha^{(\theta_d)}\cos\theta_d^{ff} - v_\beta^{(\theta_d)}\sin\theta_d^{ff}\right)\sin 2\theta_d^{ff}}{2\left(1-\cos 2\theta_d^{ff}\right)} \end{cases} \tag{6}$$

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As can be seen, (6) is very complex and needs many arithmetic operations for its real-time implementation. Hence, by doing some mathematical arrangements and simplifications, we can obtain a more simplified expression of $\hat{v}_\alpha^{-1}$ and $\hat{v}_\beta^{-1}$ as shown in (8) where θ_d^{ff} is the value of θ_d in ideal grid frequency condition ($f = f_{ff}$). Equation (8) is therefore a simplified version of the first-order FDSC that can be implemented in real-time using less arithmetic operations.

$$\begin{cases} \hat{v}_\alpha^{-1} = \dfrac{1}{2}\left[v_\alpha + v_\beta \dfrac{1}{\tan\theta_d^{ff}} \right] - \dfrac{1}{2}\dfrac{1}{\sin\theta_d^{ff}} v_\beta^{(\theta_d)} \\ \hat{v}_\beta^{-1} = \dfrac{1}{2}\left[v_\beta - v_\alpha \dfrac{1}{\tan\theta_d^{ff}} \right] + \dfrac{1}{2}\dfrac{1}{\sin\theta_d^{ff}} v_\alpha^{(\theta_d)} \end{cases} \quad (8)$$

The gain and phase angle of the proposed simplified first-order FDSC for each h[th] order harmonic component are computed as shown in (9)

$$G_{FDSC}(h) = \left| \frac{\sin\left((\theta_d^{ff} + h\theta_d)/2\right)}{\sin\theta_d^{ff}} \right| \angle -(h\theta_d - \theta_d^{ff})/2 \quad (9)$$

Define now ε_{θ_d} as a phase angle deviation due to frequency deviation ($\varepsilon_f = f - f_{ff}$) from its nominal value. i.e. $\varepsilon_{\theta_d} = \theta_d - \theta_d^{ff} = 2\pi N_d \varepsilon_f T_s$. Therefore, the gain and phase angles in (9) can be expressed in terms of the frequency deviation such that:

$$\begin{cases} G_{FDSC}(h) = \left| \dfrac{\sin\left(\left((h+1)\theta_d^{ff} + h\varepsilon_{\theta_d}\right)/2\right)}{\sin\theta_d^{ff}} \right| \\ \angle -\left((h-1)\theta_d^{ff} + h\varepsilon_{\theta_d}\right)/2 \end{cases} \quad (10)$$

Fig. 10 illustrates the first-order FDSC's gain versus the harmonic order obtained with two values of N_d (5 and 10). As can be seen, with ideal grid frequency operation ($\varepsilon_f = 0$ i.e. $\varepsilon_{\theta_d} = 0$), the FDSC is able of completely removing the FFNS component with any chosen value of N_d. However, a larger value of N_d is suitable since it provides less harmonic amplification but it affects in turn the dynamic response of the PLL. In this paper N_d = 10 is chosen to make a compromise between mitigation of harmonic amplification and dynamic response. Moreover, one can observe that in case of frequency deviation, the first-order FDSC gain becomes non-zero at the frequency of the FFNS component. To improve the robustness against frequency jump, this paper proposes to use a second-order FDSC that is obtained by duplicating twice the first-order FDSC operator as shown in Fig. 6. The gain of the proposed second-order FDSC is shown in Fig. 11. Fig. 12 illustrates a zoom in of Fig. 10 and Fig. 11 for N_d = 10. It is clear that the waveform of the second-order filter's gain becomes smoother in the neighborhood of the FFNS implying that it provides a better filtering of signals with frequency located around the negative value of the fundamental frequency.

Compared to the conventional QT1-PLL, the following two main modifications are proposed to construct the newly proposed TQT1-PLL

- A third-order MAF (N/3) is used instead of a conventional MAF (N). This high-order filter was built with the aim to enhance the harmonics rejection capability of the PLL.
- A second-order FDSC based prefiltering stage, less sensitive to frequency jump is used with the aim to reject the FFNS.

This will inherently enhance the performance of the proposed TQT1-PLL under harmonic distortion and unbalance of the grid voltage with frequency jump as will be discussed in the simulation and real-time implementation section.

D. DC-offset rejection

The presence of DC offset in the signals feeding the PLL's input is a major problem since it may give rise to fundamental frequency ripple in the estimated phase and frequency as well as DC-current injection by the GSC [23,24]. The existing techniques for DC-offset rejection usually use filtering stages that can be classified into two main categories depending on their position [23]:

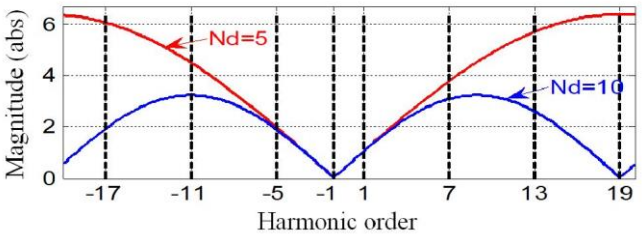

Fig. 10. First-order FDSC's gain versus harmonic order obtained with N_d =5 (red) and N_d =10 (blue)

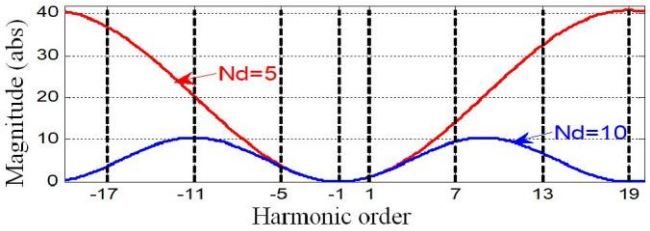

Fig. 11. Second-order FDSC's gain versus harmonic order obtained with N_d =5 (red) and N_d =10 (blue)

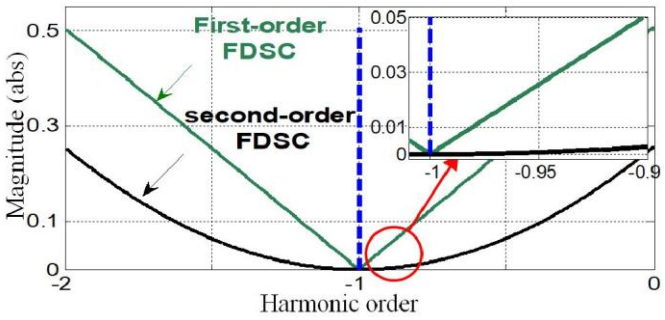

Fig. 12. Zoom in the two blue curves of Fig. 10 and Fig. 11 (N_d = 10) around the FFNS

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- In-loop filtering stages, implemented in the dq reference frame such as the dq delayed signal cancellation (dq-DSC) operator [23], the modified delayed signal cancellation operator (MDSC) [25], and the dq- second-order complex coefficient filter (dq-DSOCCF) [24]. Notice that in-loop filtering stages worsen the dynamic behavior of the PLL.
- Prefiltering stages usually implemented in a stationary reference frame. In [26] a band-pass filter (BPF) is inserted in the input terminals of the PLL to reject the DC offset. However, the BPF slows-down the dynamic response of the PLL and may cause a phase-shift under grid frequency variation. The αβ-DSC operator is used in [27]. This filter is also sensitive to grid frequency deviation and needs an additional phase error compensator (PEC).

The second-order FDSC presented in the former subsection can decrease the amplitude of the DC offset to approximately 25% of its initial value as can be seen in Fig. 12. In this subsection, we introduce a solution to enable the complete rejection of the DC offset. This paragraph only explains analytically the proposed solution i.e. the latter will not be considered in the remaining of the paper. The proposal consists of an additional filter placed in cascade with the second-order FDSC as shown in Fig. 13. The filter consists of two identical blocks namely αβ-DC-rejection filter (αβ-DC-R) as it rejects the DC offset from the grid voltages in the αβ reference frame.

The αβ components of the grid voltage without DC offset namely ($\hat{v}_\alpha^{\emptyset}$, $\hat{v}_\beta^{\emptyset}$) are estimated from $\hat{v}_\alpha^{-1}$ and $\hat{v}_\beta^{-1}$ as shown in (11). $v_\alpha^{-1}(\theta_d^{'})$ and $v_\beta^{-1}(\theta_d^{'})$ are the inputs ($\hat{v}_\alpha^{-1}$ and $\hat{v}_\beta^{-1}$) delayed by a phase angle $\theta_d^{'}$. The latter depends on the number of delayed samples $N_d^{'}$ such that $\theta_d^{'} = 2\pi f N_d^{'} T_s$. f is the grid voltage fundamental frequency. T_s is the sampling period of the controller. $\theta_d^{'ff}$ is the value of $\theta_d^{'}$ in ideal grid frequency condition ($f = f_{ff}$). The relationship between ($\hat{v}_\alpha^{-1}$, $\hat{v}_\beta^{-1}$) and ($v_\alpha^{-1}(\theta_d^{'})$, $v_\beta^{-1}(\theta_d^{'})$) are expressed similarly as done in (7).

$$\begin{cases} v_\alpha^{\emptyset} = \dfrac{v_\alpha^{-1} - v_\alpha^{-1}(\theta_d^{'})}{\sin\left(\theta_d^{'ff}/2\right)} \\ v_\beta^{\emptyset} = \dfrac{v_\beta^{-1} - v_\beta^{-1}(\theta_d^{'})}{\sin\left(\theta_d^{'ff}/2\right)} \end{cases} \tag{11}$$

By doing some mathematical developments, the gain and phase angle of the proposed αβ-DC-R filter for each hth order harmonic component are computed as shown in (12) hereafter:

$$G_{\alpha\beta-DC-R}(h) = \left|\frac{\sin\left(h\theta_d^{'}/2\right)}{\sin\left(\theta_d^{'ff}/2\right)}\right| \angle \frac{\pi}{2} - \frac{h\theta_d^{'}}{2} \tag{12}$$

It is clear that the filter with a transfer function given in (12) is able to remove the DC offset (h = 0). To better enhance the performance of this filter by adding the rejection capability of even harmonics, a second αβ-DC-R filter and a multiplication bloc (-1) are added in cascade with the first αβ-DC-R filter as illustrated in Fig. 13. Accordingly, the gain and phase angle of equivalent second-order αβ-DC-R (2nd-αβ-DC-R) filter are derived as follows:

$$G_{2^{nd}-\alpha\beta\,DC-R}(h) = \left|\frac{\sin\left(h\theta_d^{'}/2\right)}{\sin\left(\theta_d^{'ff}/2\right)}\right|^2 \angle -h\theta_d^{'} \tag{13}$$

Fig. 14 shows the gain of the proposed 2nd-αβ-DC-R versus the harmonic order obtained with $N_d^{'}$ = 100. As can be seen, the gain at the DC (0 Hz) and all even harmonic components is equal to zero. Fig. 15a displays the gain of the prefiltering stage obtained with only a second-order FDSC (blue curve) and after adding the 2nd-αβ-DC-R filter. As can be seen, the gain with the added 2nd-αβ-DC-R filter is always inferior or equal to the one of the second-order FDSC i.e. undesirable amplification of harmonics is avoided. Fig. 15b shows that at the DC frequency (0 Hz) the gain of the proposed solution (green curve) is equal to zero implying that the DC offset is completely removed at (0 Hz). Moreover, from the DC (0 Hz) to the second-order negative harmonic sequence, the gain is lower than 0.035, implying that the FFNS component will be removed whatever the variation of the grid frequency. Furthermore, Fig. 15c emphasizes that the added 2nd-αβ-DC-R filter has no negative impact on the gain of the FFPS, which remains equal to 1. Notice that by adding the 2nd-αβ-DC-R filter in the prefilling stage, the value of the compensation gain (K_φ) of the PLL should be updated as follows:

$$K_\varphi = \left(N_d + N_d^{'}\right) T_s \tag{14}$$

Where N_d and $N_d^{'}$ are the number of delayed samples of the second-order FDSC and the 2nd-αβ-DC-R filter respectively.

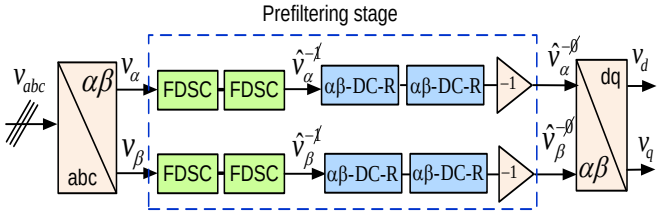

Fig. 13. 2nd-αβ-DC-R filter cascaded with the second-order FDSC in the prefiltering stage

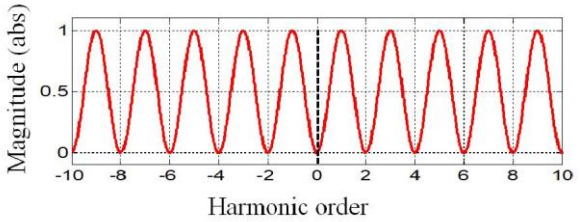

Fig. 14. 2nd- αβ-DC-R filter's gain versus harmonic order obtained with N'_d = 100

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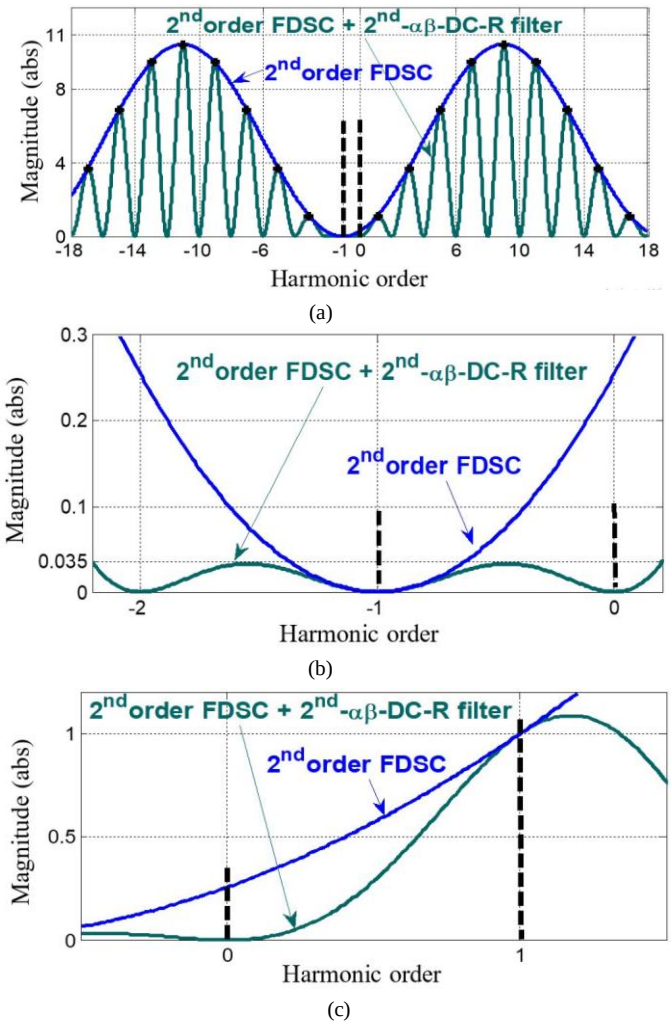

Fig. 15. (a) Gain of the prefiltering stage versus harmonic order (blue) second-order FDSC (green) second-order FDSC cascaded with the 2nd-αβ-DC-R filter with $N_d^{'}$ = 100 (b) zoom in of waveforms around the FFNS and DC (0 Hz) components (c) zoom in of waveforms around the FFPS and DC (0 Hz) components

IV. Small-Signal Modeling and Stability Analysis

In this section, the stability of TQT1-PLL is analyzed based on a small-signal model. The stability of the whole power conversion system (PLL and grid-connected converter) [28] is beyond the objective of this paper. Fig. 16 shows a small-signal model of the TQT1-PLL derived from the block diagram depicted in Fig. 6 (without the DC-offset rejection filter). The model is obtained by applying and combining the simplification procedures used for PLLs' modeling with in-loop and prefiltering stages [29,30]. After some rearrangements, an equivalent standard form of the small-signal model suitable for the stability analysis is obtained as depicted in Fig. 17.

To simplify the stability analysis of the derived equivalent model, the continuous time delay block $e^{-T_\omega s}$ appearing in (1) is linearized using the first-order Padé approximation given in (15)

$$e^{-x} \approx \frac{1-x/2}{1+x/2} \quad \text{and} \quad x = T_\omega s \tag{15}$$

The equivalent open-loop transfer function of TQT1-PLL namely $G_{OL\text{-}TQT1}(s)$ is therefore obtained as given in (16).

$$G_{OL-TQT1}(s) \approx \left[\frac{8}{T_\omega s^2}\left(\frac{s\left(1+K_pK_\varphi\right)+K_p}{\left(T_\omega s\right)^2+6\left(T_\omega s\right)+12}\right)\right] \tag{16}$$

It is worth mentioning that the equivalent small-signal model given in (16) is developed with the assumption of the phase error between the locked-phase (phase computed by the PLL) and the one of the FFPS of the grid voltage is small. Notice that under unbalanced grid voltages, a large amplitude of the negative sequence component causes a time periodic variation in the trajectory of the phase error [31, 32] due to the frequency-coupling dynamics and making the system linear time periodic (LTP). The proposed TQT1-PLL uses a prefiltering stage (in the outer loop) to eliminate the FFNS in the grid voltage i.e. the signal fed to the input of the loop in Fig. 17 is theoretically free of 2ω ripple ($\omega = 2\pi f$). Therefore, the analytical expression of the open-loop transfer function given in (16) could be considered linear time invariant (LTI) since the assumption of a small phase error is still valid.

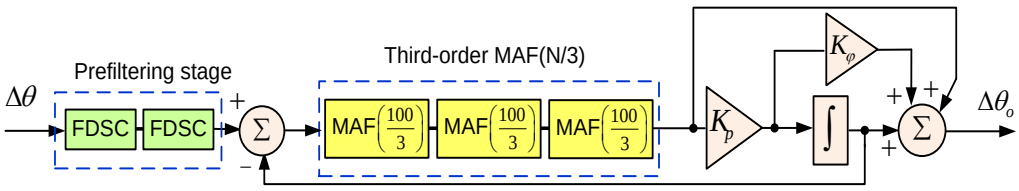

Fig. 16. Small signal model of TQT1-PLL

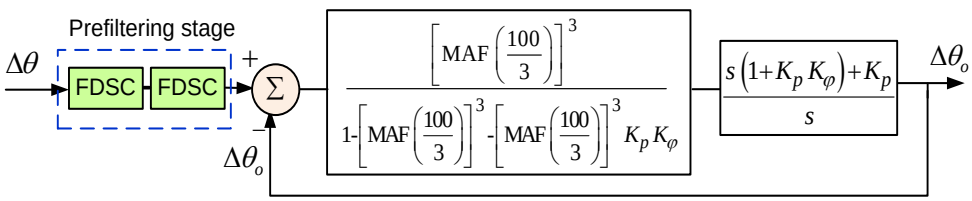

Fig. 17. Equivalent standard form of the small-signal model of TQT1-PLL

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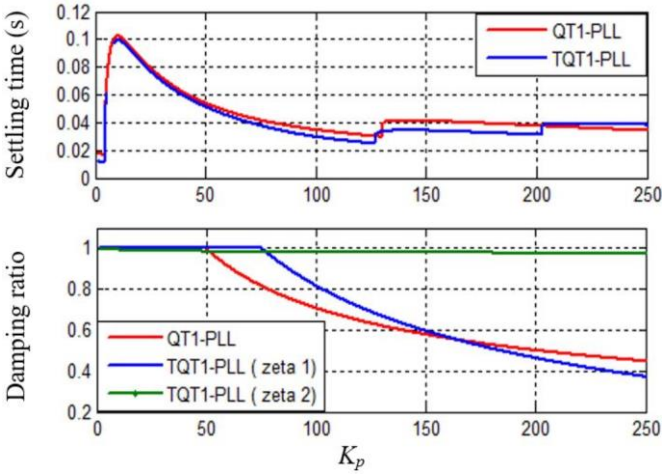
Figs.18a-b show the phase and gain margins versus the proportional gain K_p of the proposed TQT1-PLL and QT1-PLL. The open-loop transfer function namely $G_{OL\text{-}QT1}(s)$ of QT1-PLL is shown in (17) as given in [14].

$$G_{OL-QT1}(s) \approx \left[\frac{2}{T_\omega} \left(\frac{s+K_p}{s^2} \right) \right] \quad (17)$$

Referring to [33], the system is stable if both, its phase margin (*PM*) and gain margin (*GM*) of the open-loop transfer function are positive. Moreover, *PM* should be greater than *GM* (Bode criterion). However, to achieve a robust stability, the appropriate values of *PM* and *GM* should be limited within the range 30-60° and 2-10 dB respectively. Fig. 18a, shows that the *PM* of both PLL systems (TQT1-PLL and QT1-PLL) could be effectively located within the range 30-60° with an appropriate choice of the proportional gain K_p. For instance, K_p of the proposed TQT1-PLL should be limited within the range 38-228. On the other hand, Fig. 18b shows that the *GM* of the TQT1-PLL remains within the appropriate band 2-10 dB for the determined operation range of K_p (38-228). However, the *GM* of the conventional QT1-PLL remains outside the band 2-10 dB. Fig. 18c displays the settling time (ST) and the damping factor (zeta) versus the proportional gain K_p obtained with QT1-PLL and TQT1-PLL. It is clear that for the suitable operation values of K_p, the ST of the TQT1-PLL is almost equal to or less than that of the conventional QT1-PLL. Therefore, and according to section III-B and the outcome of this paragraph, it can be concluded that the TQT1-PLL provides a better rejection of harmonic components under high variation of the grid frequency from its nominal value without any degradation of stability and transient performance as compared to the conventional QT1-PLL.

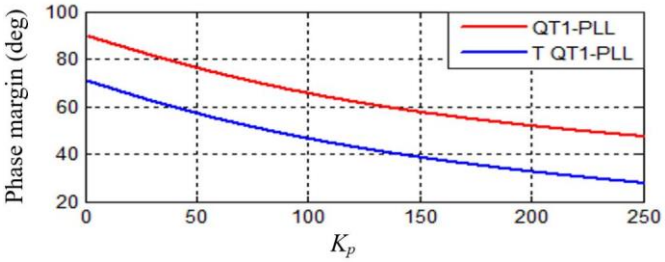
To emphasize this concluding remark, more accurate open-loop models of the TQT1-PLL and QT1-PLL are developed by increasing the Padé approximation order. Table III hereafter reports the expressions of (2,2) and (3,3) Padé approximation orders of the exponential term as well as the open-loop transfer functions of QT1-PLL and TQT1-PLL.



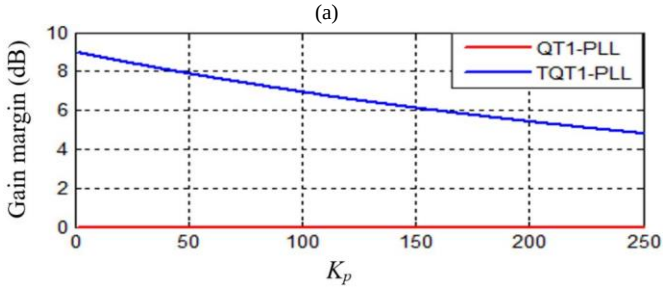
(c)

Fig. 18. (a) PM, (b) GM, (c) settling time and damping ratio (zeta) of TQT1-PLL and QT1-PLL versus proportional gain based on open-loop transfer function obtained using the first-order Padé approximation

Figs. 19a-b-c show the *PM*, *GM*, and settling time versus the proportional gain K_p of the approximated open-loop transfer functions of TQT1-PLL and QT1-PLL obtained with the Padé approximation order (3,3) (see (18) and (19) in Table III). The results of Fig. 19a clearly shows that the *PM* of both PLL systems (TQT1-PLL and QT1-PLL) could be located within the suitable range 30-60° through an appropriate choice of the proportional gain. Indeed, with the TQT1-PLL, K_p should be maintained within the range 12-146. As for the QT1-PLL, K_p needs to be limited within the range 37-175. On the other hand, Fig. 19b shows that the *GM* of the TQT1-PLL remains within the appropriate band 2-10 dB for the overall operation range of K_p (12-146). However, the *GM* of the conventional QT1-PLL is always located outside the suitable band 2-10 dB for the overall operation range of K_p (37-175). Fig. 19c shows once more that the ST of the TQT1-PLL is almost equal to or less than that of the conventional QT1-PLL. Therefore, the outcome obtained with the open-loop transfer function based on first-order Padé approximation is confirmed.



(a)



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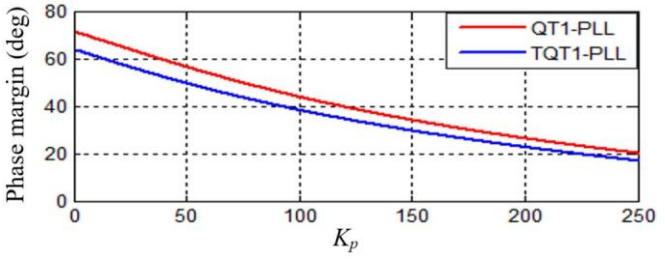
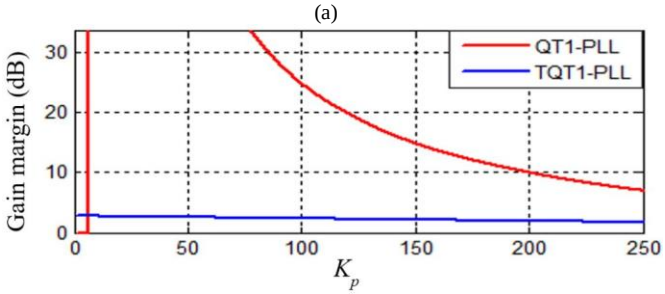


(a)



(b)

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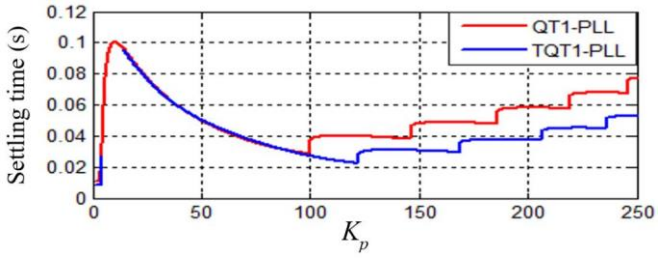
TABLE III
OPEN-LOOP TRANSFER FUNCTION OF QT1-PLL AND TQT1-PLL USING PADÉ APPROXIMATIONS (2,2) AND (3,3)

Padé-order →	(2,2)	(3,3)
e^{-x} ($x = T_\omega s$)	$\frac{1-x/2+x^2/12}{1+x/2+x^2/12}$	$\frac{1-x/2+x^2/10-x^3/120}{1+x/2+x^2/10+x^3/120}$
QT1-PLL open-loop transfer function	$\left[\frac{2}{T_\omega}\left(\frac{s+K_p}{s^2}\right)\right]\left(\frac{6}{T_\omega s+6}\right)$	$\left[\frac{2}{T_\omega}\left(\frac{s+K_p}{s^2}\right)\right]\left(\frac{(T_\omega s)^2+60}{(T_\omega s)^2+10(T_\omega s)+60}\right)$ (18)
TQT1-PLL open-loop transfer function	$\frac{12^3}{s}\left(\frac{s(1+K_pK_\varphi)+K_p}{((T_\omega s)^2+6(T_\omega s)+12)^3-12^3}\right)$	$\frac{1}{s}\left(\frac{(s(1+K_pK_\varphi)+K_p)(2(T_\omega s)^2+120)^3}{((T_\omega s)^3+12(T_\omega s)^2+60(T_\omega s)+120)^3-(2(T_\omega s)^2+120)^3}\right)$ (19)



(c)

Fig. 19. (a) *PM*, (b) *GM*, (c) settling time of TQT1-PLL and QT1-PLL versus proportional gain based on open-loop transfer function obtained using the Padé approximation order (3,3)

On the other hand, by inspecting again Fig. 18c and Fig. 19c, one can observe step changes of the ST for high values of K_p i.e. underdamped system (zeta is less than 1). For instance, a first step change of the TQT1-PLL's ST occurs with $K_p \approx 127$ (Fig. 18c). To properly justify this phenomenon, a first plot of the TQT1-PLL step response is performed with $K_p = 125$ (just before the first step change in Fig. 18c). Fig. 20 shows that the time response curve gets trapped within the 2% tolerance band after the first peak (maximum). The second peak (minimum) can be observed by the naked eye; however, it remains within the band. A second plot of the TQT1-PLL step response is performed with $K_p = 130$ (just after the first step change in Fig. 18c). The results of Fig. 20 illustrate that the second peak leaves the 2% band. Therefore, the step response curve gets trapped within the 2% tolerance band after this second peak leading to a step increase of ST despite the small variation of K_p. A similar phenomenon occurs for the second step change of ST with $K_p \approx 200$. Indeed, the step response obtained with $K_p = 195$ (just before the second step change) is always getting trapped within the 2% band after the second peak. The third peak (maximum) does not leave the band. As for the plot of the step response with $K_p = 205$ (just after the second step change), the third peak leaves the 2% band. The time response curve gets therefore trapped within the band after this third peak. Consequently, a new step increase in the value of ST occurs despite the small variation of the proportional gain. More analytical details and thorough explanation of discontinuities in the ST of LTI systems can be found in [34,35].

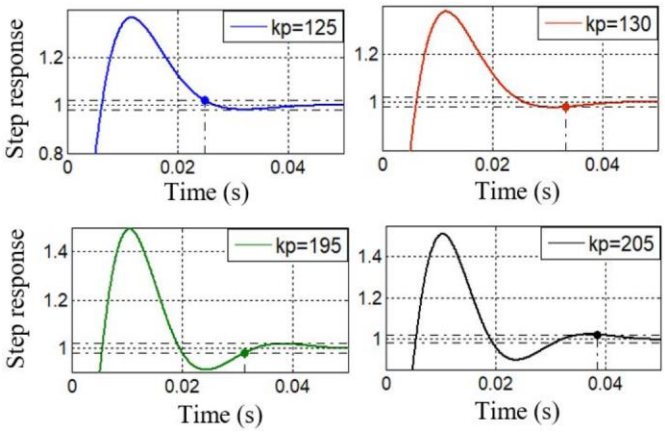


Fig. 20. Step response of TQT1-PLL obtained with four values of K_p (125, 130, 195, and 205)

V. COMPUTER SIMULATION AND DSP BASED REAL-TIME IMPLEMENTATION

A. Frequency domain verification of the analytical model

To verify the accuracy of the proposed small-signal model as given in (19) that describes the open-loop transfer function of the TQT1-PLL (obtained with Padé (3,3) approximation), frequency domain analysis is carried out based on numerical simulation results. A first TQT1-PLL block described by the schematic block diagram of Fig. 6 (without the prefiltering stage) is implemented in discrete time domain using Matlab/Simulink software as shown in Fig. 21. The third-order Adams-Bashforth method [36] is utilized for the digital implementation of the integrator to enhance the discretization accuracy and avoid algebraic loops. The PLL is fed by a positive-sequence voltage system. The grid voltage phase is emulated with an integrator that provides a periodic waveform varying from 0 to 2π rad. The negative-sequence component is not added since it is assumed to be perfectly removed by the prefiltering stage. The grid and controller's parameters are shown in Table IV. An input perturbation (phase perturbation) is added to the instantaneous waveform of the grid voltage phase feeding this PLL block. The phase perturbation is emulated with a small-amplitude multi-sine signal. Its peak amplitude with reference to the maximal value of the grid phase is equal to $0.1/2\pi$ in p.u. Its frequency is swept in the range [1, 200] Hz. From 1 to 9 Hz the variation step is equal to 1 Hz. From 10 to 200 Hz, it is set to 10 Hz. A second TQT1-PLL block is running in parallel with the first one without

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adding any input phase perturbation. The output small signal deviation from the steady state trajectory caused by the input perturbation is simply the difference between the two PLLs' outputs. A frequency scan is thereafter performed using the linear analysis tool of Simulink. This tool allows the possibility to generate the Bode diagram of the whole simulated system from the input perturbation source to the output measurement as depicted in the results of Fig. 22 (blue stars). On the other hand, the Bode plot of the closed-loop transfer function of the TQT1-PLL deduced from the open-loop transfer function (19) is depicted on the same Fig. 22 (red curve). As can be seen, the frequency scan results are consistent with the analytical small signal model, which confirms the accuracy of the proposed transfer function given in (19).

B. Time domain simulation

Computer simulations in the time domain are carried out to evaluate the performance of the newly proposed TQT1-PLL as compared to the conventional QT1-PLL published in [14]. The parameters of the grid voltage fundamental component and controller are reported in Table IV. Two patterns of harmonic components in the grid voltages are used as shown in Table V. The value of K_p for TQT1-PLL is selected to achieve a *PM* equal to 50° based on the first-order Padé approximation model. As for the QT1-PLL, the value of K_p is equal to the one used in [14]. In order to avoid repetition of results published by previous research works, only the case of harmonic distortion and unbalance of the grid voltages with frequency jump is addressed in this section. Indeed, the only drawback of conventional QT1-PLL is its weakness against this type of grid disturbance. A first simulation test is therefore made with a grid voltage pattern involving the harmonic content shown in Table V (test 1) and an abrupt frequency jump of +5 Hz. Such test conditions are selected to highlight the performance of the proposed PLL under extreme frequency deviation. Fig. 23 illustrates the frequency error responses obtained with the conventional and proposed PLL algorithms. As can be seen, the conventional QT1-PLL provides a low-frequency ripple in steady state operation that is ranged between ± 1 Hz. This disturbing ripple is mitigated with the newly proposed TQT1-PLL; its amplitude is less than ± 0.025 Hz. Fig. 24 illustrates the phase error responses obtained with both, the conventional and proposed PLL algorithms. The conventional QT1-PLL provides a phase error ripple varying between ± 4 deg. With the proposed TQT1-PLL, the ripple amplitude is decreased down to ± 0.01 deg.

A second simulation test is also made with the harmonic content shown in the third column of Table V (test 2). The frequency and phase error responses obtained with both algorithms (QT1-PLL and TQT1-PLL) are displayed in Fig. 25 and Fig. 26 respectively. Though the amplitude of harmonics has been reduced, the ripples of both phase error and frequency error responses obtained with the conventional QT1-PLL still exist. The enhanced performances of the proposed TQT1-PLL are also verified through this second simulation scenario and confirm its capability to reduce the PLL gain at harmonic frequencies during off-nominal frequency operation. This outcome will enable the proper operation of the GSC under harmonic distortion of grid voltages and including dedicated control of harmonic currents since a strict accuracy is required for the reference frame transformations [9].

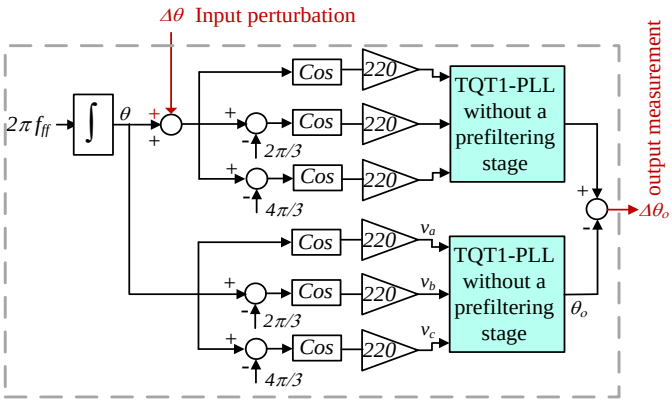

Fig. 21. Frequency analysis with an input phase perturbation

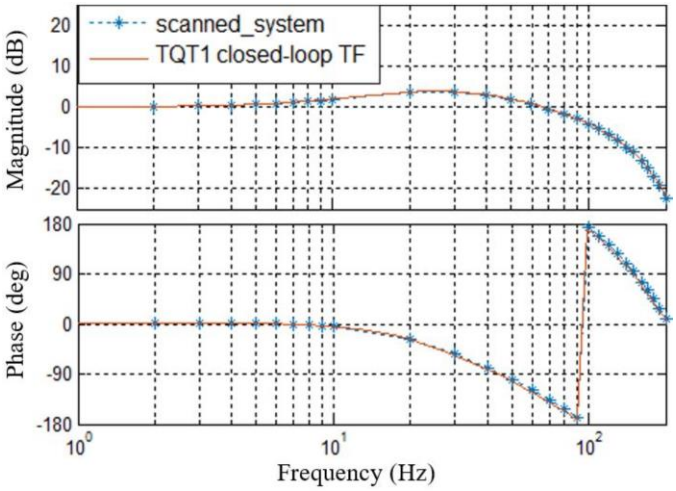

Fig. 22. Bode plot of TQT1 PLL's closed-loop transfer function and the frequency scan results

TABLE IV
PARAMETERS OF THE GRID VOLTAGE AND CONTROLLER

Parameter	QT1-PLL	TQT1-PLL
RMS value of the FFPS	220 V	220 V
Grid voltage fundamental frequency (f_{ff})	50 Hz	50 Hz
Controller's sample time (T_s)	10^{-4} s	10^{-4} s
MAF's order	1	3
MAF's window length (T_ω)	0.01 s	0.0033 s
Proportional gain (K_p)	92.34	79.5
Compensation gain (K_φ)	-	10^{-3}
Number of FDSC's delayed samples (N_d)	-	10

TABLE V
GRID VOLTAGE HARMONICS RATIOS

Harmonic Order	Amplitude (%) test 1	Amplitude (%) test 2	Sequence
1	30	30	-
5	30	20	-
7	30	10	+
11	30	5	-
13	30	3	+

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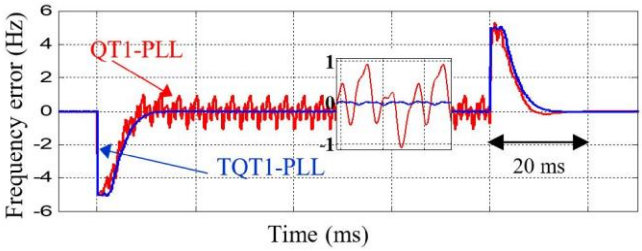

Fig. 23. Frequency error response under the harmonic content of Table V (test 1) and a frequency jump of 5 Hz

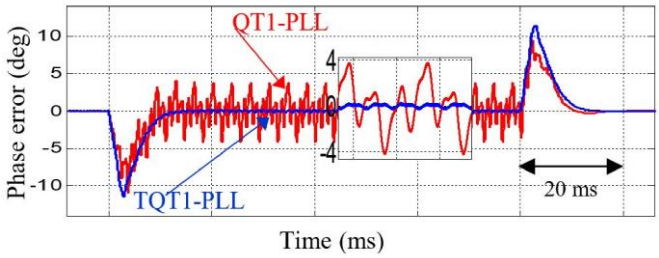

Fig. 24. Phase error response under the harmonic content of Table V (test 1) and a frequency jump of 5 Hz

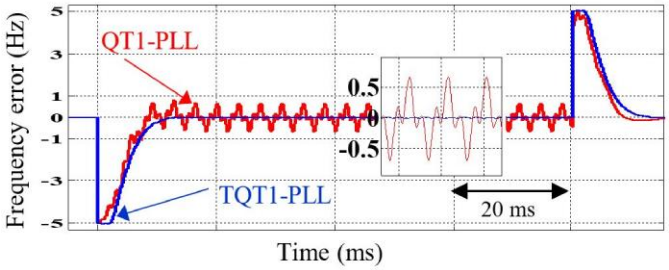

Fig. 25. Frequency error response under the harmonic content of Table V (test 2) and a frequency jump of 5 Hz

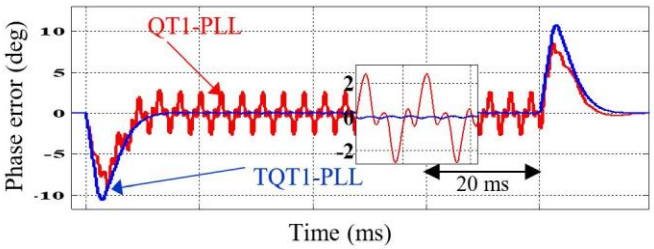

Fig. 26. Phase error response under the harmonic content of Table V (test 2) and a frequency jump of 5 Hz

C. *Real-time implementation*

The proposed and conventional PLL algorithms are implemented in real-time on a 32-bit floating point digital signal processor (DSP) TMS320F28335 from Texas Instruments running at a clock frequency of 150 MHz and using the same parameters of numerical simulations. The grid voltages pattern including the harmonic contents of Table V (test 2) and the frequency jump of +5 Hz are emulated in real-time on the same DSP. The instantaneous values of the frequency and phase errors are sent to two enhanced pulse width modulation (epwm) output modules of the DSP to make a digital to analog conversion of the internal variables. These are displayed on a digital oscilloscope that is equipped with a low-pass filter to eliminate the high frequency components caused by the pulse width modulation operation of the original signal. The obtained results are displayed in Fig. 27 and Fig. 28 respectively. As can be seen, the real-time waveforms of frequency and phase error responses are consistent with those obtained with computer simulations. Indeed, the conventional QT1-PLL provides an important ripple around zero in the frequency and phase errors waveforms. As for the proposed TQT1-PLL algorithm, the amplitude of the ripple is reduced where the phase and frequency errors remain close to zero in steady state operation. Notice also that this steady state performance is achieved without affecting the dynamic response of the proposed algorithm, which provides approximately the same settling time as compared to the conventional QT1-PLL. It can therefore be concluded that the proposed TQT1-PLL is robust against harmonically distorted grid voltage with a frequency jump.

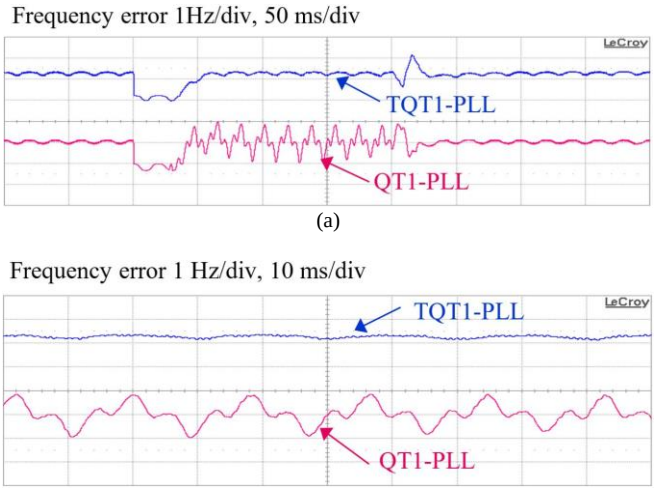

Fig. 27. (a) Frequency error response obtained in real-time under the harmonic content of Table V (test 2) and a frequency jump of 5 Hz (b) zoon in during steady-state operation

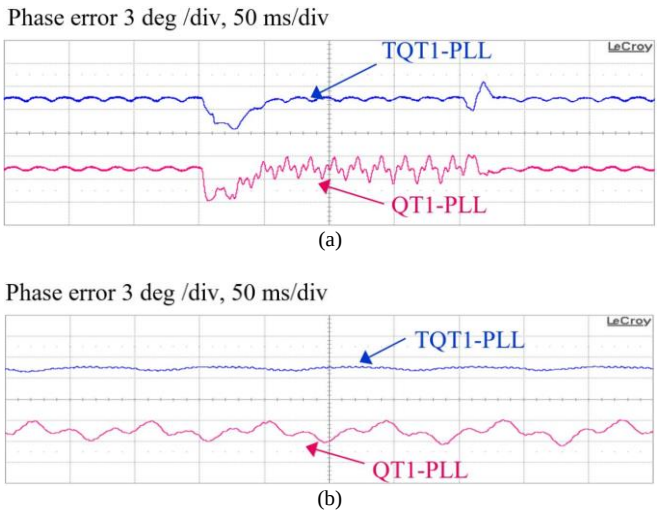

Fig. 28. (a) Phase error response obtained in real-time under the harmonic content of Table V (test 2) and a frequency jump of 5 Hz (b) zoon in during steady-state operation

VI. CONCLUSION

This paper presented a systematic design and stability analysis of a new QT1-PLL referred to as TQT1-PLL. The suggested technique was based on the use and design of an in-loop third-order MAF with a reduced window and a second-order FDSC based prefiltering stage. The performance and robustness of the proposed PLL technique were tested under the worst operation case i.e. highly distorted grid voltages with frequency jump. The obtained results showed its ability to reduce the ripple in the estimated grid frequency and phase. The proposed PLL could therefore enable the proper operation of the GSC under harmonic distortion of grid voltages and including dedicated current harmonic compensators that need a strict accuracy of the reference frames transformation.

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Mohamed Mellouli was born in Sousse in 1989. He received his engineer and M.S. degrees from the National Engineering School of Sousse, University of Sousse, Tunisia, in 2014.

He is currently working toward the Ph.D. degree in electrical engineering at the National Engineering School of Sousse, University of Sousse, Tunisia. He is a member of the research Laboratory of Advanced Technology and Intelligent Systems (LATIS), National Engineering School of Sousse, University of Sousse. His research interests are focused on grid-connected inverters, PLL based synchronization techniques, and power quality.

Mahmoud Hamouda (M'15–SM'20) received his B.S., Agregation, M.S., and Ph.D. degrees, all in electrical engineering, from ENSET and the Ecole Superieure des Sciences et Techniques, University of Tunis, Tunisia, in 1995, 1996, 2004, and 2010, respectively. He received the HDR from the University of Sousse in 2017.

He is currently a Professor of electrical engineering with ISSAT at the University of Sousse, Tunisia. He is affiliated with Canada Research Chair in Electric Energy Conversion and Power Electronics, Ecole de Technologie Supérieure in Montreal, Canada. He is also a member of the research laboratory LATIS, National Engineering School of Sousse, University of Sousse, Tunisia. His main research interests include renewable energy conversion systems, digital signal processor, and field-programmable gate array for embedded real-time control, grid-connected converters, and fault diagnosis of power converters.

Jaleleddine Ben Hadj Slama (M'09–SM'13) was born in Akouda, Tunisia, on May 30, 1971. He received the engineer and the Ph.D. degrees, both in electrical engineering, from Ecole Centrale de Lyon, Lyon, France, in July 1994 and December 1997 respectively.

Since 2015, he has been a full Professor in Electrical Engineering at the National Engineering School of Sousse, Tunisia, where he is the leader of the EMC research group in the LATIS laboratory. His main research interests include electromagnetic compatibility of transportation systems, near-field techniques, EMI issues of power electronics systems and their modeling, smart grid, renewable energy and development of remote laboratories for internet based engineering education.

Kamal Al-Haddad (S'82–M'88–SM'92–F'07–LF'20) received his B.Sc.A. and M.Sc.A. degrees from the University of Québec à Trois-Rivières, Canada in 1982 and 1984, respectively, as well as his Ph.D. degree from the Institut National Polytechnique, Toulouse, France in 1988.

Since June 1990, he has been a Professor at the École de Technologie Supérieure, Montreal, where he has been the holder of the senior Canada Research Chair in Electric Energy Conversion and Power Electronics since 2002. He has supervised more than 150 Ph.D. and M.Sc.A. students and co-authored more than 600 papers and 2 books. His fields of interest are in high-efficiency power electronic converters, active and hybrid filters, modular multilevel converter, multilevel converters, and active rectifiers, including modeling, control, and development of industrial prototypes.

Prof. Al-Haddad is the 2016-2017 President of the IEEE Industrial Electronics Society and a fellow member of the Canadian Academy of Engineering.